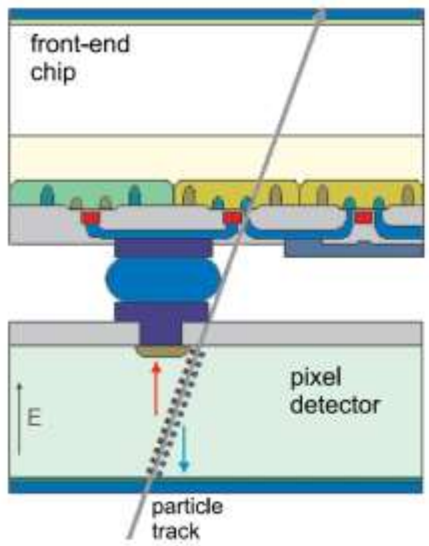
UNIVERSITÄT BONN

SI LAB Silizium Labor Bonn

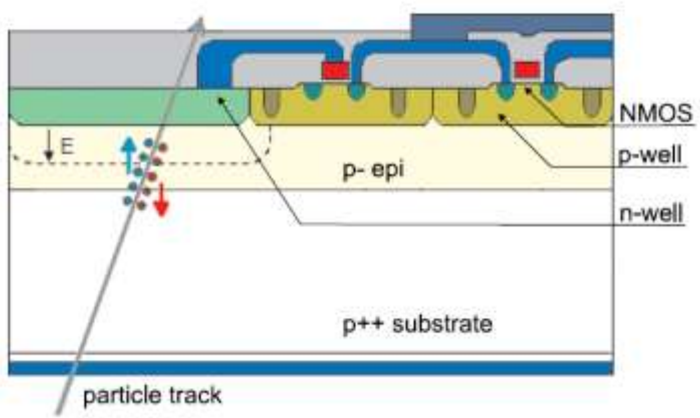
Overview and perspectives of depleted CMOS sensors

Tomasz Hemperek

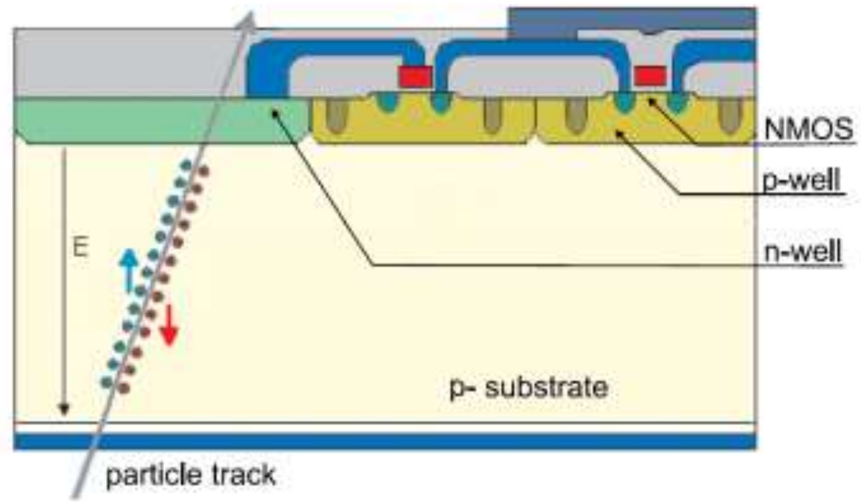
Hybrid Pixel Detectors



Monolithic Pixels

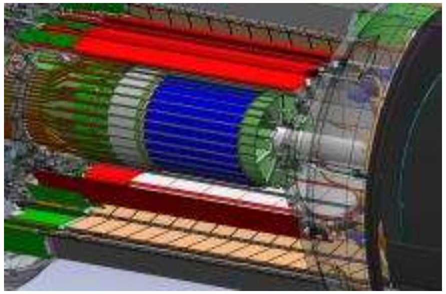


Depleted Monolithic Pixels

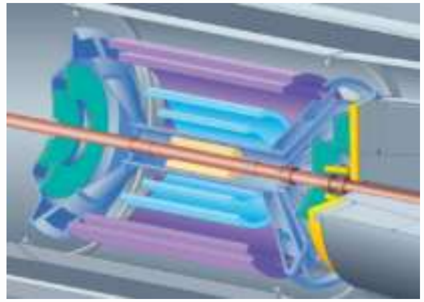


Introduction

STAR

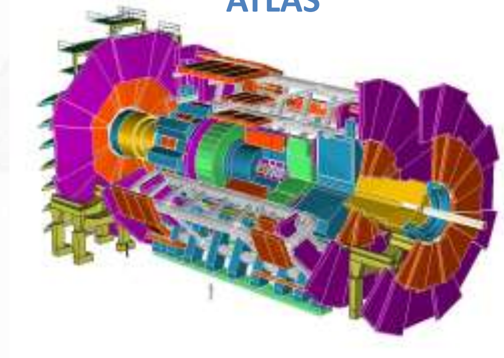


ALICE-LHC



ILC

ATLAS

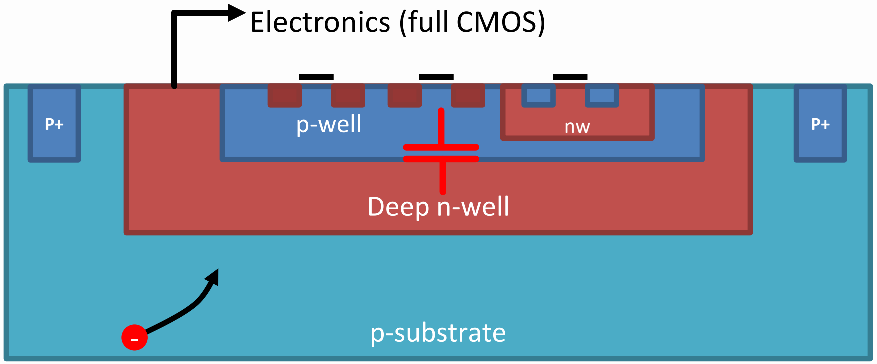


Requirements for inner pixel layers

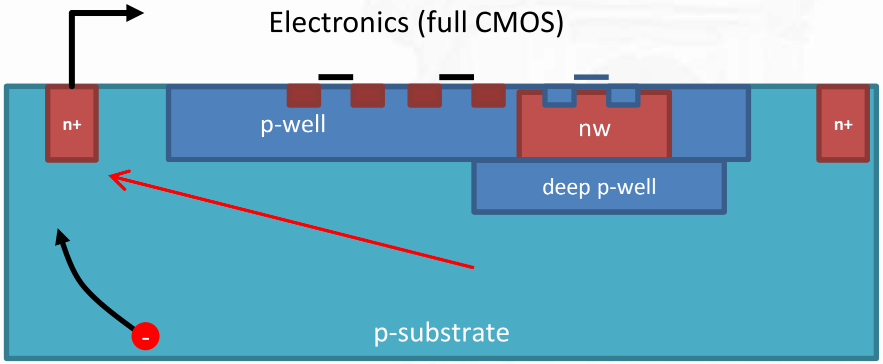
	STAR	ALICE-LHC	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	**25**	**25**
Particle Rate [kHz/mm^2]	100	10	250	1000	10000
Fluence [n_{eq}/cm^2]	> 10^{12}	> 10^{13}	10^{12}	**2×10^{15}**	**2×10^{16}**
Ion. Dose [Mrad]	> 0.3	0.7	0.4	**80**	**>500**

Bulk process options (simple options, n-on-p)

Charge signal



Charge signal



Electronics **inside** charge collection well

- Collection node with **large fill factor** → rad. hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

Electronics **outside** charge collection well

- Very **small sensor capacitance** → low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep-p implant

Consequences of the additional inter-well capacitance

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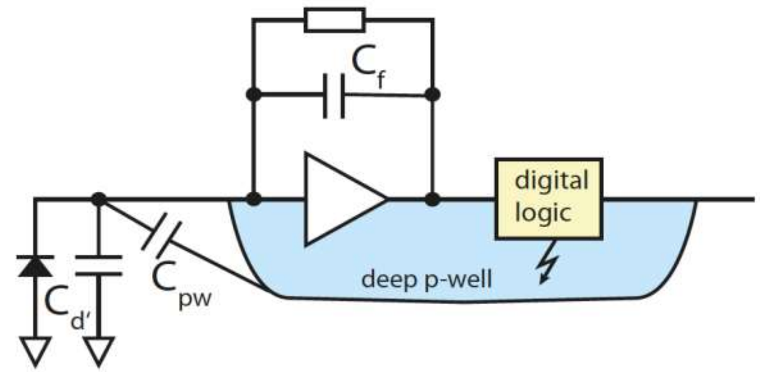
- larger total detector capacitance: $\mathbf{C_d} = C_{d'} + C_{pw}$



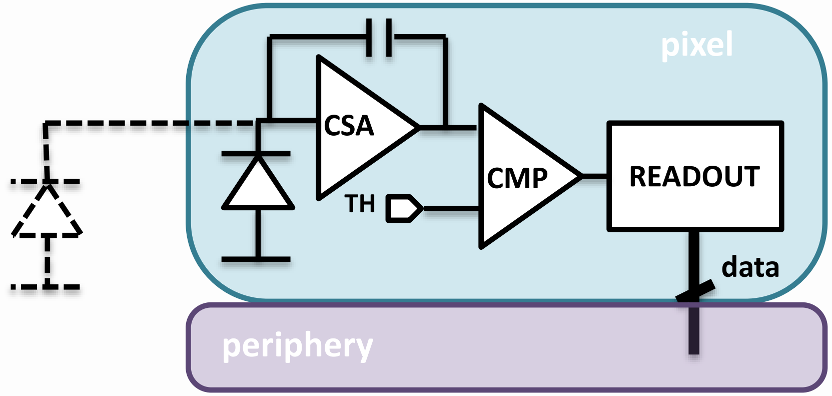
- noise $$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$$

- timing $$\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$$

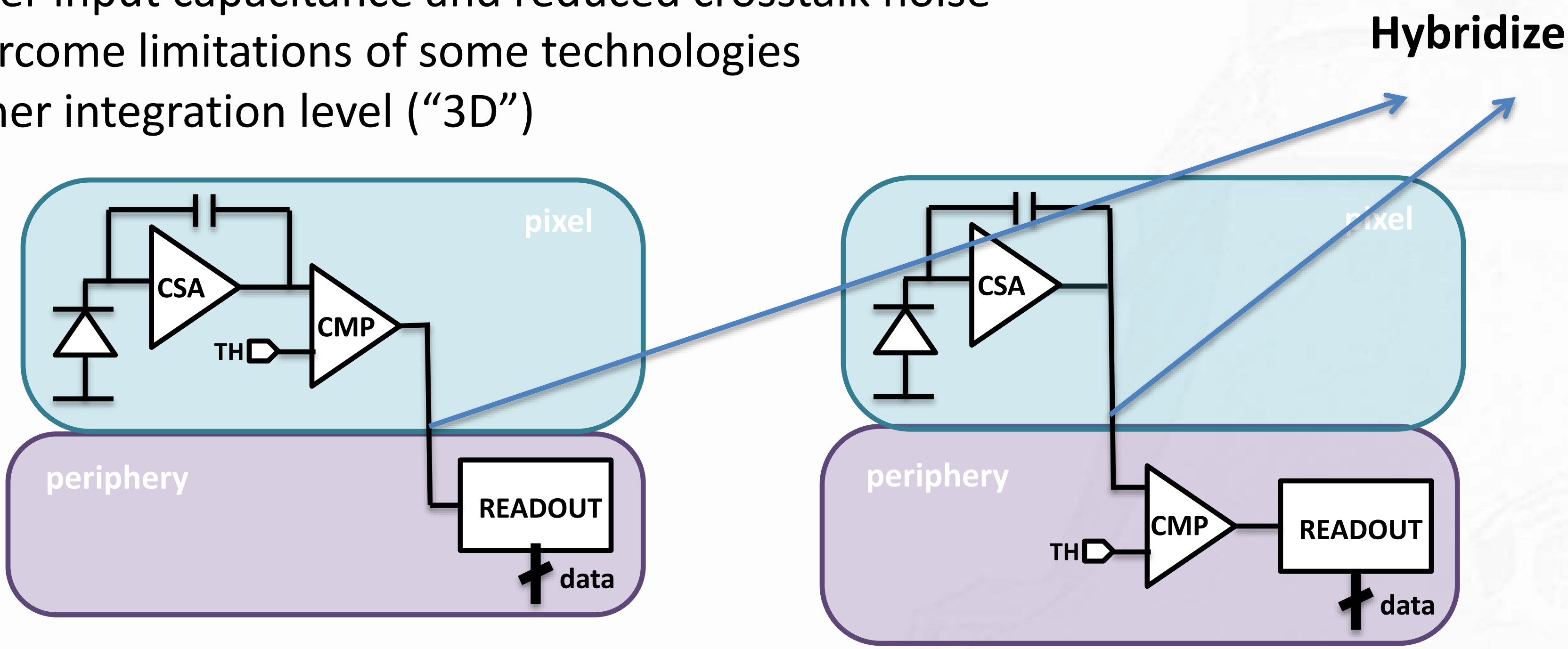
need to increase g_m to compensate
=> increased power ($g_m \propto I_d$)

- cross talking into sensor
The PW/DNW capacitance C_{pw} directly couples into the sensor (the CSA input node).
Even with careful layout and low noise digital circuitry the operation threshold can be affected.
For example: for C_{pw} = 100 fF, ΔV_{pw} = 1mV => $Q_{x\text{-talk}}$ = 625 e^-

Readout concepts

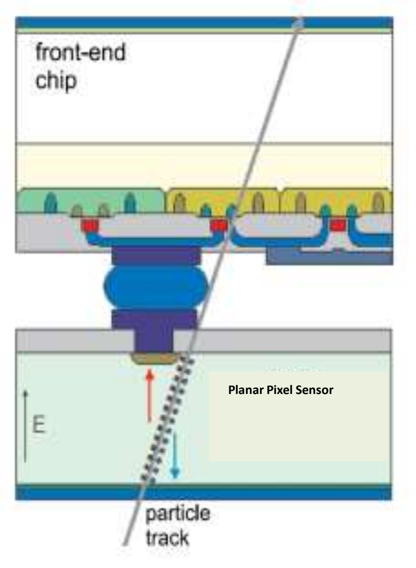


- Lower input capacitance and reduced crosstalk noise
- Overcome limitations of some technologies
- Higher integration level (“3D”)



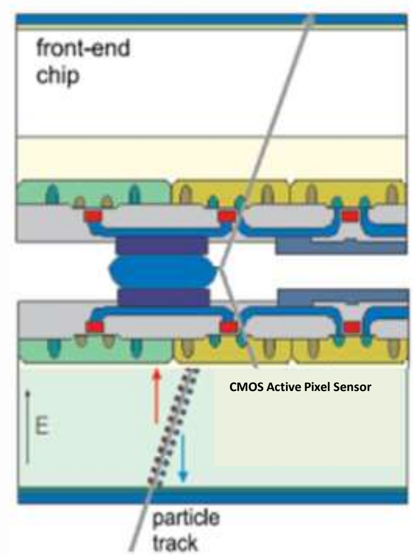
Configurations

Standard Hybrid



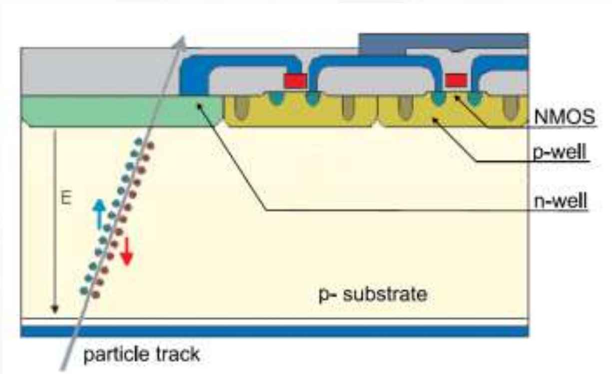
with CMOS planar sensor

CMOS Active Hybrid



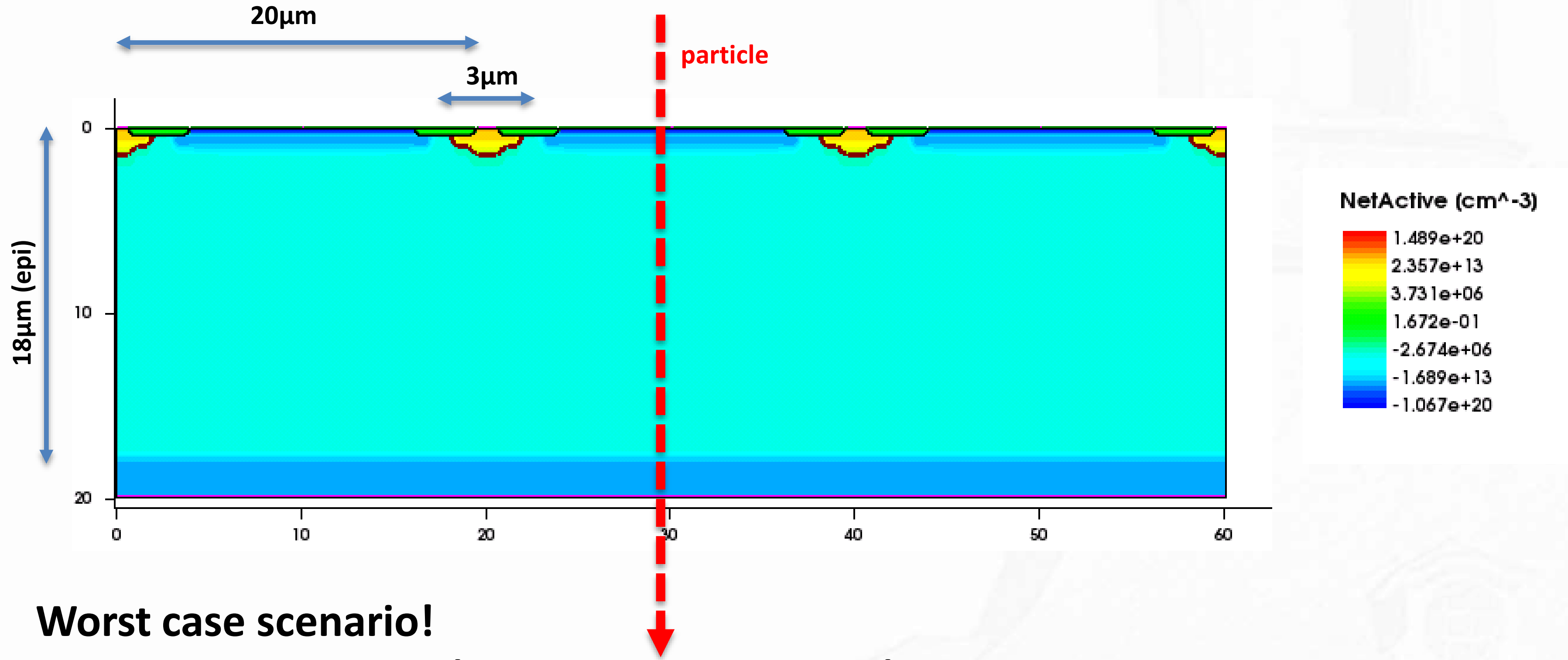
bumped, glued or bonded

Depleted Monolithic



Sensor Design Paramters

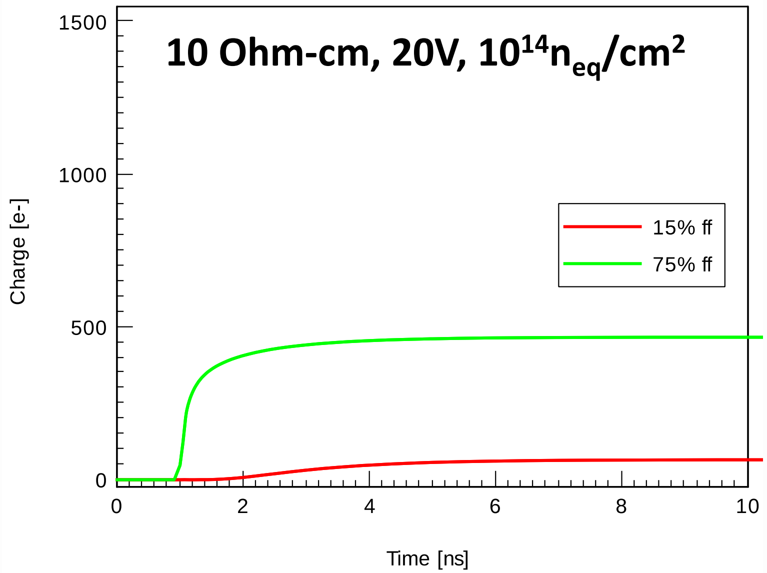
- Substrate doping concentration (resistivity)
- Maximum sensor bias voltage
- Geometry (thickness, fill-factor)

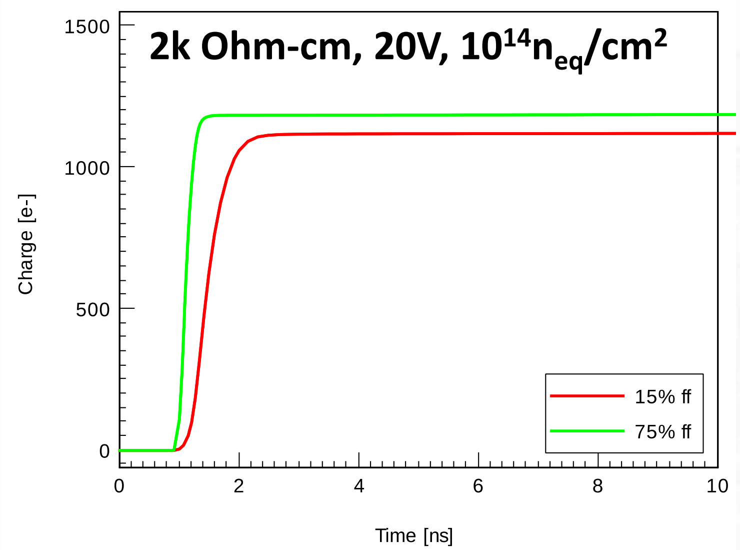


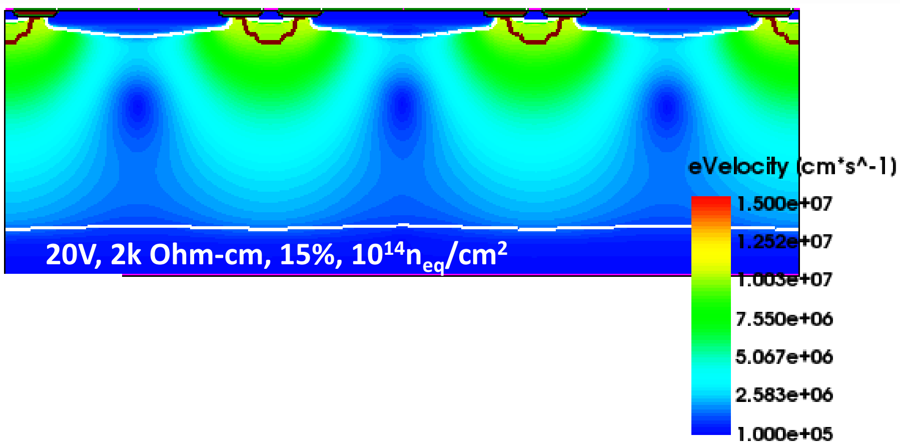
- **Worst case scenario!**
- **No acceptor removal (this is only simulation)**

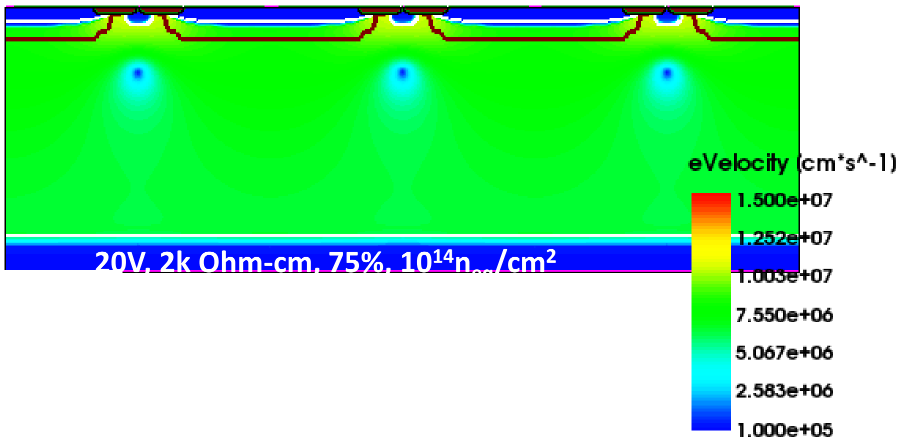
Code: https://gitlab.cern.ch/TCADExamples/ChargeCollection

Geometry/Fill Factor





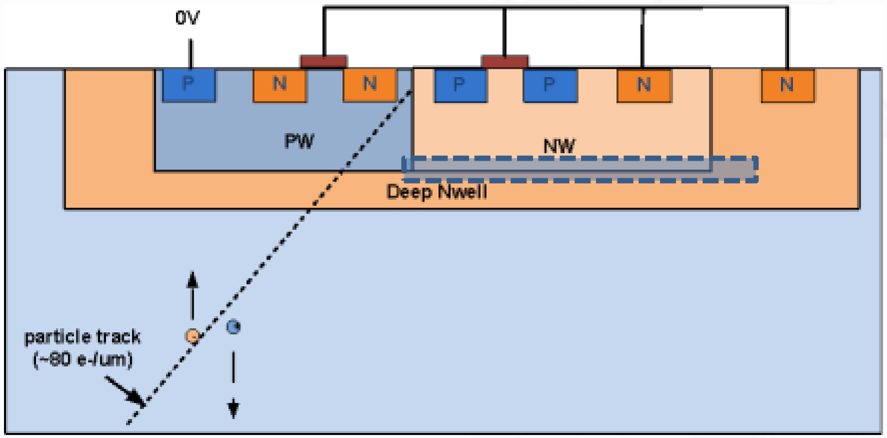


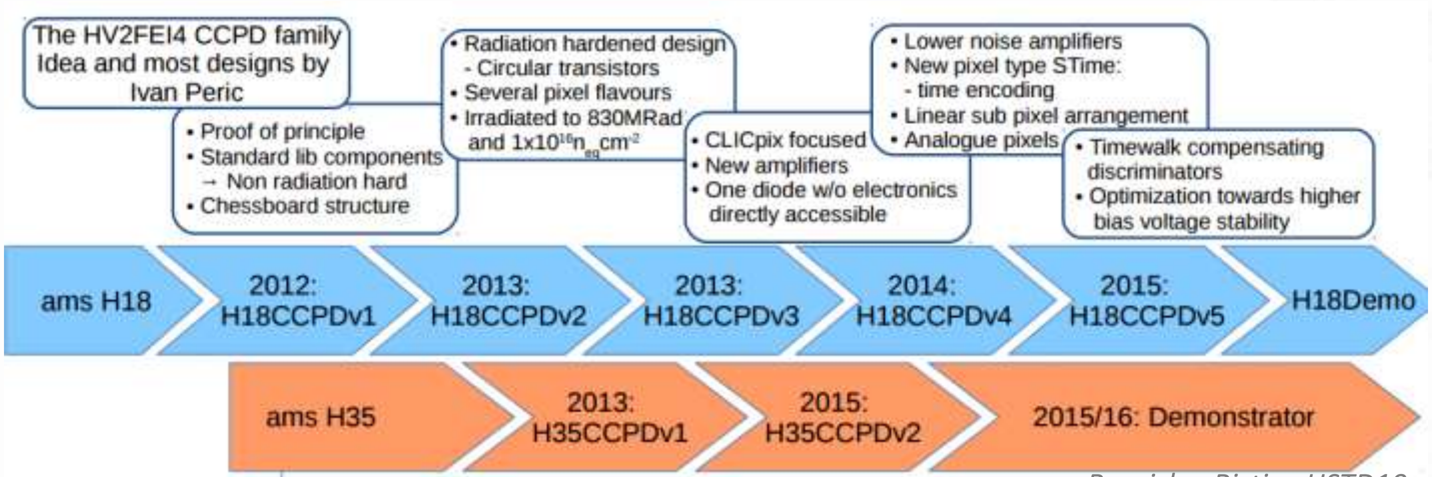


CMOS Devices Performance

AMS 180nm/350nm

- Substrate: **10 (initially) – 2k Ohm-cm**
- Bias: >60 – 100 V
- 180nm/350nm
- 3-6 metal layers
- KIT, Geneva, Barcelona, Liverpool, CCPM, CERN, Bonn , ..



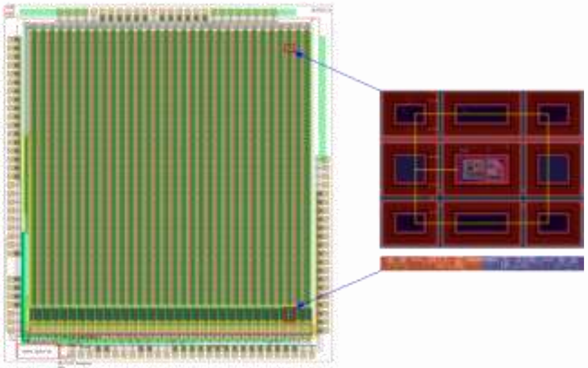


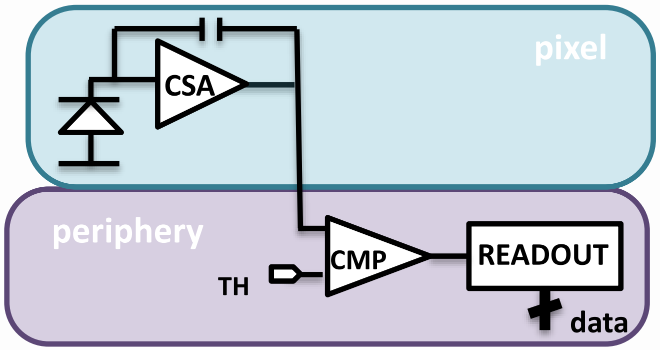
Branislav Ristic - HSTD10

- Initially low resistive substrate now also **high**
- Initially no **PMOS isolation** -> now also available

I. Peric et al. Nucl.Instrum.Meth. A582 (2007) 876-885
Nucl.Instrum.Meth. A765 (2014) 172-176

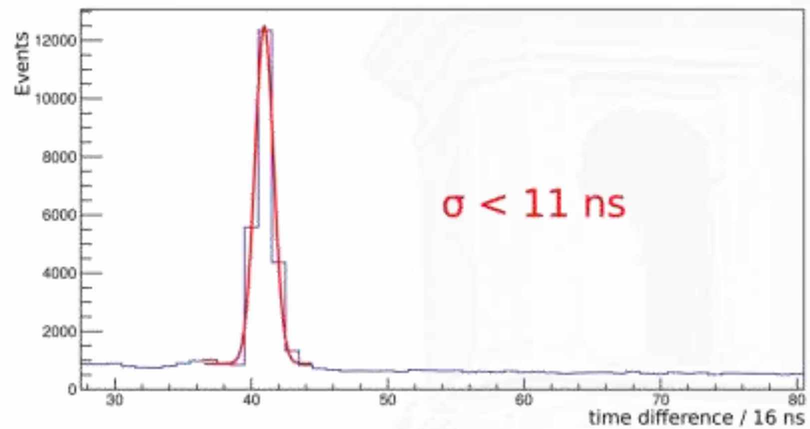
AMS 180 – MuPix7 - Mu3e @ PSI



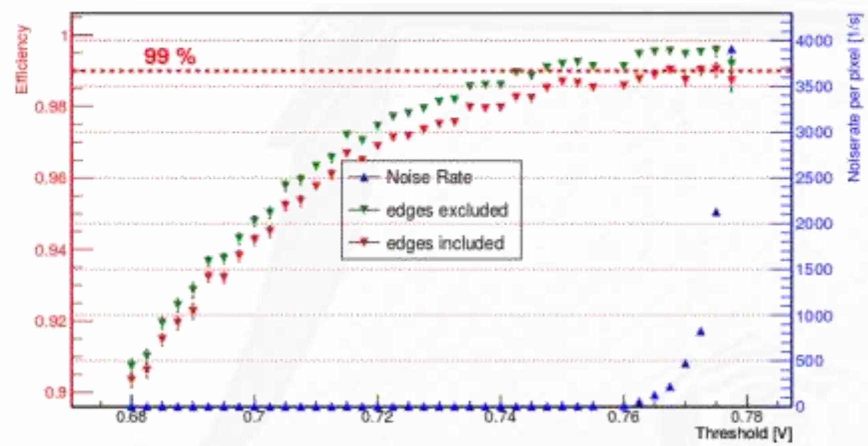


Technology: AMS 180nm
Design: KIT
Dimension: 40 x 32 pixels (103 x 80 μm^2 each)
Preamplifier Inside pixel cell
Bias: 85V
Substrate 20 Ohm-cm, 80 Ohm-cm for MuPix8

Timestamping resolution:

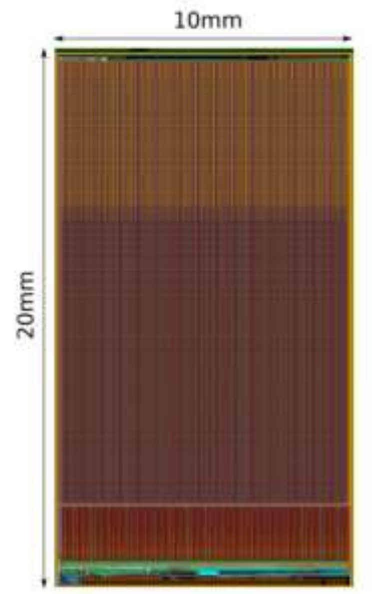


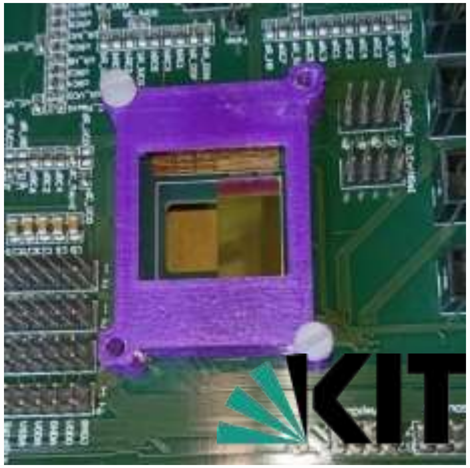
Efficiency:



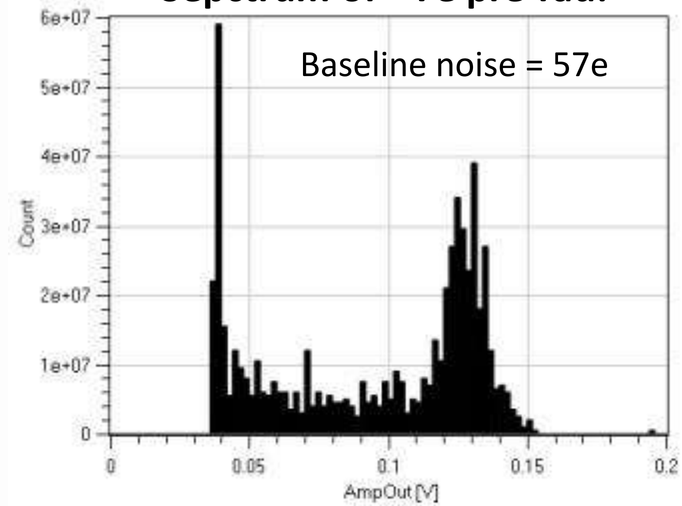
Dirk Wiedner, VCI2016

AMS 180 – MuPix8 – First Results

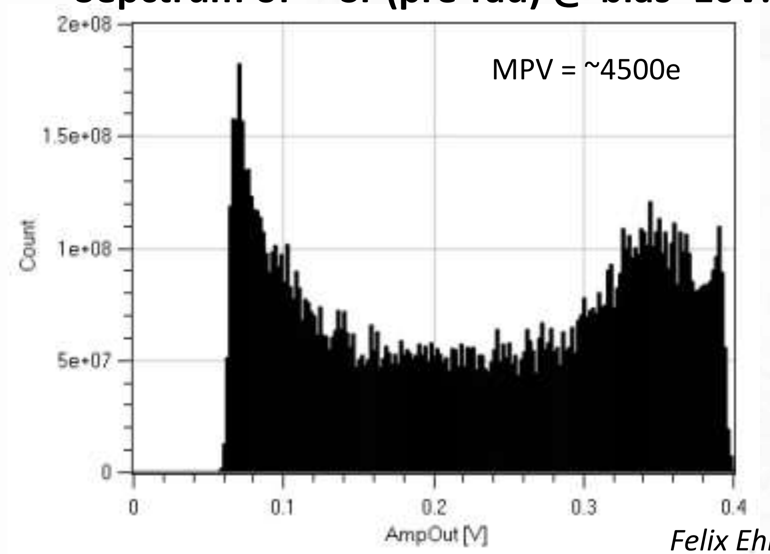




Sepctrum of ^{55}Fe pre-rad:



Sepctrum of ^{90}Sr (pre-rad) @ bias=10V:



Felix Ehrler (KIT)

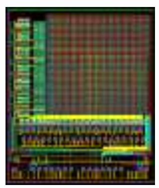
Technology: AMS 180nm
Design: KIT
Dimension: 128 x 200 pixels (80 x 80 µm^2)
Output: 4 x 1.25 Gbps
Preamplifier: Inside pixel cell
Substrate : 80 Ohm-cm
Readout: Monolithic
Characterization ongoing

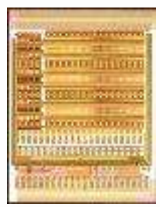
AMS 180 - CCPDv4

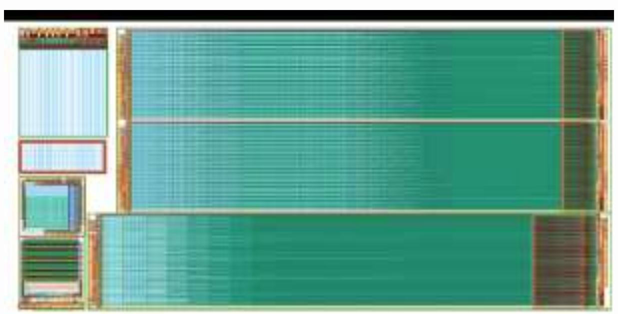
Technology: AMS 180nm
Dimension: 24 x 36 pixels (125x 33μm^2 each)
Bias: > 60V
Substrate: 20 Ohm-cm (80/200/1k)

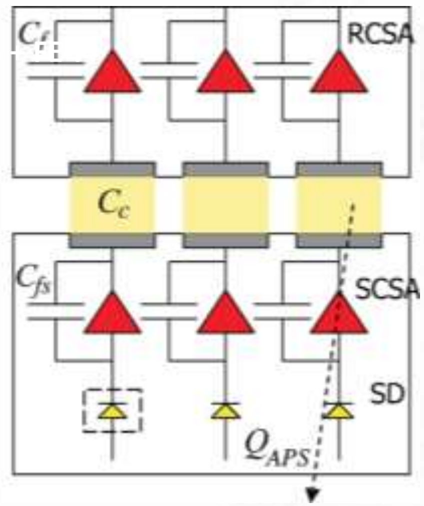

CCPDv1

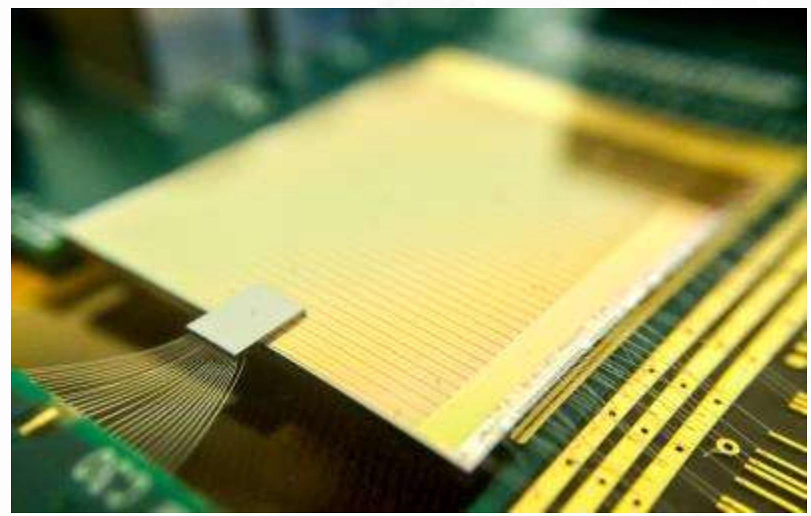

CCPDv2


CCPDv3

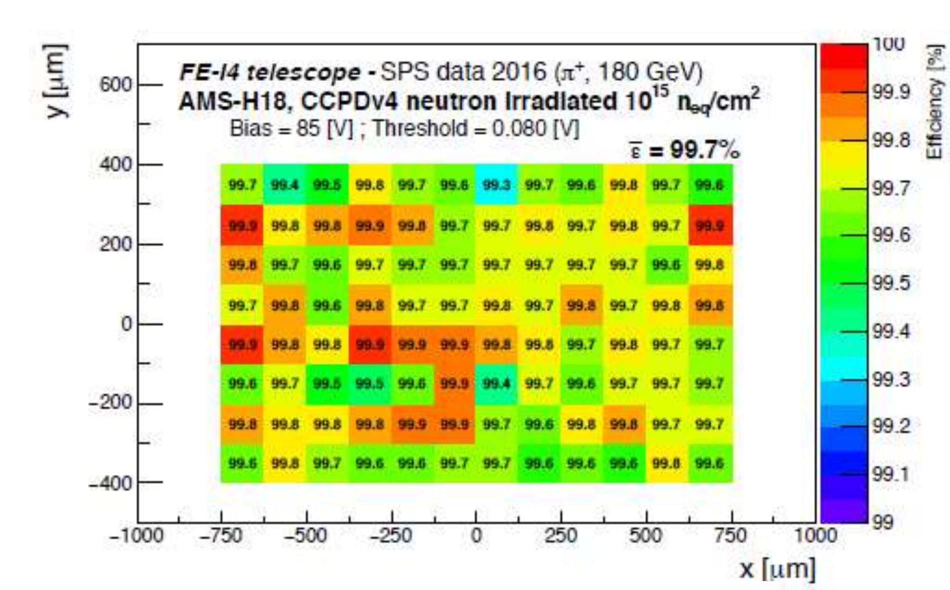

CCPDv4

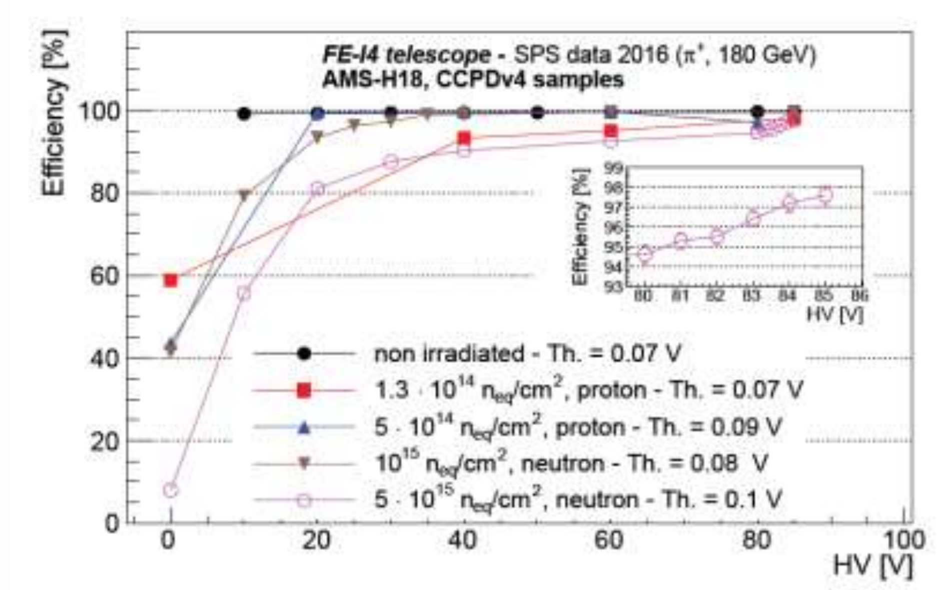

ATLASPIX



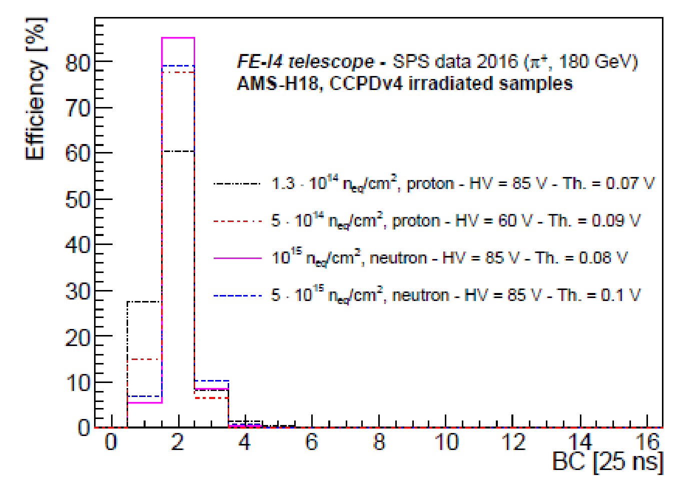


AMS 180 - CCPDv4 - Efficiency





Arxiv : 1611.02669



High detection efficiency above $10^{15}n_{eq}$

ATLASPIX (large monolithic design in AMS180) is being measured.

AMS 350 demonstrator (H35DEMO)

4 resistivity : 20Ωcm (standard), 80Ωcm, 200Ωcm, 1kΩcm

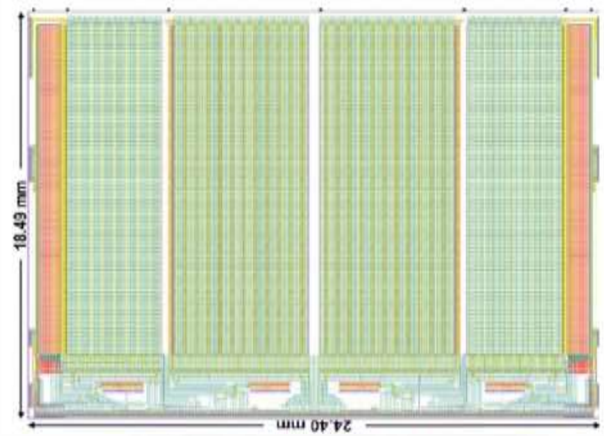
Device types:

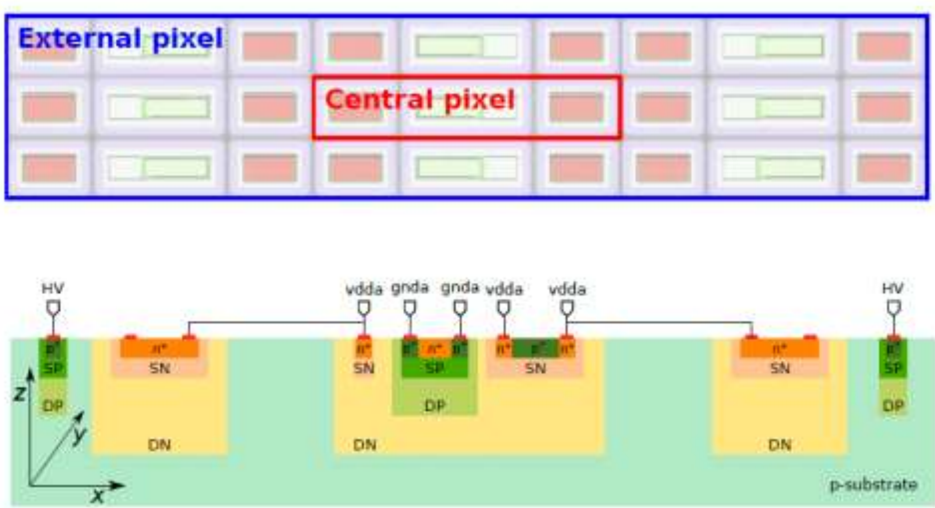
- Standalone nMOS matrix
- Analog matrix
- Standalone CMOS matrix (monolithic)

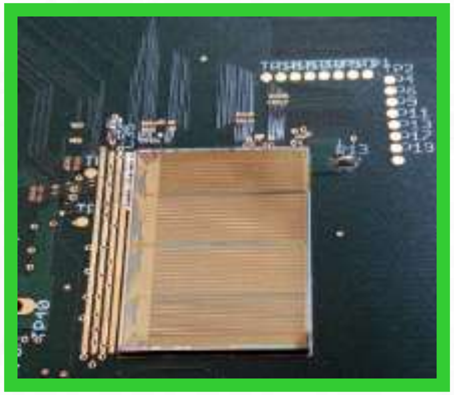
Demonstrated Bias up to 160V

Full readout + control in preparation for summer test beams

Irradiation campaign ongoing up to 1.5e15n_{eq}/cm^2

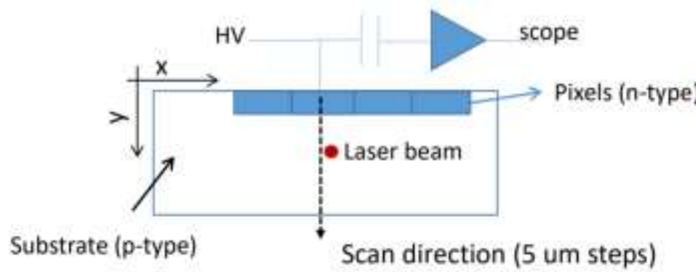




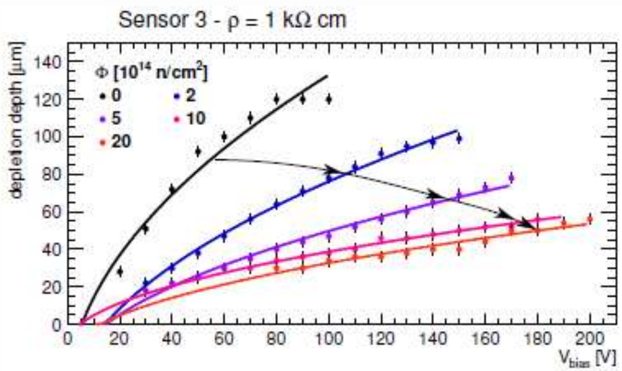


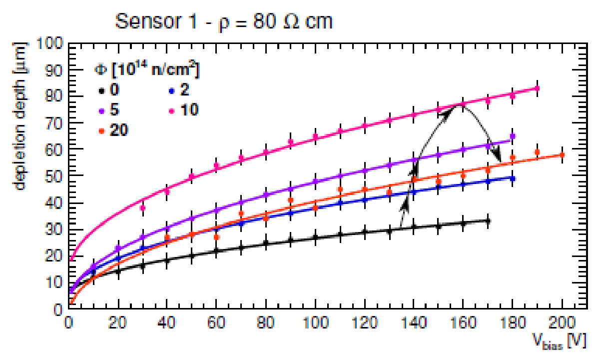
Strip development: CHESS-1, CHESS-2, …

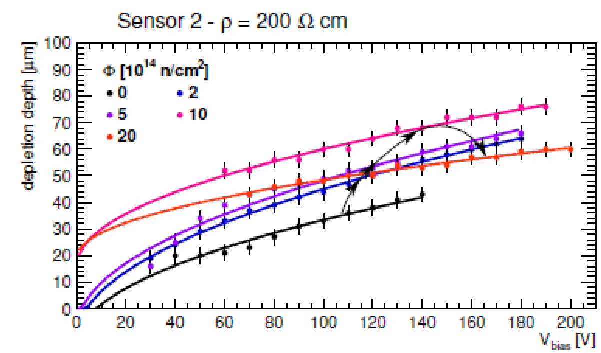
AMS350 - H35DEMO



Edge-TCT:

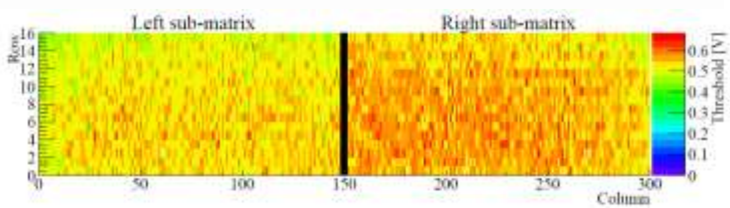


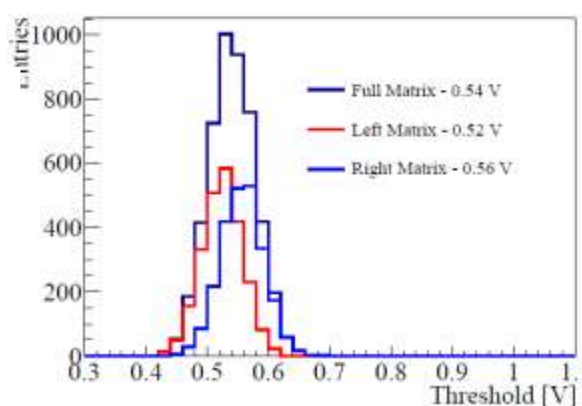




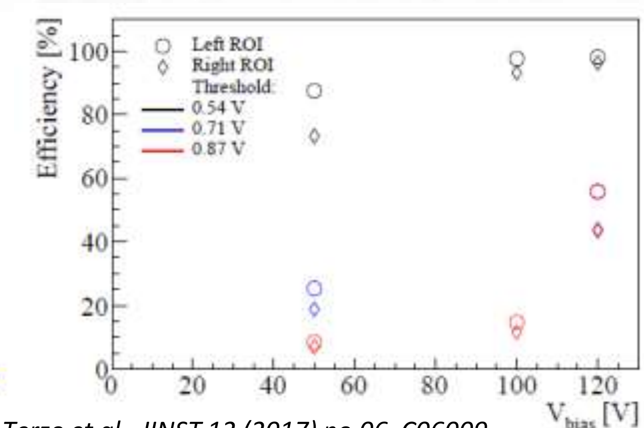
E.Cavallaro et al., JINST 12 (2017) no.01, C01074

Tuning



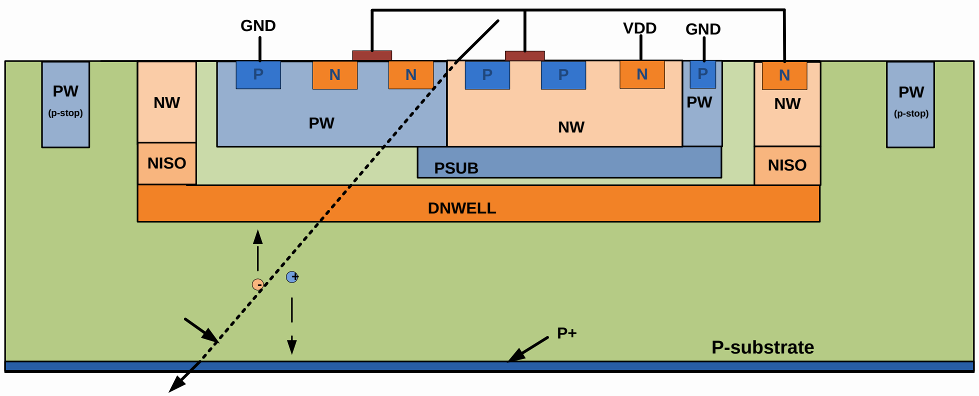


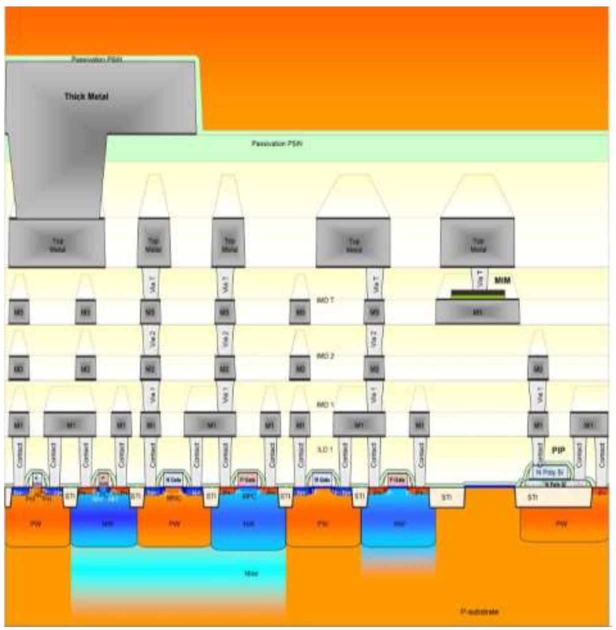
Efficiency



S.Terzo et al., JINST 12 (2017) no.06, C06009

LFoundry LF150





LFA150:

- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer: >2000 Ω·cm
- Small implant customization
- Backside processing

CCPD_LF prototype:

- Pixel size: 33um x 125 µm (6 pix =2 pix of FEI4)
- Chip size: 5 mm x 5 mm (24 x 114 pix)
- Bondable to FEI4 (+pixel encoding)
- **300um and 100um** version
- Bonn + CCPM +KIT

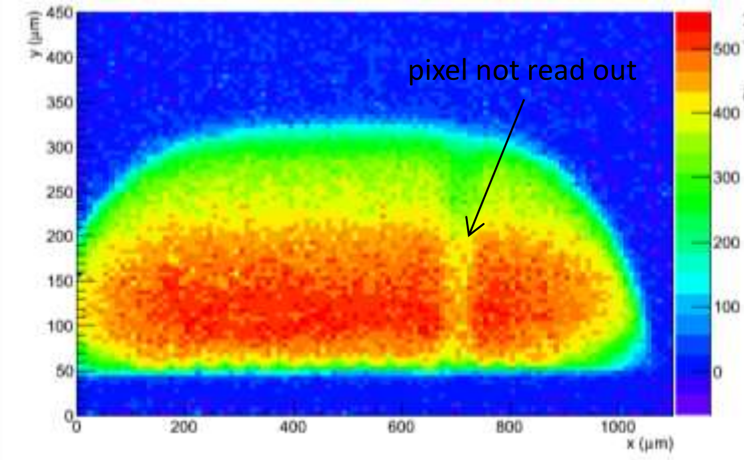
LF-CPIX (Demonstrator)

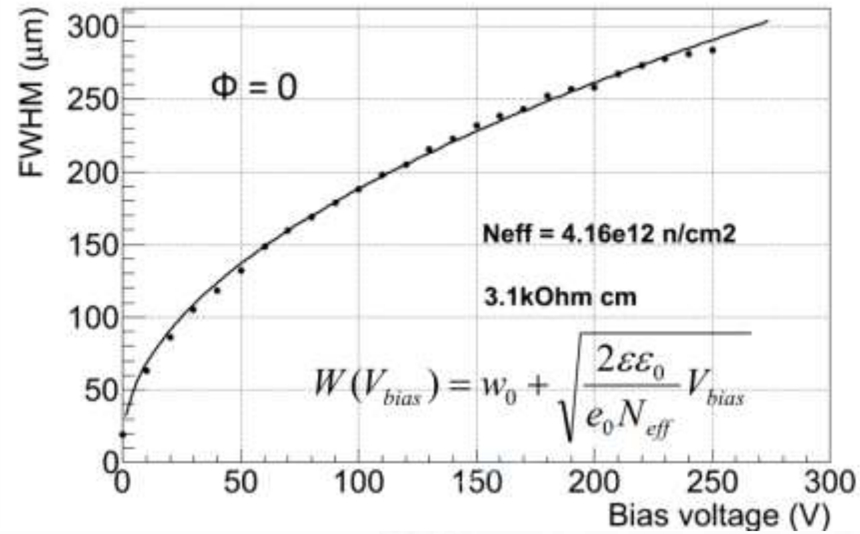
- Pixel size: 50um x 250 µm
- Chip size: 10 mm x 10 mm
- 200um and 100um version
- Bonn + CPPM + IRFU

LF-Monopix (monolitic FE-I4)

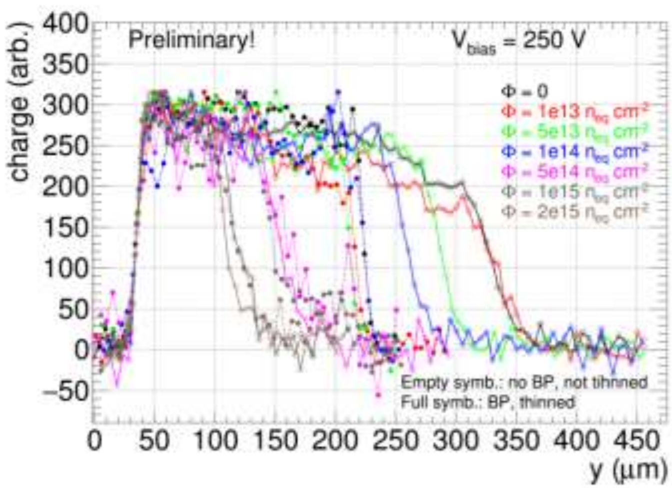
- Pixel size: 50um x 250 µm
- Chip size: 10 mm x 10 mm
- Bonn + CPPM + IRFU

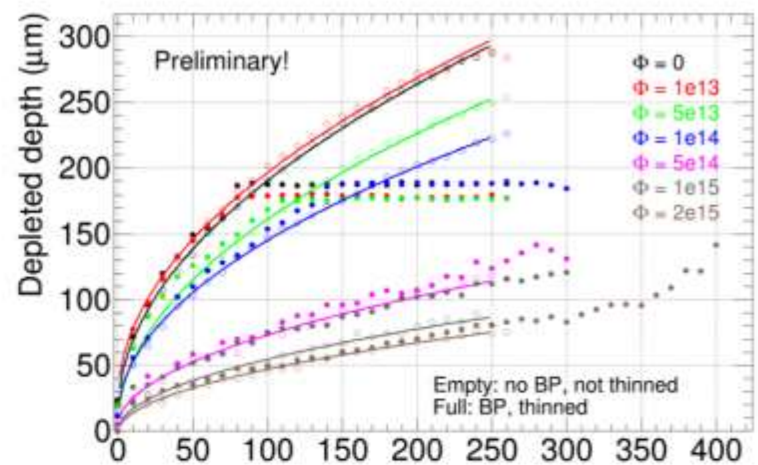
LFoundry - sensor performance – E-TCT





Edge-TCT for different fluence and backside:

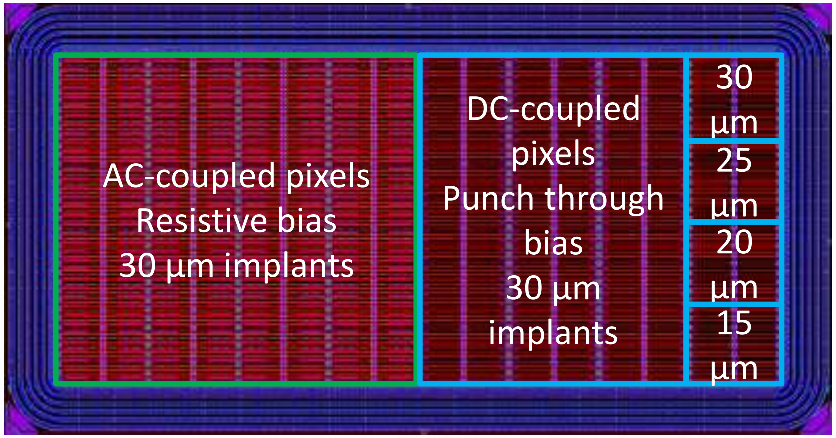


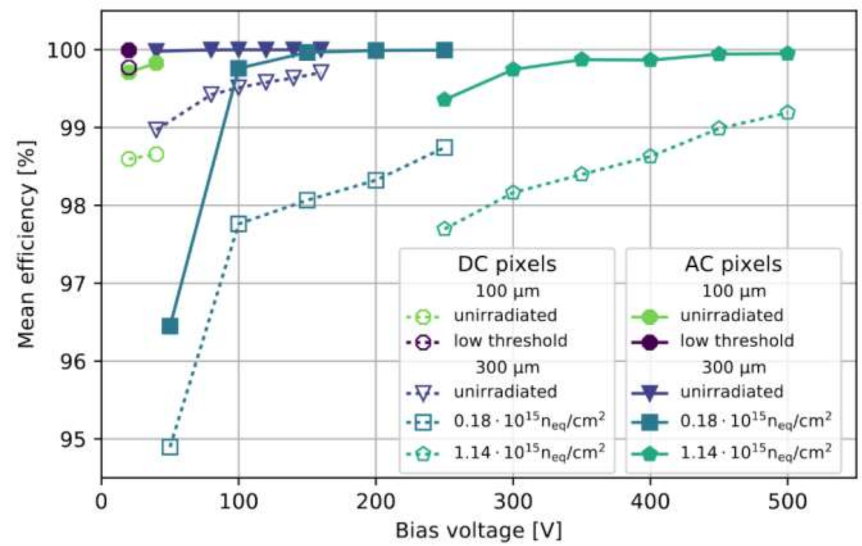


Igor Mandic, RD50 2017

Passive LFCMOS sensor prototype

- LFoundry 150 nm CMOS technology
- >2 kΩ-cm p-type bulk, 8“
- 100/300 µm thick, backside processed
- Bump bonded to the ATLAS FE-I4
- Pixel size: 50 µm x 250 µm
- Matrix size: 16 x 36 pixels (1.8 mm x 4 mm)
- Bonn + MPI



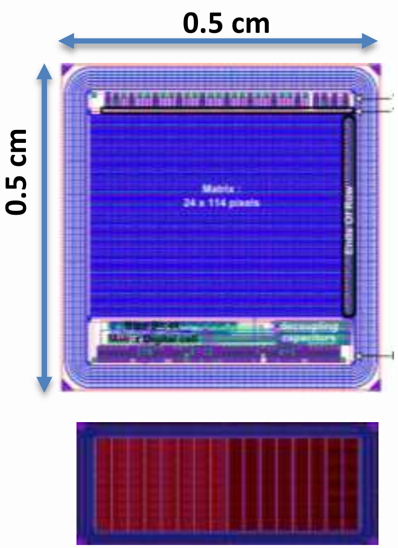


CMOS foundries can do good planar sensors (8”).

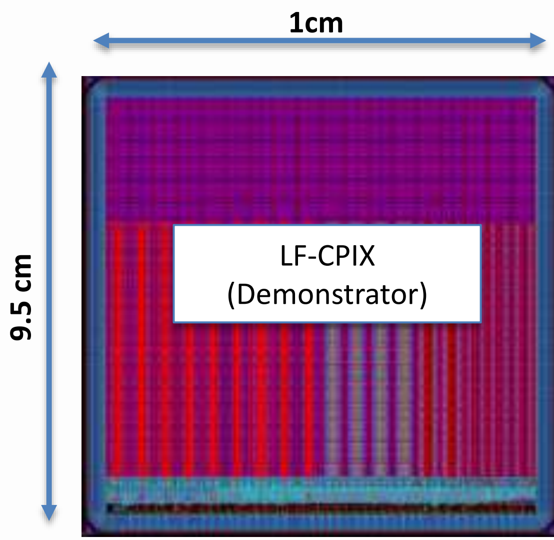
D.-L. Pohl et al., JINST 2017

113 of 114 measured sensors have identical parameters

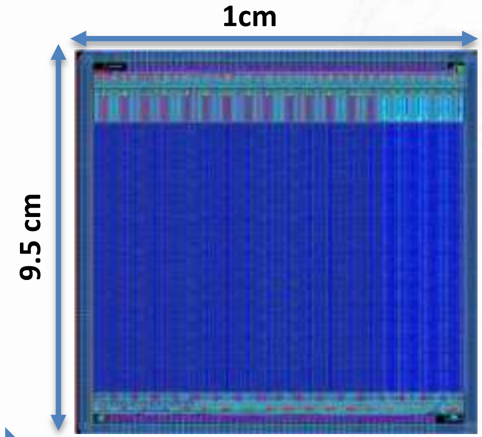
LFoundry timeline



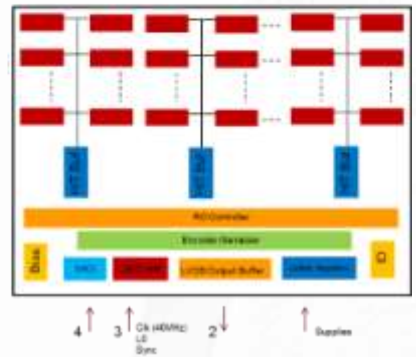
Bonn, CPPM ,KIT
CCPD_LF, ..(Aug. 2014)



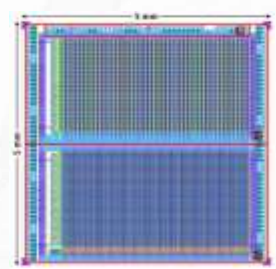
Bonn, CPPM ,IRFU
LF-CPIX (April 2016)



Bonn, CPPM ,IRFU
Monopix (Aug. 2016)

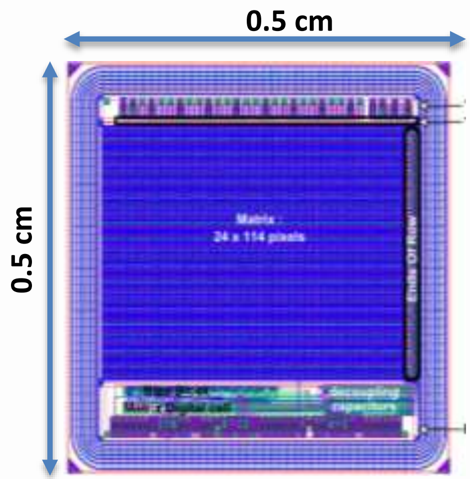


SLAC
COOL (Aug. 2016)

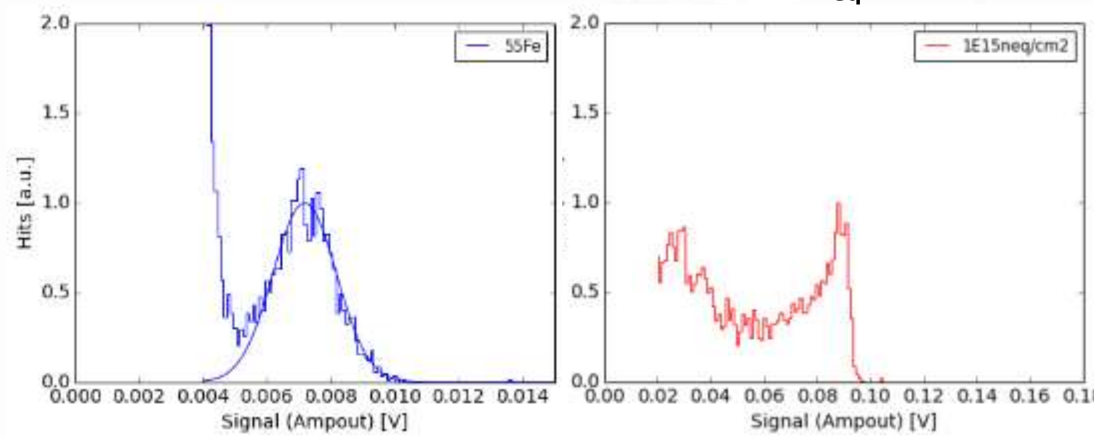


KIT, Liverpool, Barcelona, Geneva
LFHVMAPS_FEI4 (Aug. 2016)

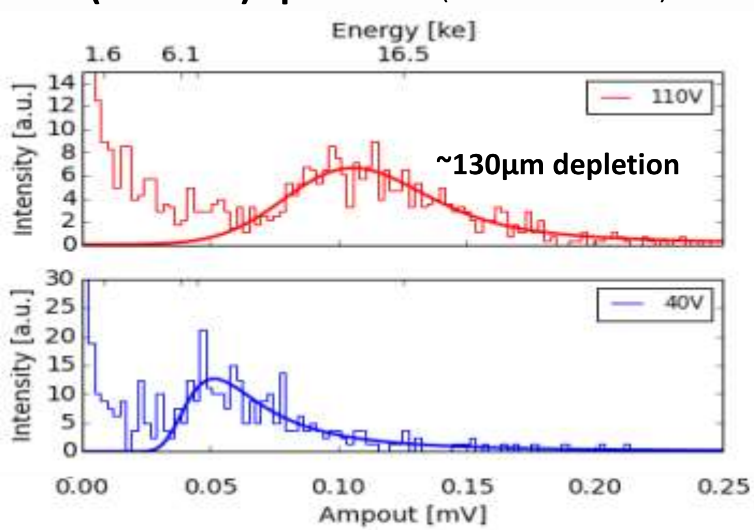
CCPD_LF results



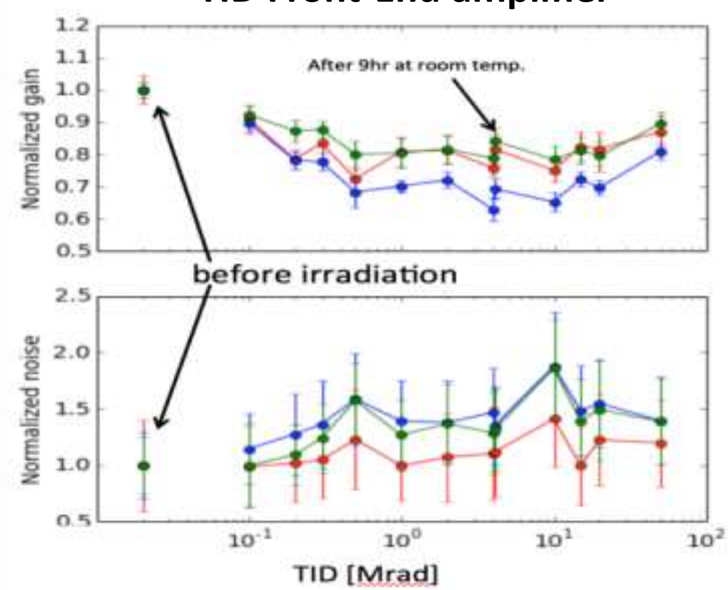
Sepctrum of ^{55}Fe and ^{241}Am after $10^{15} n_{eq}/cm^2$



MIP (3.2 GeV) spectrum (before radiation)



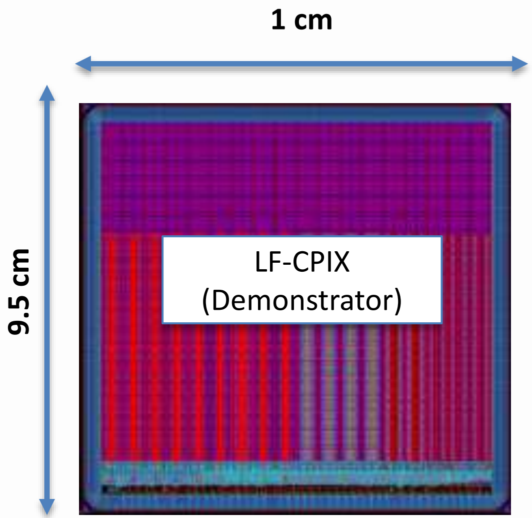
TID Front-End amplifier

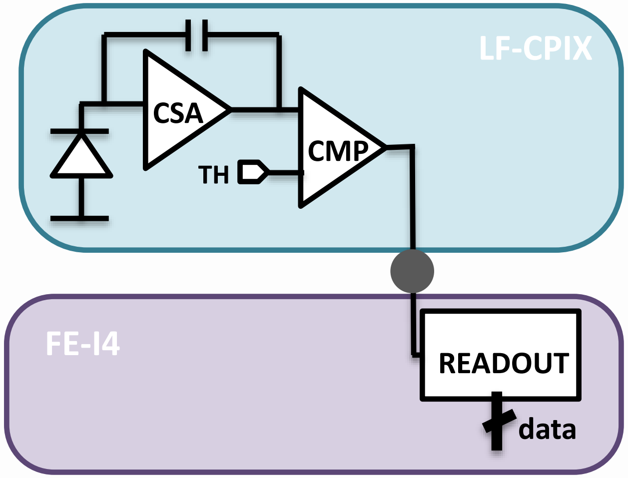


Normal (L=0.9um)
Long (L=1.5um)
Enclosed Layout (ELT)

T. Hirono (Bonn)

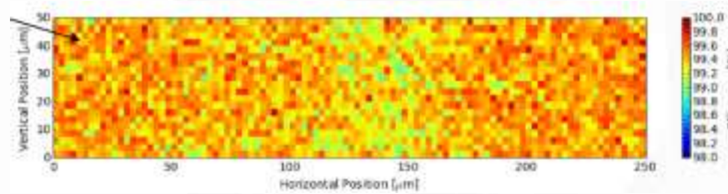
LF-CPIX

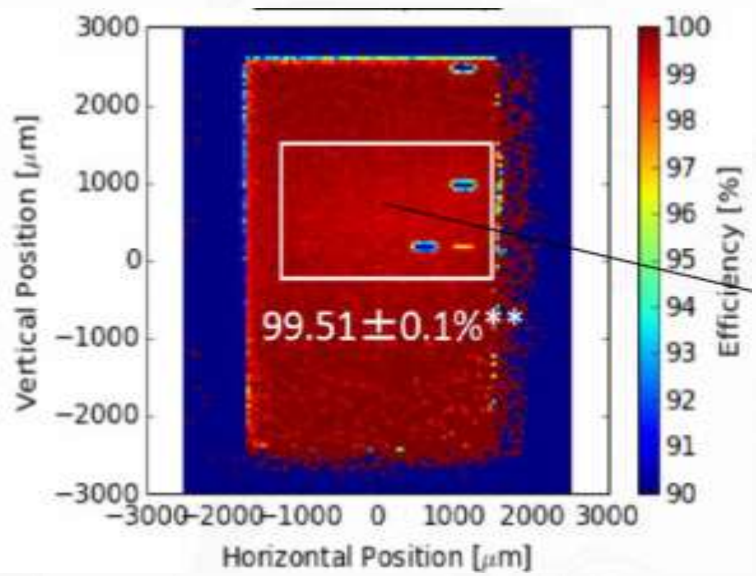




Efficiency pre-rad:

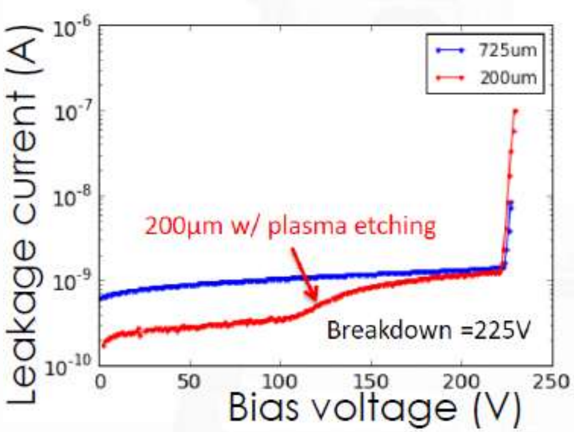
200um HV : -200V Threshold: 2750 e
Independedt readout





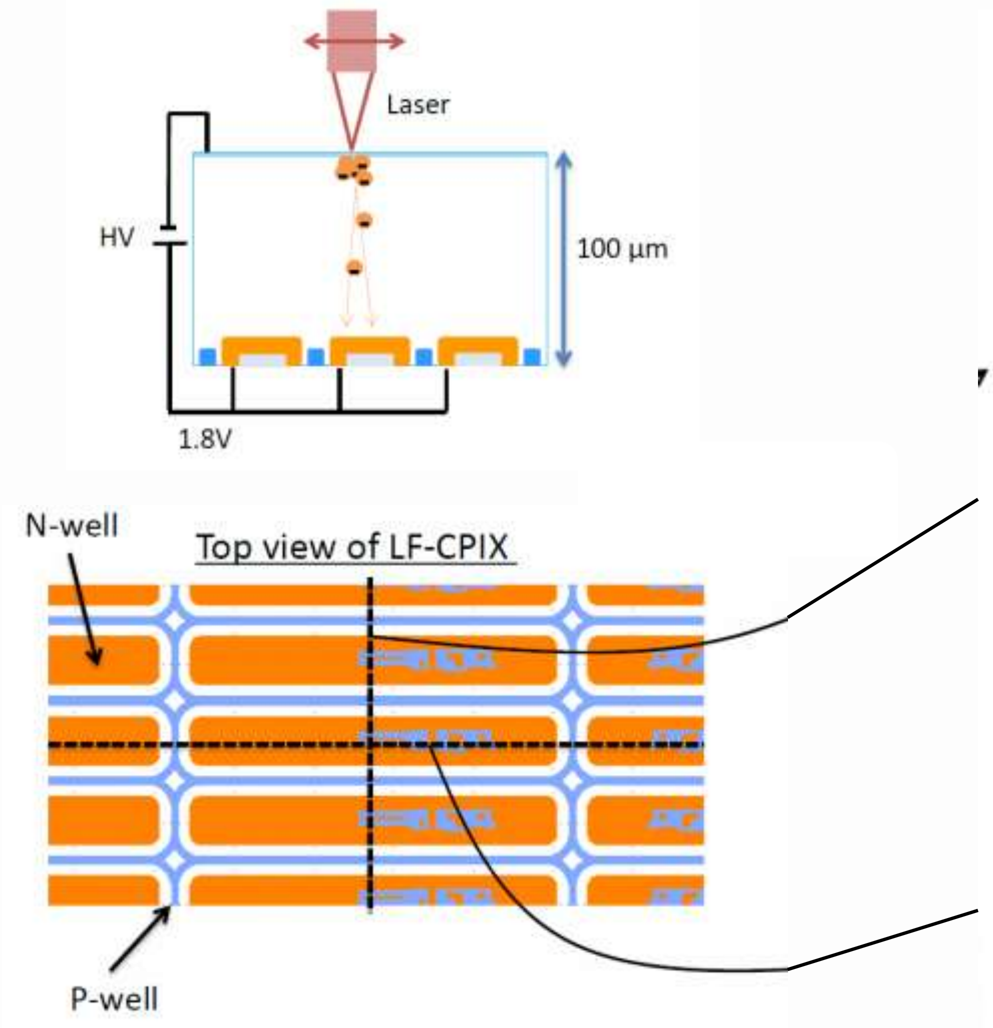
- **Hybrind (FE-I4)**
- **Independedt readout**
- **Pixel: 250x50um**
- **Fully functional**
- **Back processed to 100/200um**

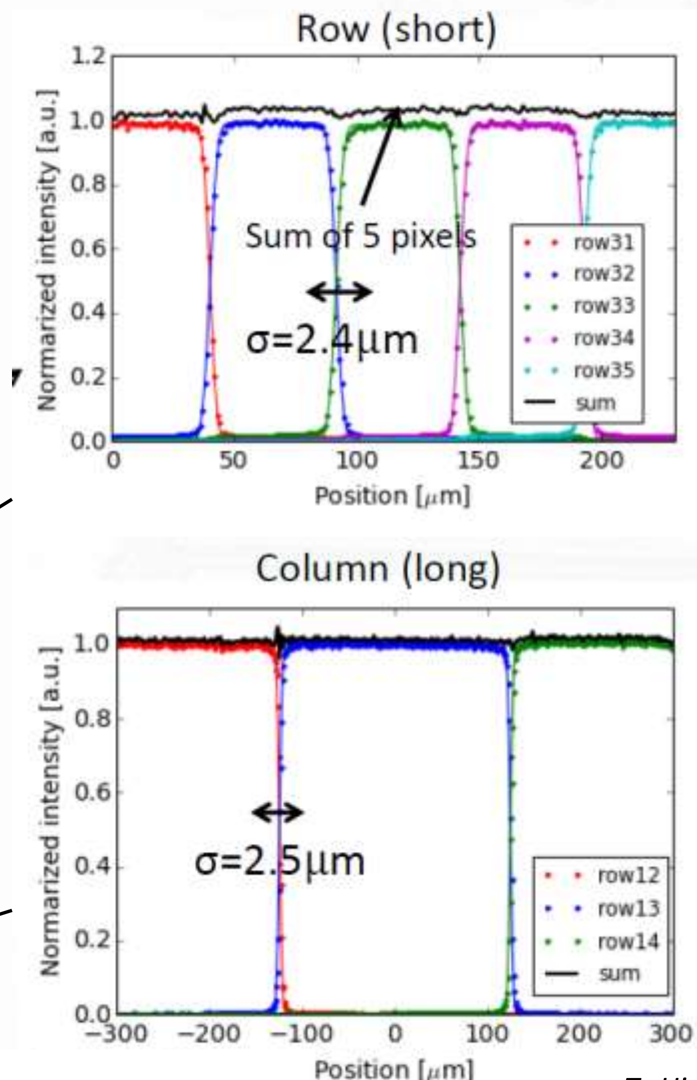
IV:



T. Hirono (Bonn)

LF-CPIX

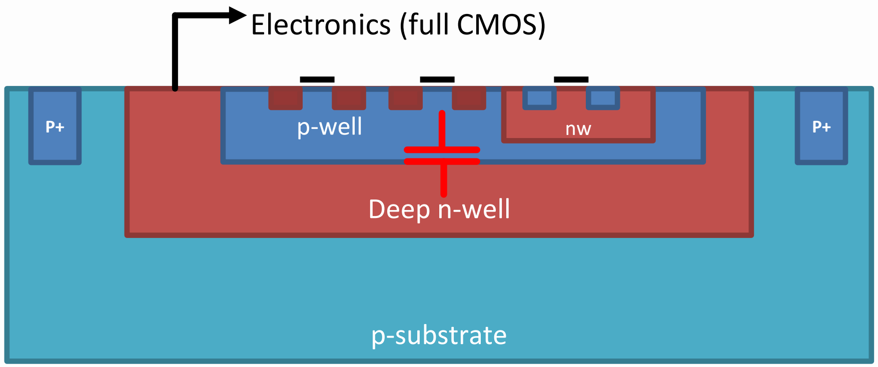


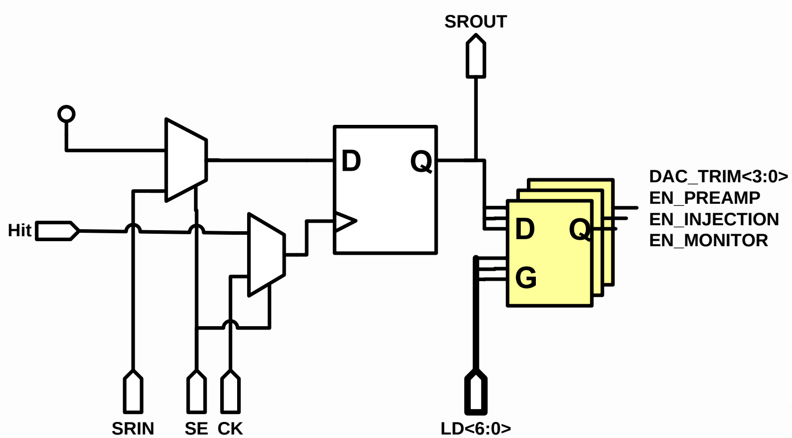


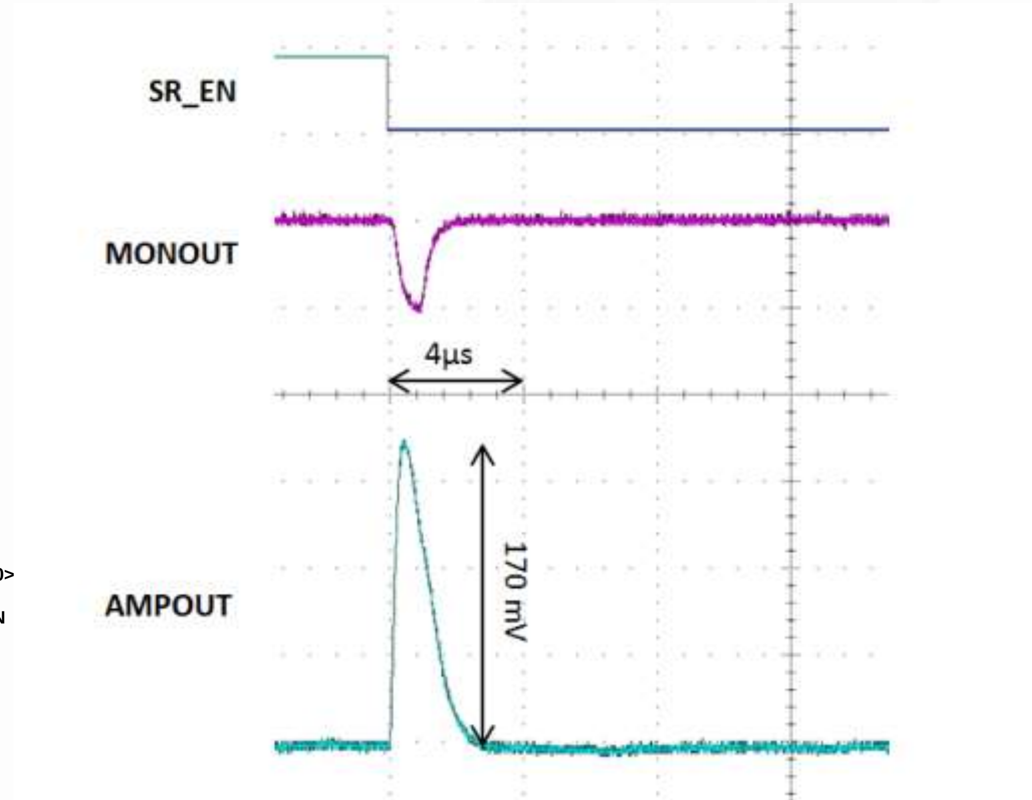
T. Hirono (Bonn)

Noise issue

Charge signal

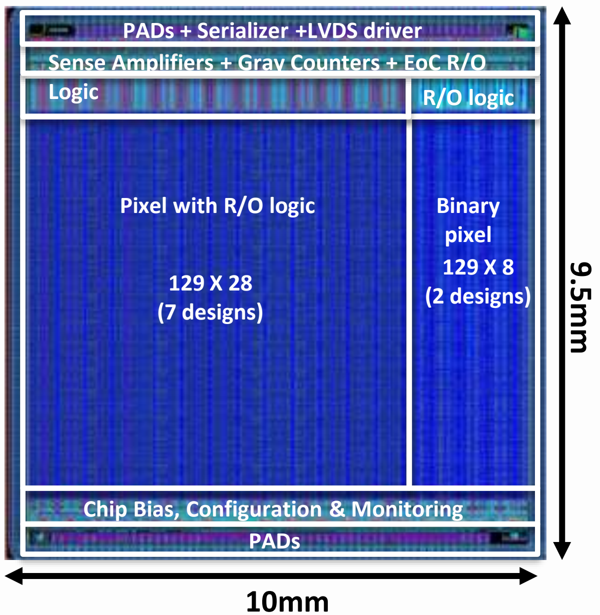


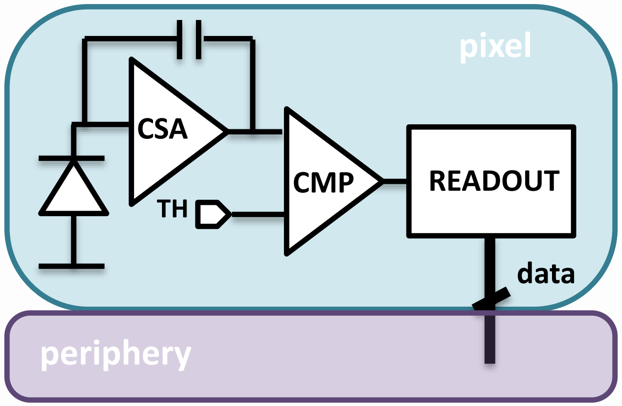


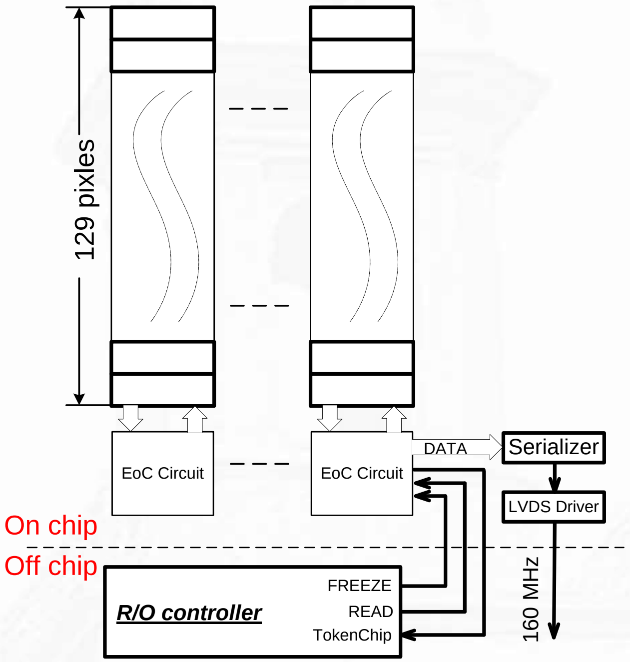


+ extra 200-400fF (50x250um^2)

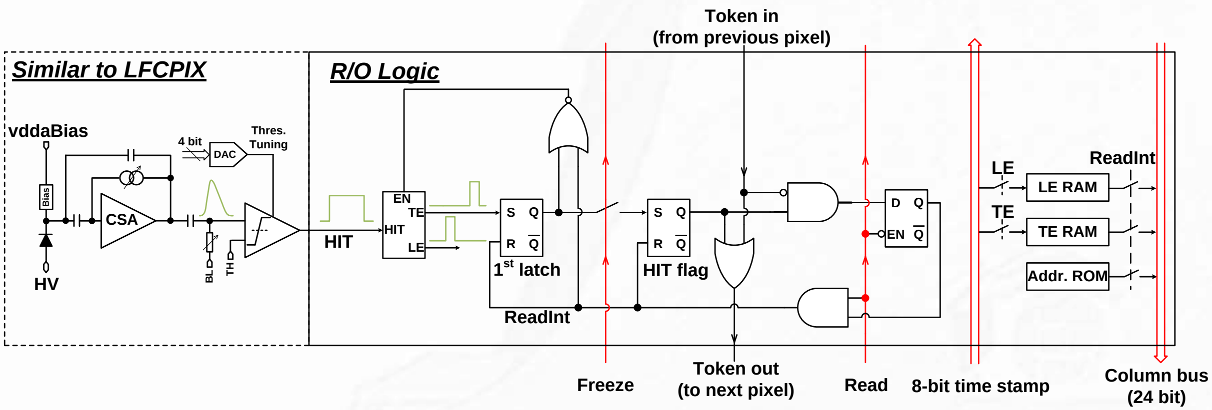
LF-Monopix





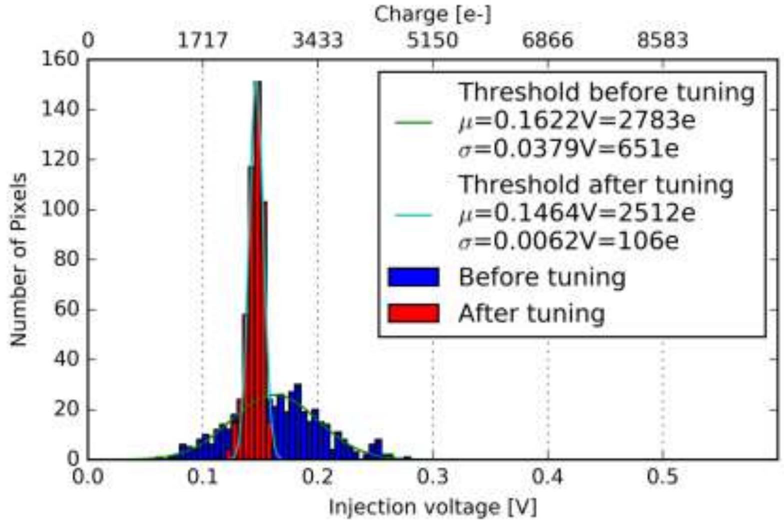


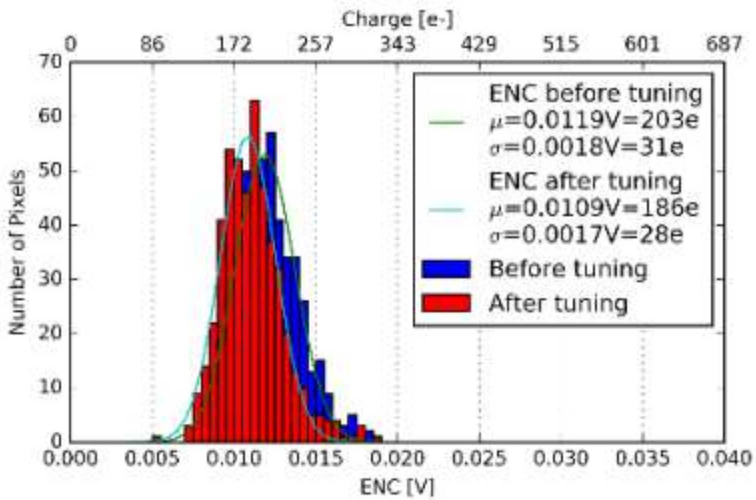
- Fully monolithic
- Different readout configurations
- Low noise design
- High resistive substrate (> 2k Ohm-cm)
- Fully functional
- Measurement campaign ongoing
- To be back processed to 100/200um



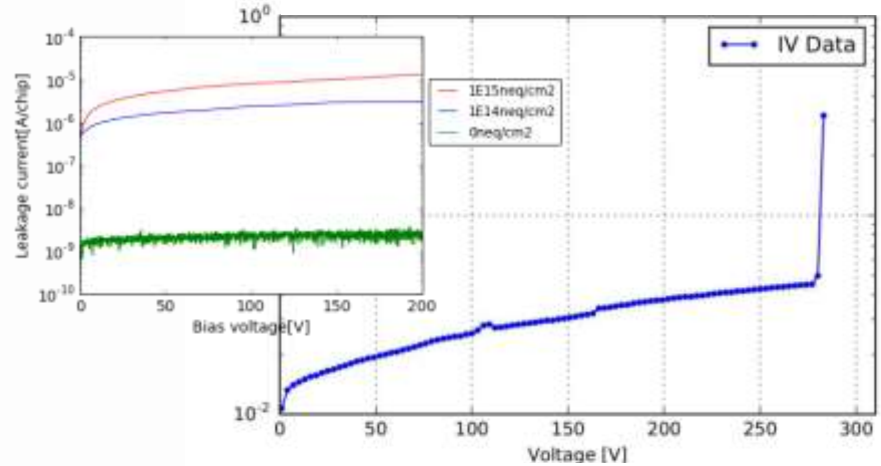
LF-Monopix

Tuning

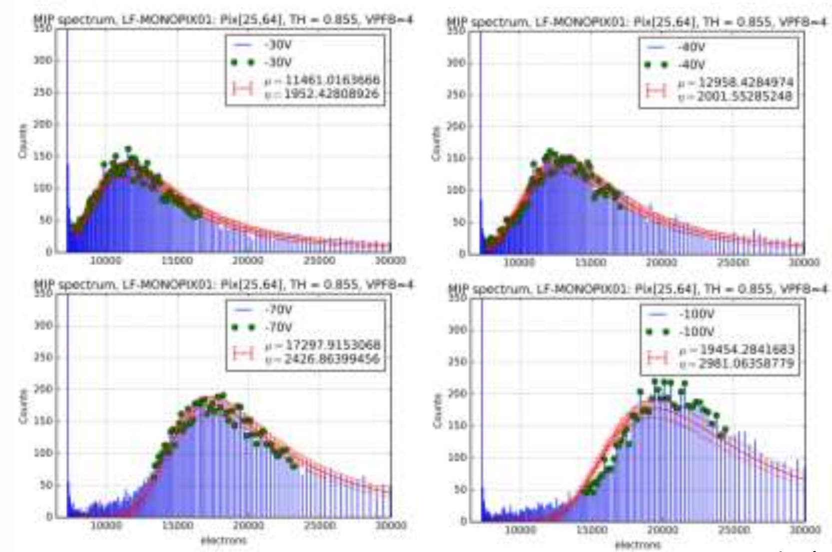




IV

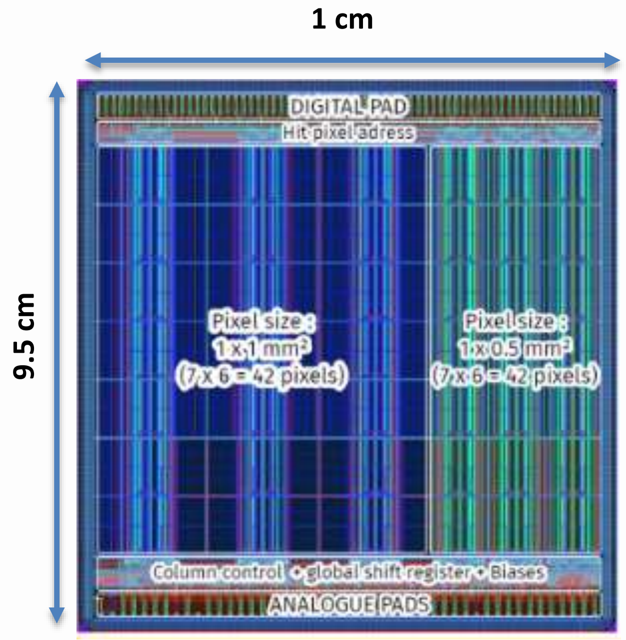


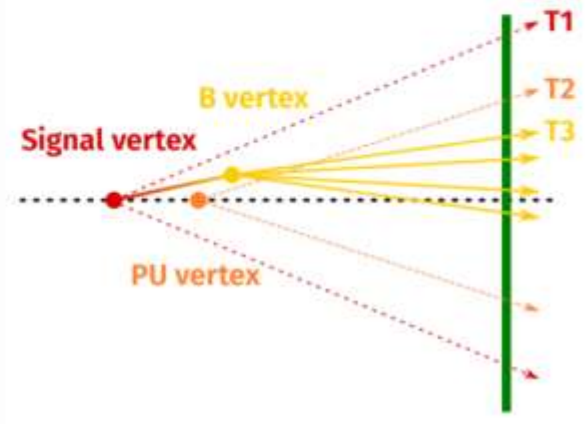
MIP single pixel spectra



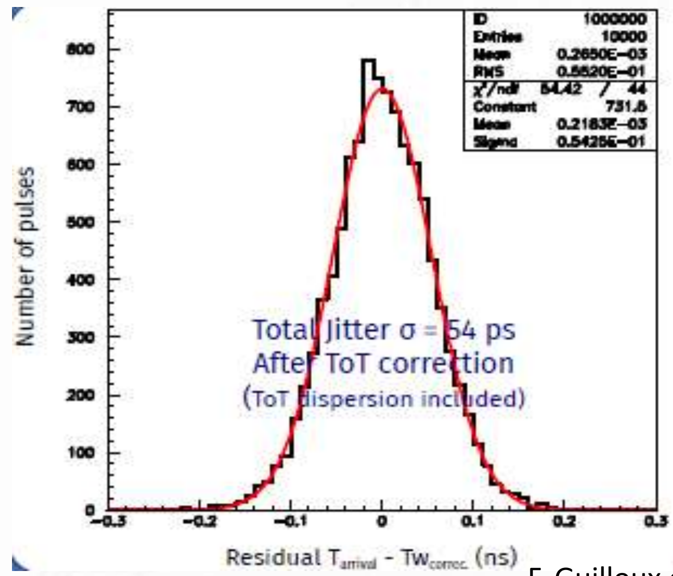
I. Caicedo (Bonn)

LF 150 time tagging - CAcTµS





Simulated timing (including sensor and readout:

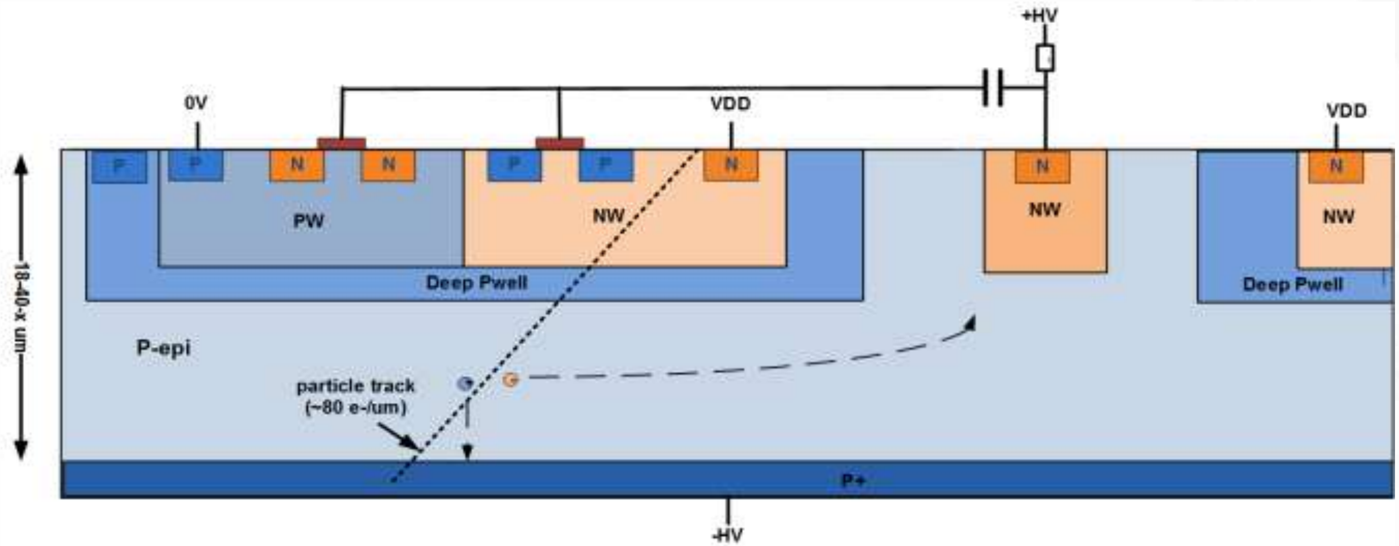


F. Guilloux et al. TWEPP 2017

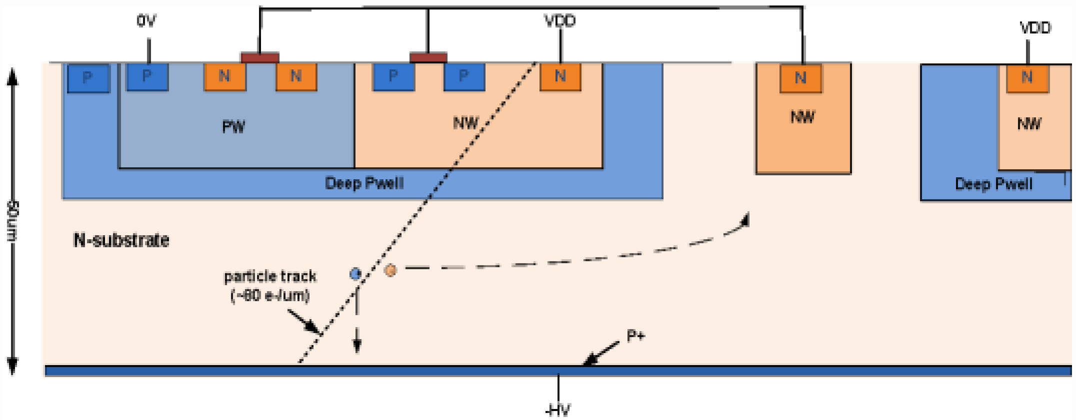
CAcTµS :

- L-Foundry 150 nm process
- 1x1 and 1x0.5mm^2
- Expected timing resolution < 100ps
- 100/50um thin
- Design: IRFU

Logic outside collecting well

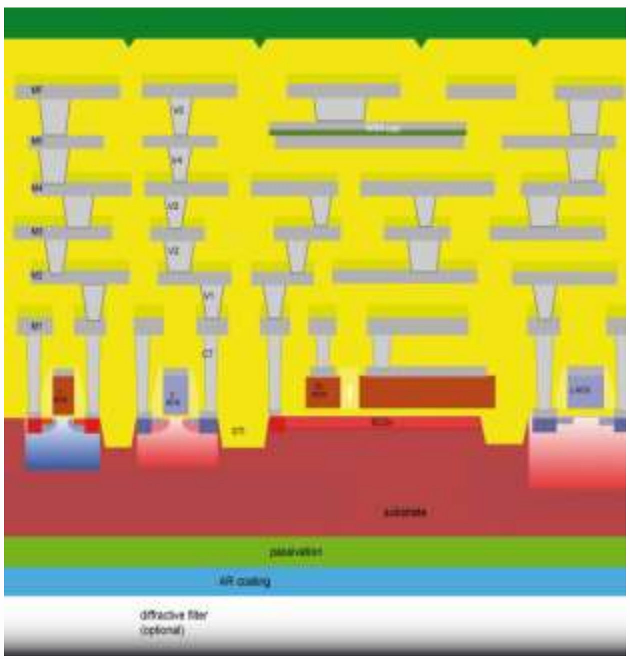


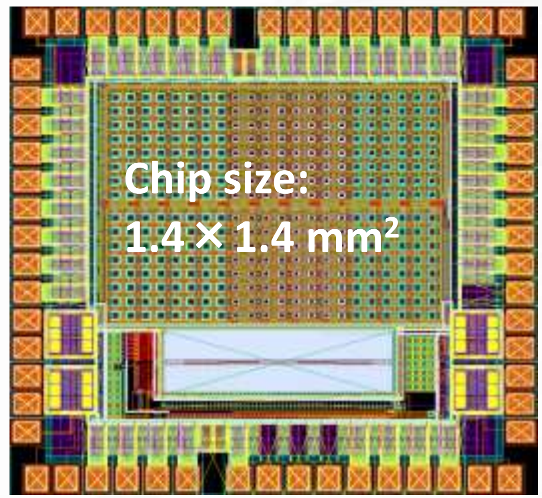
ESPROS Photonic CMOS™



OHC15L

- 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer (n-type): >2000 Ω·cm
- Backside processing
- **50um thin**
- Design: Bonn, Prag*

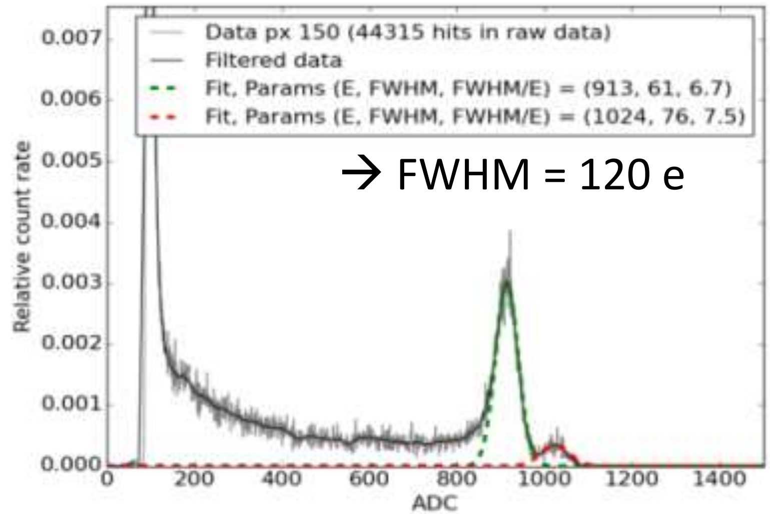




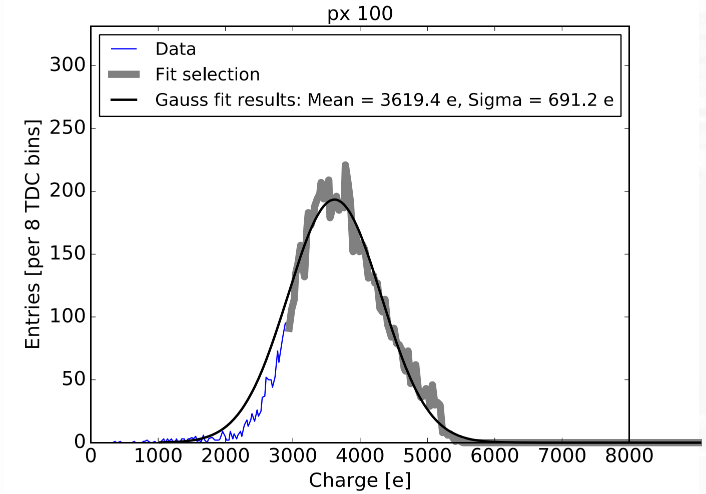
M. Havránek et al. JINST 10 (2015) 02, P02013

EPCB01

Fe^{55} spectrum

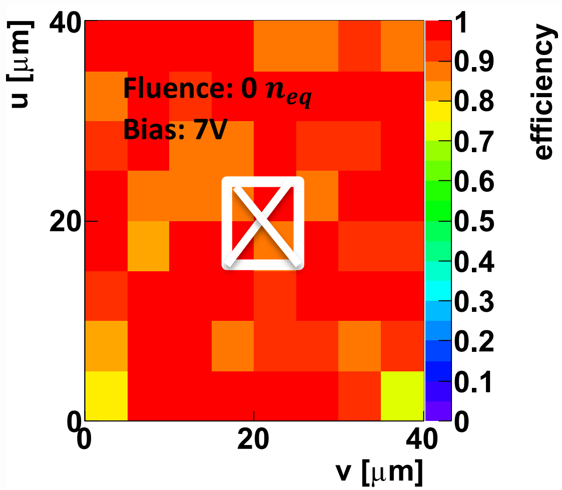


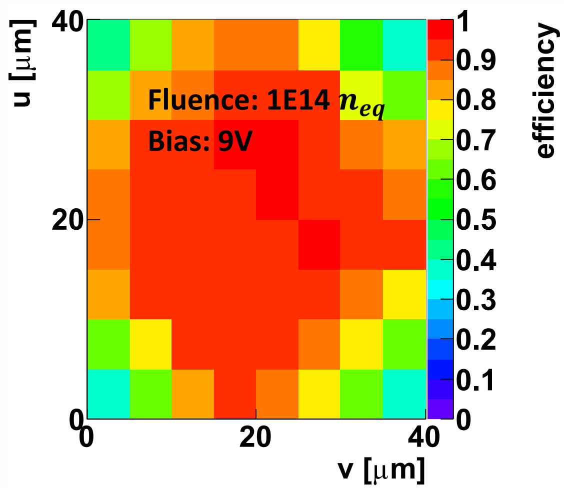
Calibrated single hit cluster spectrum Sr^{90}:

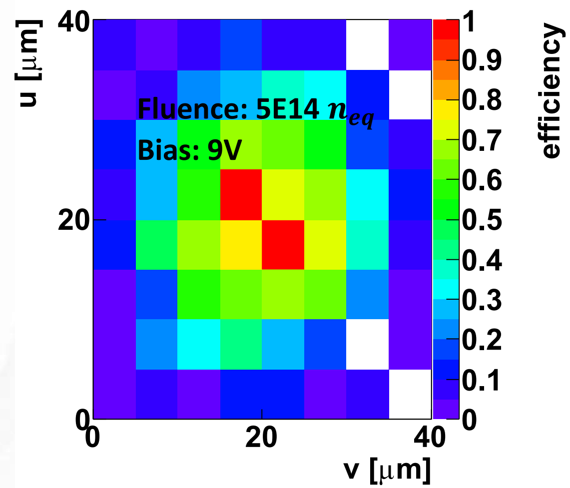


In pixel efficiency

T. Obermann (Bonn)



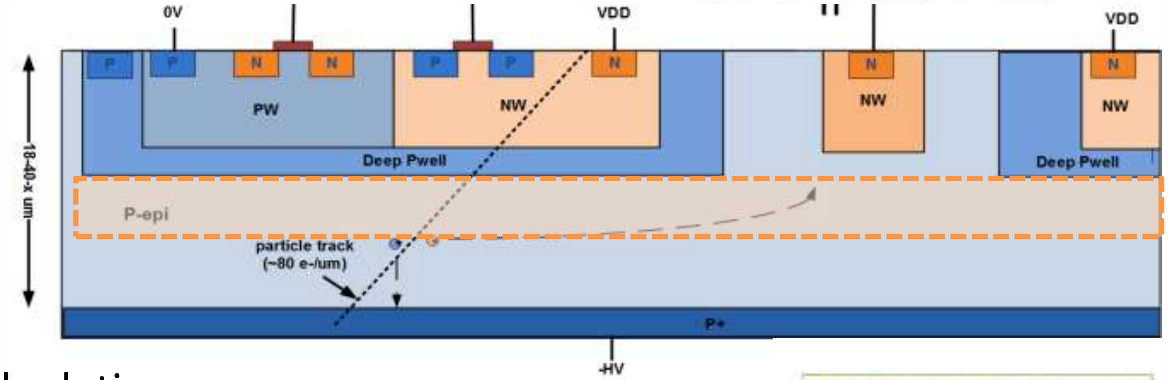


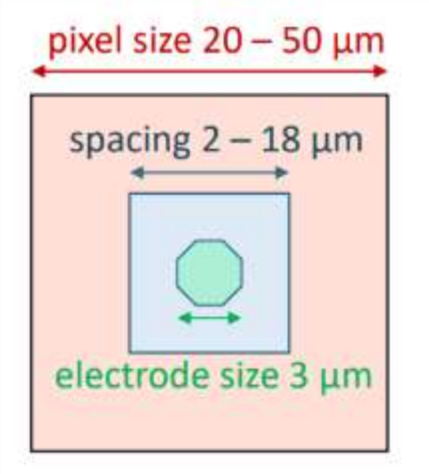


geometry, threshold ....

TowerJazz

- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN)





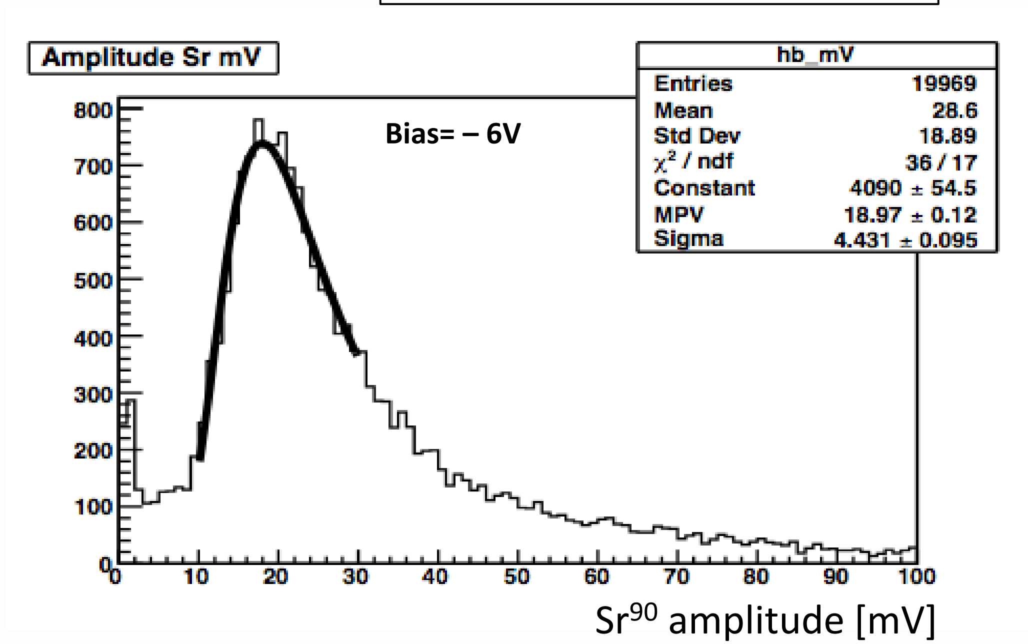
Pixel dimensions:

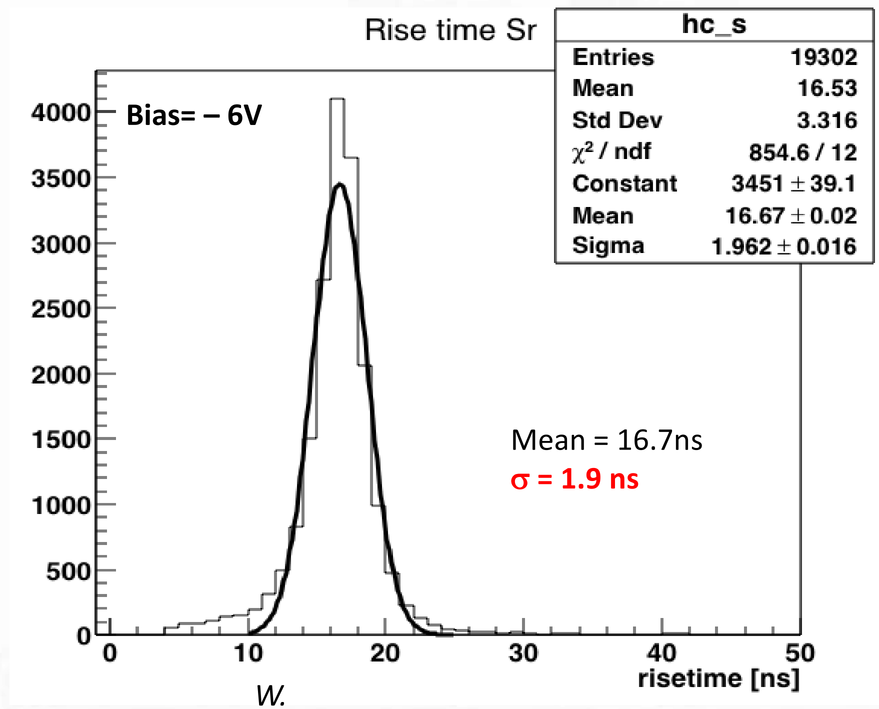
- 50x50um pixel size
- **3 µm diameter electrodes** and 40um Pwell openin
- 25um EPI layer
- **The pixels have a measured capacitance <5fF** (approximately factor 20 less than large fill-factor pixel) C. Gao et al., NIM A (2016) 831
- With this low capacitance, simulations indicate a front end similar to the one in the ALPIDE but compatible with 25 ns timing would consume ~ 200 nA)

Signal collection for small electrodes

- Normally small electrodes produce weak fields under p-well and charge gets lost after irradiation
- This usually means that efficiency drops significantly towards pixel edges
- **TJ modified its process to improve the efficiency after irradiation on pixel edges while keeping small capacitance** which makes this in particularly interesting for fast charge collection after irradiation
  - Pixel capacitance without process modification ~ 2-3fF with modification <5fC

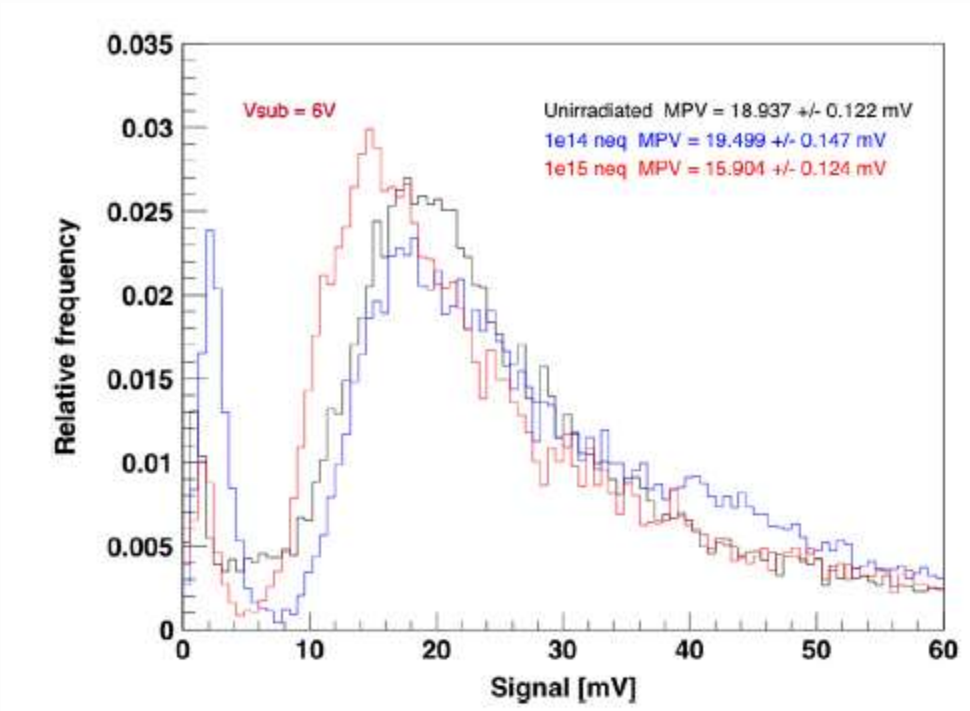
Modified process



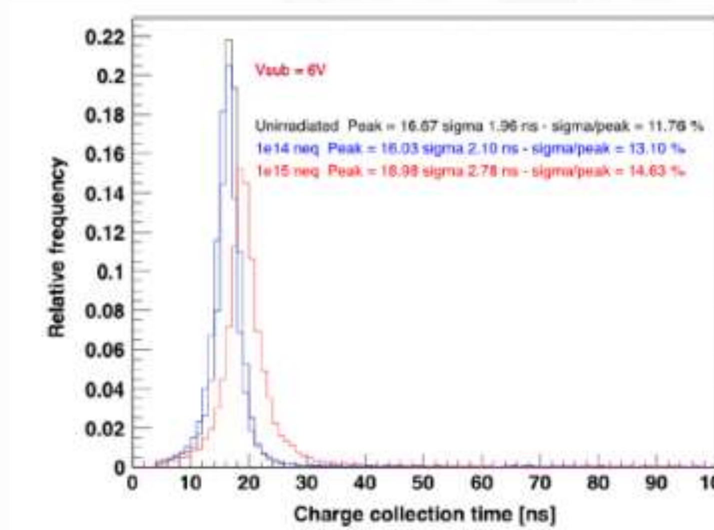


Neutron irradiation to 10^{14} and 10^{15} n/cm^2

- Investigator irradiated by IJS Ljubljana in several steps up to 10^{15}
- Irradiations up to 10^{16} ongoing
- This detector has received NIEL 10^{15} n/cm^2 and 1Mrad TID
- First test beam measurements indicate no efficiency loss on pixel boundaries after 10^{15} n_{eq}



^{55}Fe source

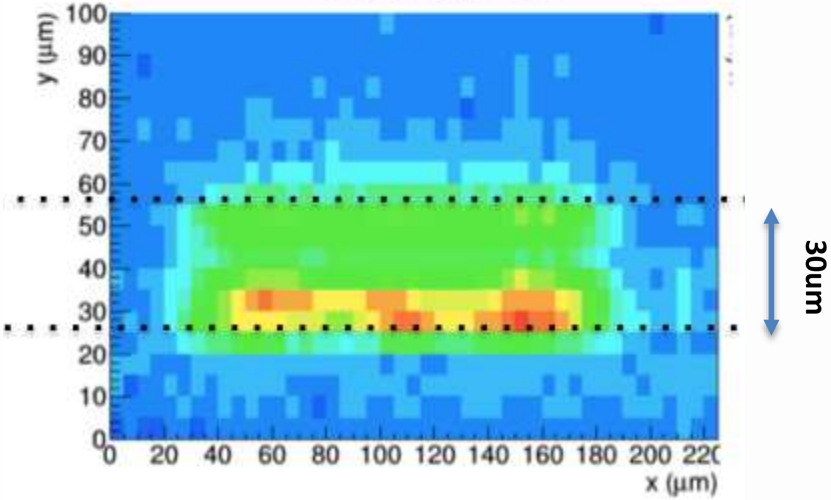


little change to signal (and capacitance !) after irradiation, -1 V is sufficient to observe a clear signal

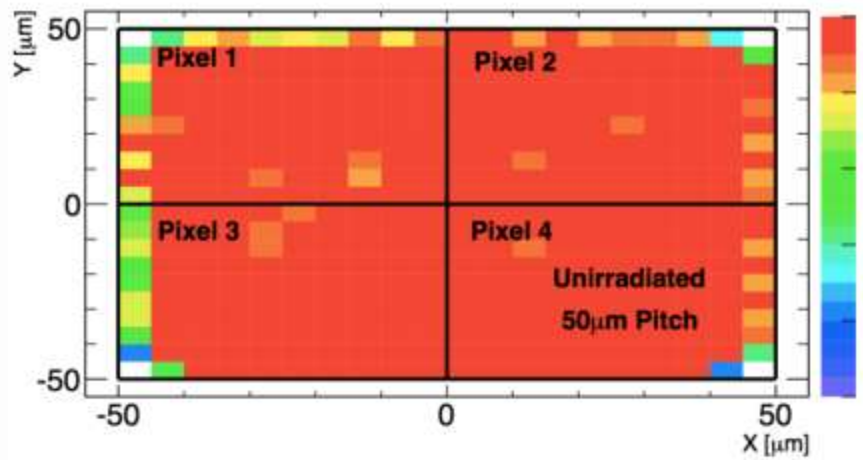
W.Snoeys et al., NIM 871, 2017

TJ - Investigator

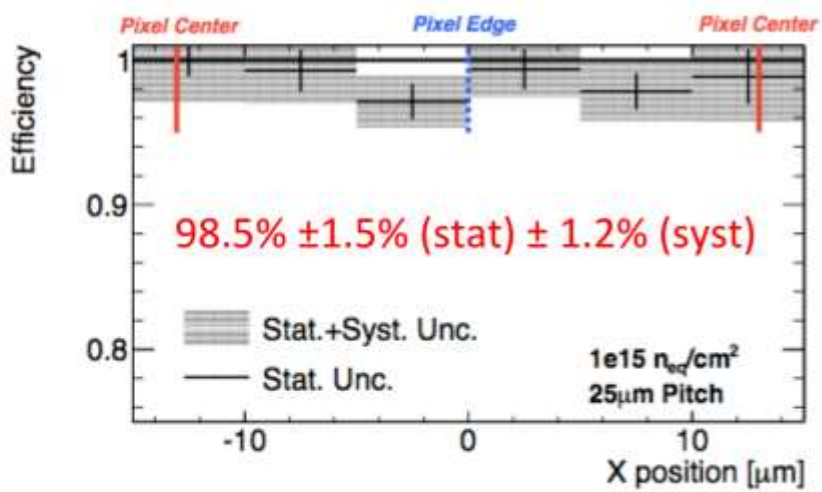
Edge-TCT for $10^{15} n_{eq}/cm^2$ @ 6V bias

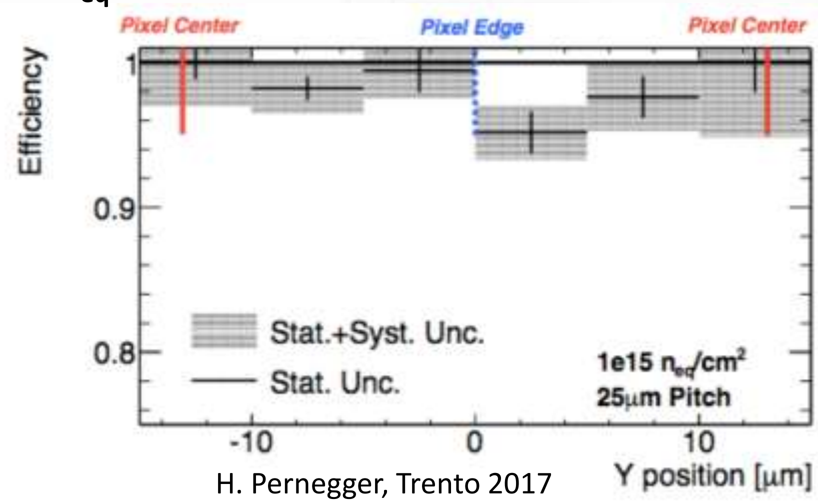


Efficency for 50x50um^2 pre-rad



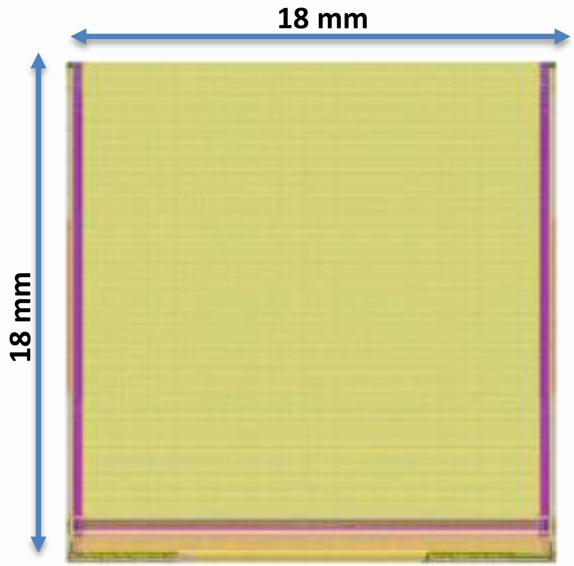
Efficency for 25x25um^2 $10^{15} n_{eq}/cm^2$ @ 6V bias

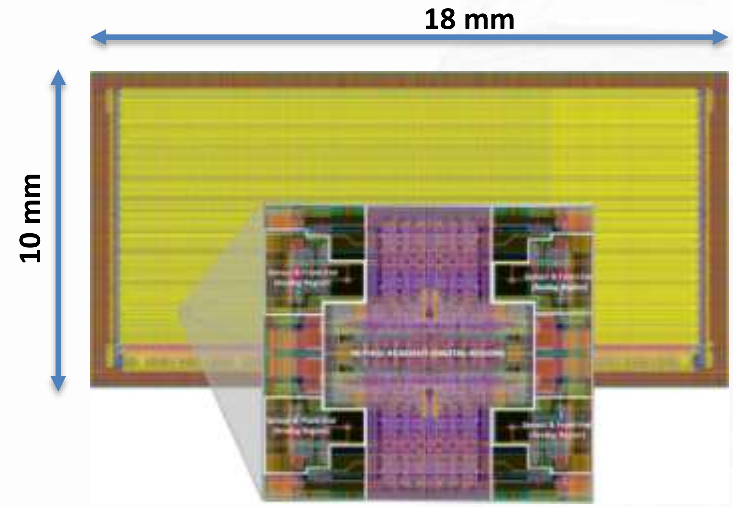




H. Pernegger, Trento 2017

TJ-MALTA/TJ-MonoPix





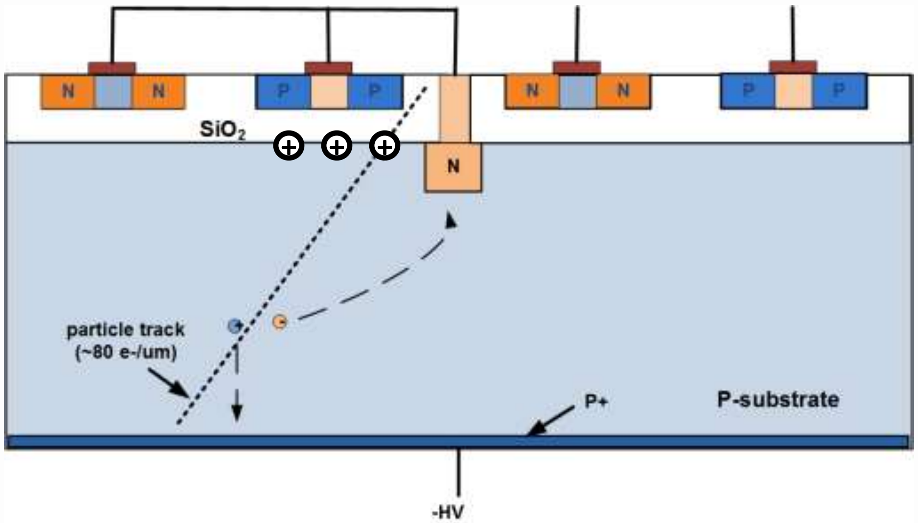
TJ-MALTA
- 512x512 pixels (**36.4 x 36.4** µm² pixel size)
- Design: CERN
- Active area 18 x 18 mm²
- Hit memory in active matrix
- All hits are asynchronously transmitted to EoC logic
- No clock distribution over active matrix

TJ-MonoPix
- **512x256** pixels (**36.4 x 36.4** µm² pixel size)
- Design: Bonn
- Active area 18 x 10 mm²
- Hit memory in active matrix (2 flip-flop per pixel)
- Synchronous column drain architecture
- Hit address asserted to bus with 40 MHz token
- 6 bit ToT coding at end of column

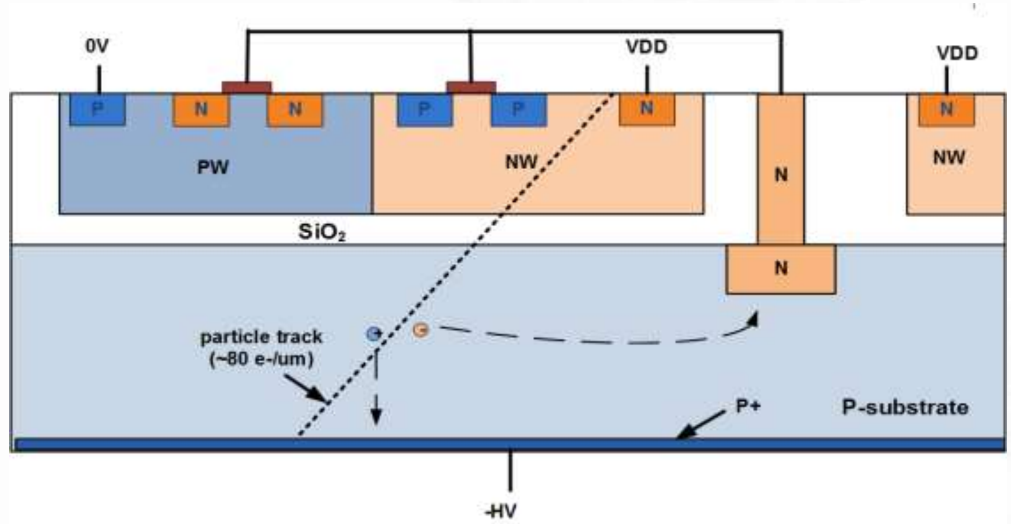
Just submitted

SOI

FD-SOI

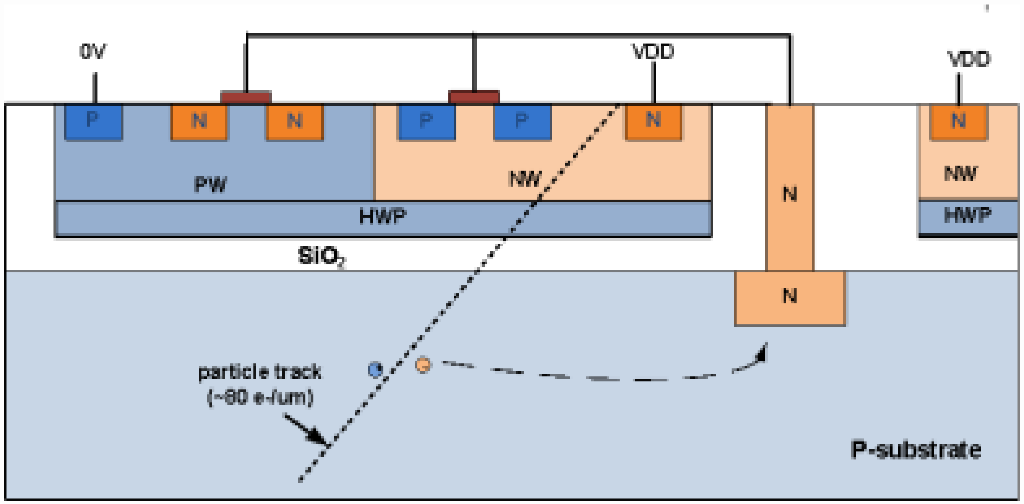


HV-SOI



see: S. Bugiel, “The performance …”
A. Takeda, ”Design and Development …”
R. Hashimoto, “Evaluation of”

XFAB XT180

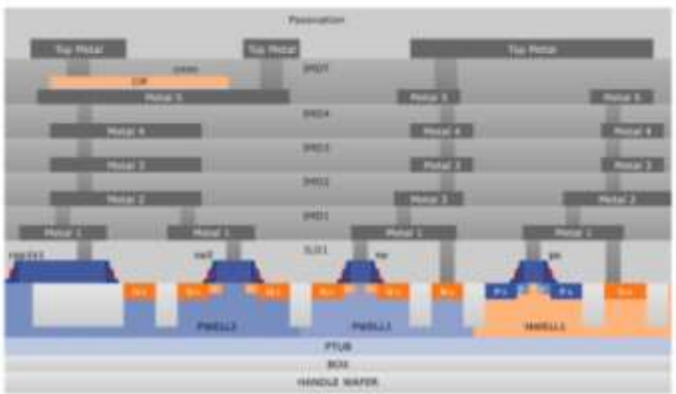


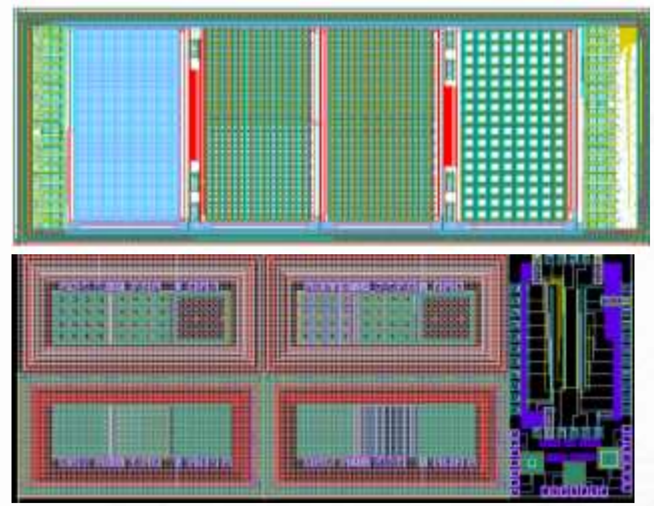
XT180:

- XFab 180 nm HV-SOI
- Up to 7 metal layers
- Resistivity of wafer: 100 Ω·cm

XTB01 and XT02 prototypes:

- Pixel pitch: 15, 50, 100um
- Chip size: 2.5 mm x 5 mm
- Design/Testing: Bonn, CERN, CPPM

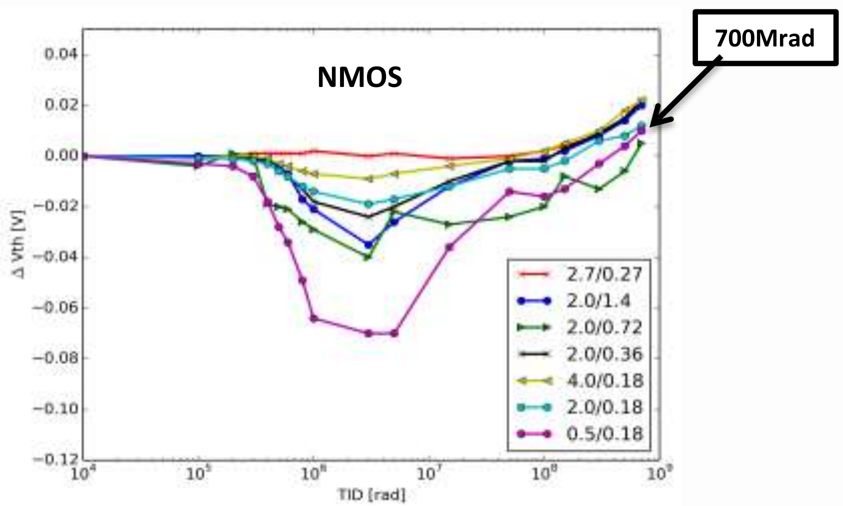


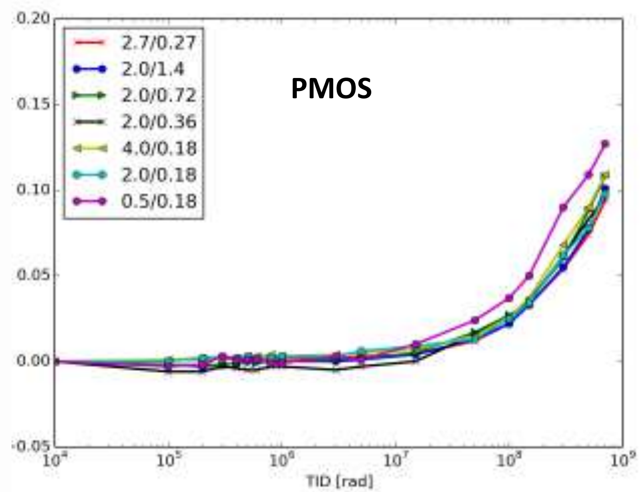


Sonia Fernandez-Perez et al. NIM A796 (2015) 13-18
Hemperek et al. JINST 10 (2015) no.03, C03047

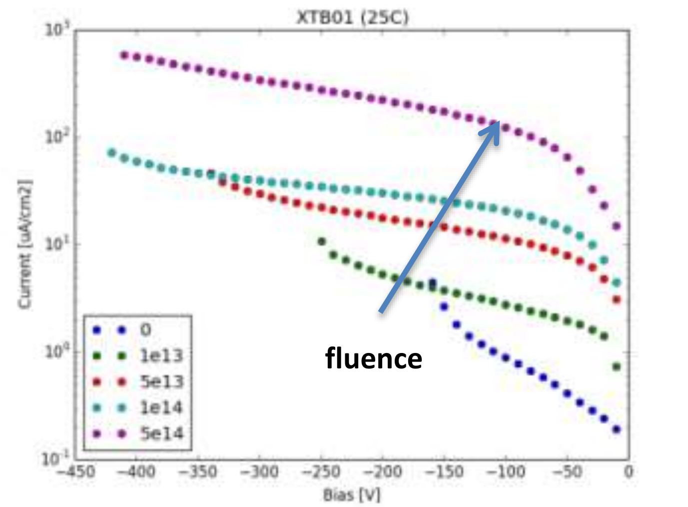
HV-SOI

Transistors threshold shift (TID)

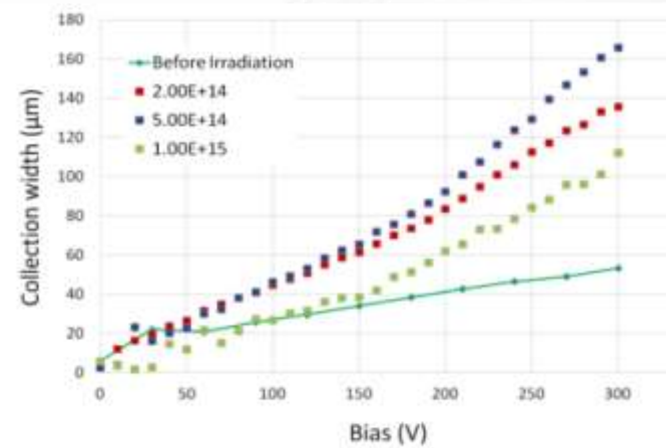




Leakage current (v1)



Collection with (edge-TCT) (v2)



Conclusions

- Lots of encouraging results (high interest and large momentum in R&D)
- Proven good radiation tolerance of sensors (and electronics)
- Lower cost alternative to conventional hybrid sensors (as monolithic or cheaper hybrid)
- Limited complexity (150-180nm)
- Successful backside processing 200/100um (50um possible)
- Possible higher resolution and lower mass (in low capacitance design)
- Proposed for ALTAS outer pixel layer Phase 2 (option)

- Coupling smart sensor and R/O chip can increase performance of hybrid sensors

CMOS Pixel Collaboration

- ~20 ATLAS ITK institutions