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Recent Developments of SOI Pixel Devices

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We are developing monolithic pixel devices utilizing Lapis 0.20um FD-SOI CMOS process. A couple of issues needed to solve in adopting SOI technology to pixel sensors for high-energy experiments, namely, back-gate effects, noise pick-up and total ionization dose (TID) damage, have been successfully overcome ultimately by use of double-SOI wafers. The application of SOI technology has been boosted recently through five-year fund of Grant-in-Aid for Scientific on Innovative Area Research. Major achievements in this development activities will be covered, including FPIX test beam results, achieving a spatial resolution as small as 0.7um, and and SOFIST development of the ILC. The FPIX has shown TID tolerance up to 1 MGy of irradiation.

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