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# Main Results of Radiation Characterization of CMOS 65nm technology and the impact on the design of RD53A, a large scale pixel chip prototype for HL_LHC.

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The results of several years of radiation characterization of the CMOS 65nm technology at both transistor level and circuit level will be summarized here.The degradation of the performance of 65 nm MOSFETs upon radiation exposure was studied using 10-keV X-rays, but also using 3-MeV protons. Models that parameterize the effect of total dose on MOS performance have been defined according to the measurements made, in particular for 200 and 500 Mrad.
The analog circuitry and building blocks designed in the framework of RD53 collaboration have been made radiation hard by design following few prescriptions and using the irradiation models. A chip has been designed to study the effect of TID on several different types of standard cell libraries provided by the foundry (Digital-RAD, DRAD chip). In particular ring oscillators have been designed in different flavors, so to measure how much the digital transitions are slowed down by irradiation.
The design of the RD53A, a large scale prototype of a new generation pixel ASIC, takes into account the radiation characterization of the CMOS 65nm technology and it is meant to demonstrate the capability to make pixel chips that can sustain and survive the extremely challenging operating conditions determined by HL_LHC in the inner layers of the experiments.

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