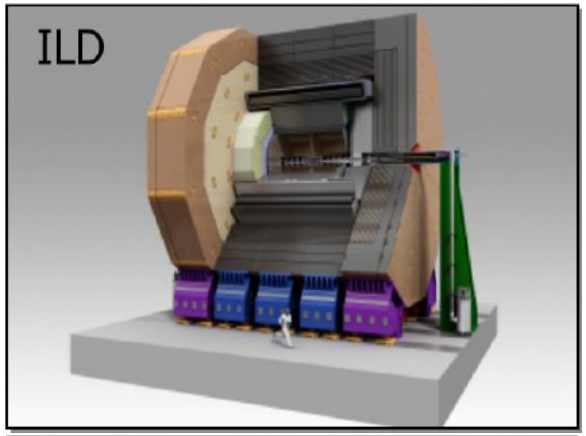
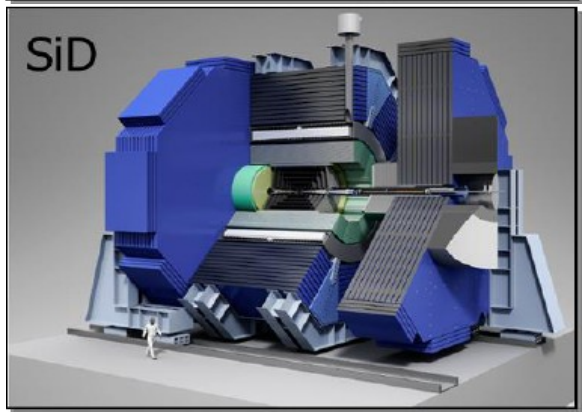
VERTEX/2017

10-15 September 2017

ILC Vertex Detectors & Silicon Trackers





Alejandro Pérez Pérez

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On behalf of the ILD and SiD detectors R&D groups

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IPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

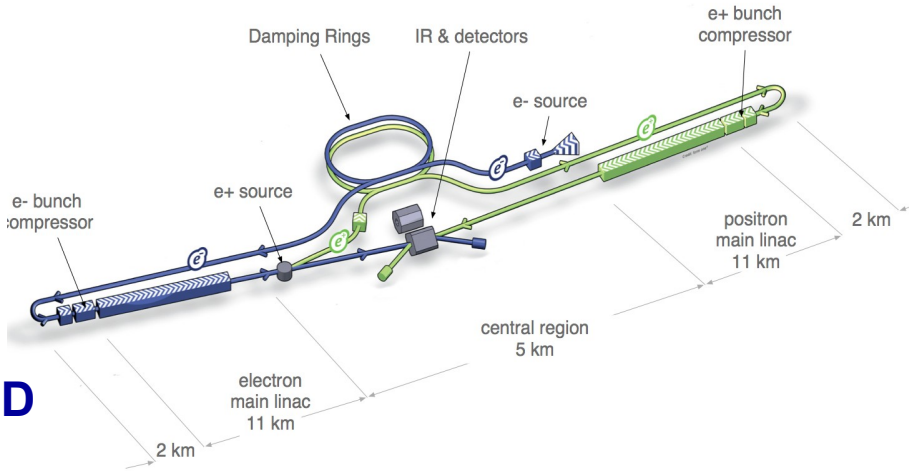
PICSEL GROUP

Outline

- The International Linear Collider
- ILC Detector Challenges
- Current vertex detector & tracking systems design
- R&D efforts
- Summary and Outlook

The International Linear Collider (ILC)

- **e^+e^- Linear Collider 31 km long with baseline $\sqrt{s}$ = 500 GeV**
  - Phases @ 250 & 350 GeV
  - Possible Upgrade @ 1TeV
- **Baseline beam parameters**
  - $2x10^{10}$ parts/bunch spaced by 554 ns
  - Polarization 80/30 for e-/e+
  - $L = 1.8x10^{34}$ $cm^{-2}s^{-1}$
- **2 Detectors in "push and pull": ILD & SiD**

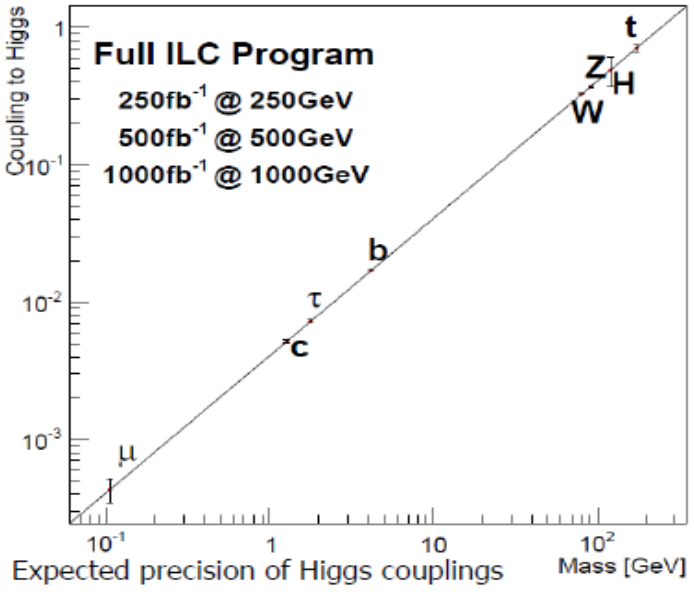


- **Brief history, Current Status & prospects**
  - **2012:** TDR and Detailed Baseline Design (DBD)
  - **Fall 2015:** High-ranking US-Japan Talk starts
  - **May 2016:** KEK Management "Japanese Decision on ILC will be Input to the European Strategy"
  - **Dec. 2016:** E-XFEL goes online
  - **2017:** Staging discussion ⇒ start @ 250 GeV to reduce cost?
  - Green Light ⇒ International Laboratorys

ILC Key Features & Physics Goals

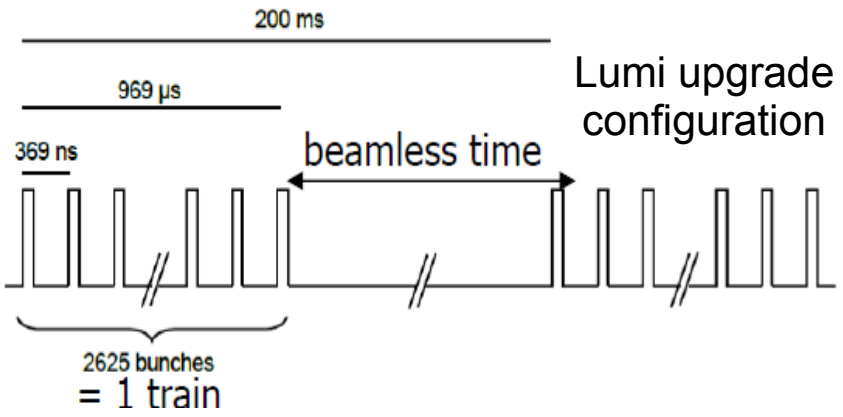
- **Key features**
  - Well known initial state, no QCD background, fully reconstructible channels
  - Precise theoretical predictions: radiation corrections O(1%) & theoretical error O(0.1%)
  - Tunable √s (threshold scan & flexibility) & Beam polarization (S/N enhancement)
  - Globally small cross-section but highly pure samples
  - **Advantages:** triggerless, low backgrounds, most measurement statistically limited
- **Very rich physics program**
  - Higgs sector
    - O(1%) precision of mass/width/spin & couplings
    - Model independent measurements (σ & σ×Br)

      ⇒ Probe BSM, model disentangling
  - Top physics
  - EW precision measurements
  - Direct/indirect BSM searches
- **Very important role of Vertex detector**
  - Favour tagging (b, c, τ)
  - Low momentum tracking (as lows as 200 MeV/c)
  - Jet charge determination



ILC Experimental Environment

- **Beam structure**
  - 5 trains/s of ~1300/2600 bunches
  - 1 bunch every 550/370 ns
  - Beam-less time ~ 200 ms
  - Operation strategies
    - Full detector readout (r.o.) ⇒ triggerless
    - Possible r.o. during beam-less time
    - Power pulsing ⇒ reduced power



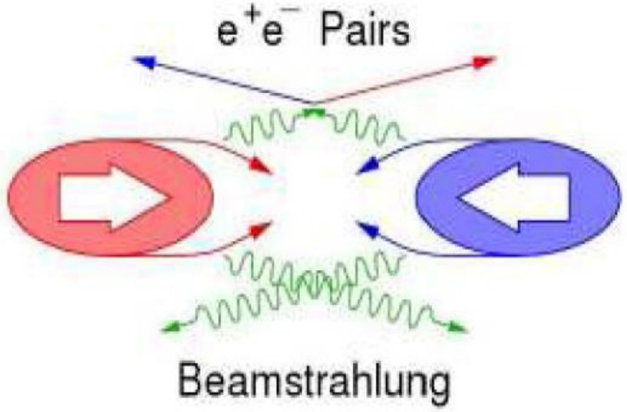
Lumi upgrade configuration

- **Beam induced bkg: Beamstrahlung**
  - Beam energy loss: ~1% @ 250 GeV
  - Radiation level: ~100kRad ⊕ 10^{11} n_{eq}/cm^2

    (HL-LHC: ~1GRad ⊕ 10^{16} n_{eq}/cm^2)
  - Low momentum (10 – 100 MeV/c) real tracks!
  - Main occupancy source: drives VTX r.o. speed & R_{min}
  - Typical rate of ~ 6 hits/cm^2/BX on innermost VTX layer
  - Large systematic uncertainty

    ⇒ Safety factor of at least x5 needed

Bunches have electric space charge
⇨ particles deflected
⇨ photons emissions
⇨ e^+e^- pairs ("beamstrahlung")



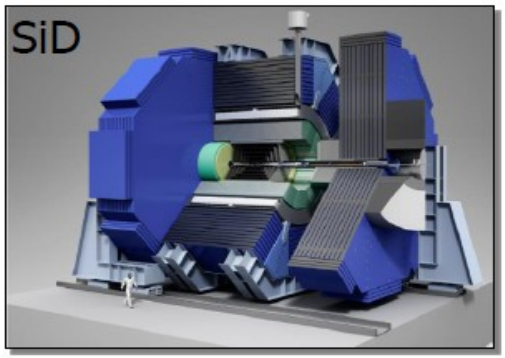
ILC Detector Challenges

- **Detector design driven by running conditions and physics goals**
  - **Strategy:** use of particle flow algorithms used to an unprecedented level

- **For this need an unprecedented precision detectors**
  - **Jet σ_E**
    - factor of 3 improvement on jet σ_E w.r.t. LHC (~200 higher calorimeter granularity)
  - **Tracking and Vertexing**
    - Momentum resolution factor of 10 w.r.t. LHC
    - Track pointing to IP
    - Low momentum tracking ($p_T \lesssim 100$ MeV/c)
    - Enhanced flavour (b,c,τ) tagging: short lived particles flying O(100 μm)
    - All this achieved with 10-20 finer pixels and ~5-10 lower Mat. Budget w.r.t. LHC

- **Other performances much less demanding w.r.t. LHC**
  - Radiation hardness
  - Time resolution
  - Data rate

ILC Detector Design: 2 complementary approaches



Common approach

- Allow push pull
- Exploit fully Particle Flow Algorithms

Common features

- SiW EMcal & Hcal inside coil
- Muon detector
- Forward trackers
- Low mass vertex detectors

long barrel ← → shorter barrel with endcap disks

- Size
- Magnetic field
- Main tracker

Larger
optimizes PFA (particle separation)

3.5 Tesla

TPC
dE/dx
Large number of hits ⇨ pattern recognition

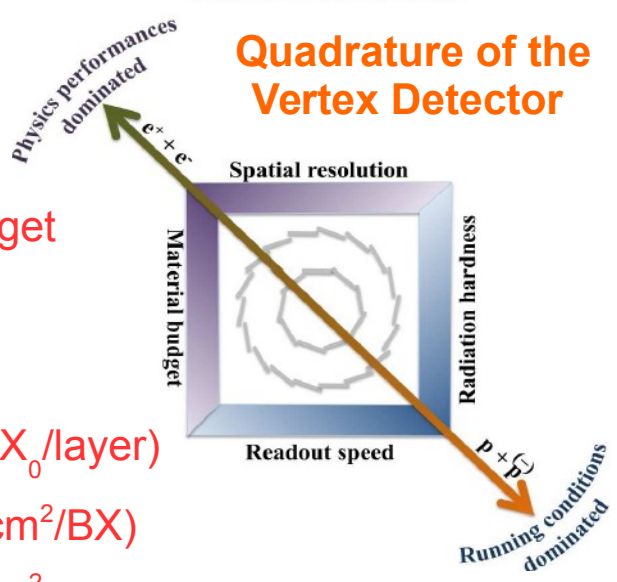
More compact

5 Tesla
optimizes vertex performances
compensates smaller size
more costs efficient

Silicon only
robustness, time stamping
few high precision points

ILC Vertex Detector (VTX) Requirements

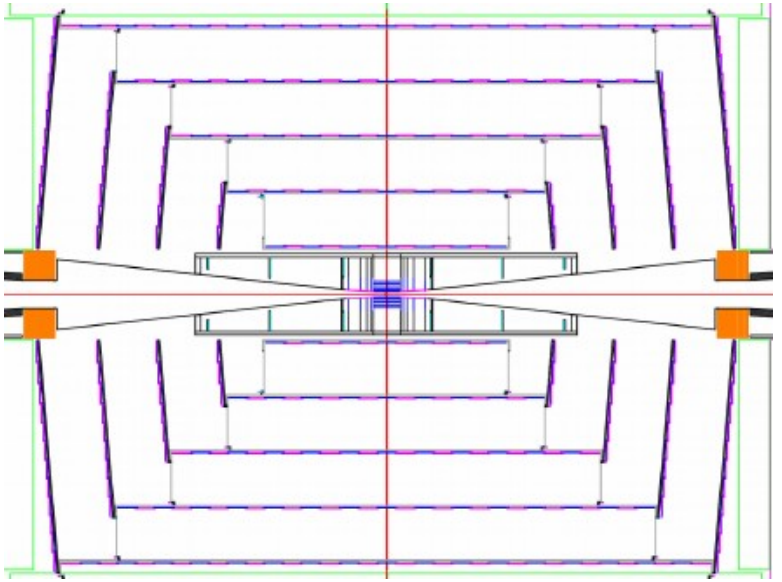
- **Linear e^+e^- collider**
  - Exhibit milder running conditions than pp/LHC
    - Relaxed readout-speed & radiation tolerance
  - Favours technologies focusing on resolution & material budget



- **VTX requirements**
  - Physics performances: $\sigma(d_0) < 5 \oplus 10/p\beta \sin^{3/2}\theta$ μm

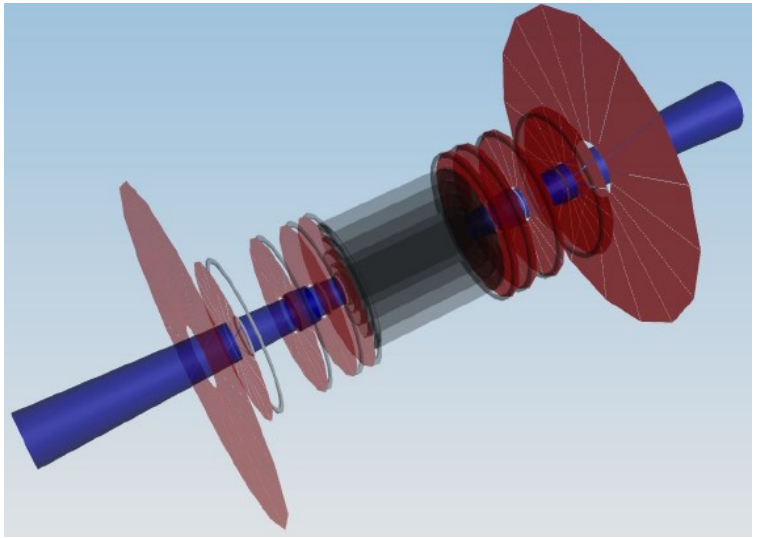
    $\Rightarrow \sigma_{sp}$ ~3 μm (~17 μm pitch) & low material budget (~0.15% X_0/layer)
  - Occupancy ⇔ readout-speed: few % occupancy (~6 hits/cm^2/BX)
  - Moderate radiation tolerance (/year): ~100kRad ⊕ 10^{11} n_{eq}/cm^2
  - Power dissipation ⇔ preferably air cooling: 600W/12W (power cycling, 3% duty cycle)
  - Readout & electronics
    - Immunity to SEU and Latchup
    - Highly integrated readout μ-circuits & high data transfer rate (triggerless)
  - Other parameters
    - Cost, fabrication reliability and flexibility
    - Mechanical integration: low mass, rigidity and heat conductive
    - Alignment: sub-micron level
- **Reach the specifications all together is the real challenge**

SiD: VTX and Silicon Strip tracker

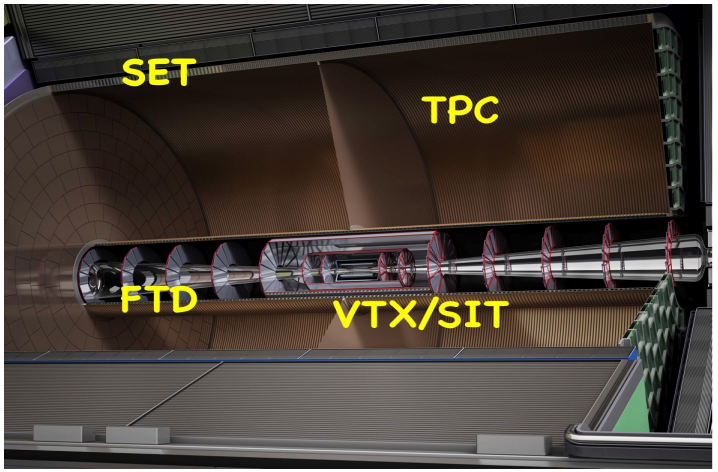


- **Silicon Strip Tracker**
  - All silicon tracker
  - Use silicon micro-strips and double metal layers
  - 5 barrel + 4 disks
  - Gas cooled
  - Material budget less than 20% X_0 in active area
  - Readout KPIX ASIC bump-bonded to modules

- **VTX**
  - 5 barrel pixel + 7 disks (4 close and 3 far away)
  - Baseline: pixel pitch 20×20 μm^2
  - **Technology options**
    - Monolithic CMOS chip ⇒ **Chronopix**
    - 3D vertically integrated silicon

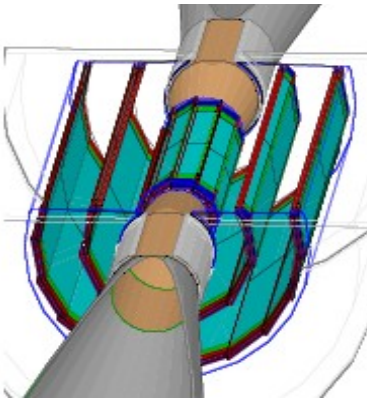


ILD: VTX and Silicon Tracking System

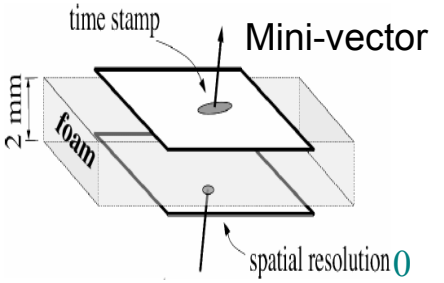


- **Silicon Inner & External Trackers (SIT & SET)**
  - Si-strip detectors: 200 μm thick, 50 μm pitch, 10×10 cm^2 sensors, edgeless, 7 μm σ_{sp}
  - Improves resolution and linking VTX-Tracker-Ecal

- **Fwd Tracker (FTD):** 7 disks (2 pixel & 5 Si-strips)
  - 2 closest layers: small pixels 20×20 μm^2 (σ_{sp} ~4 um) ⇒ **DEPFET**
  - 5 farthermost layers: strips similar to SIT/SET

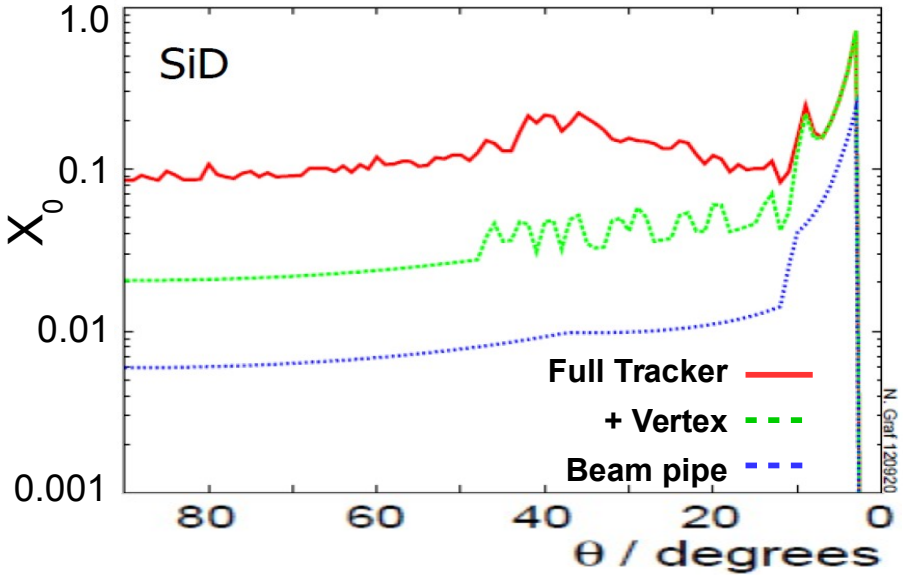


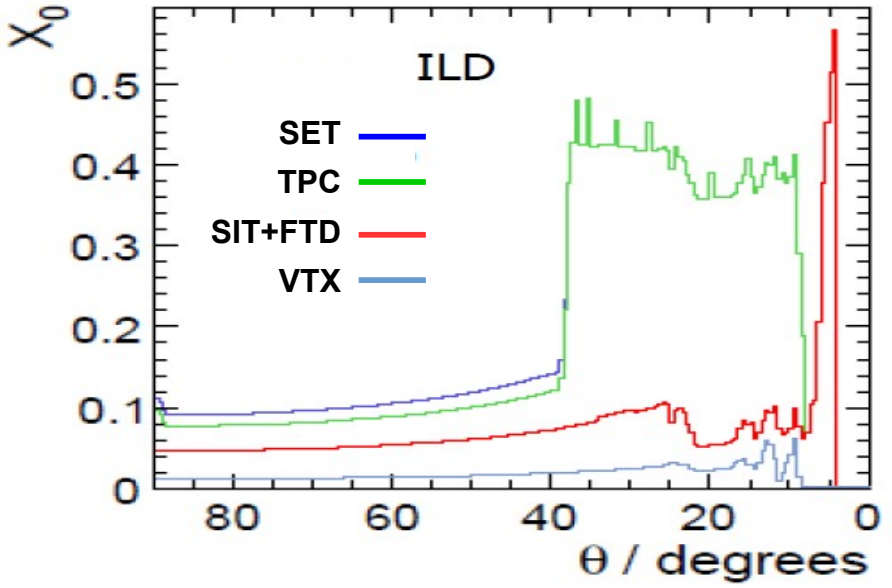
- **Barrel (VTX):** 3 × double-sided-ladders
  - Inner layers (< 300 cm^2): priority r.o. speed & σ_{sp}
    16×16/80 μm^2 pixels & binary output: $t_{r.o.}$ ~50/8 μs & σ_{sp} ~3/5 μm
  - Outer layers (~3000 cm^2): priority to power consumption & σ_{sp}
    35×35 μm^2 pixels & 3-4 bit charge encoding: $t_{r.o.}$ ~100 μs & σ_{sp} ~4 μm
  - R&D on several technologies ⇒ **DEPFET, FPCCD, SOI, CMOS**

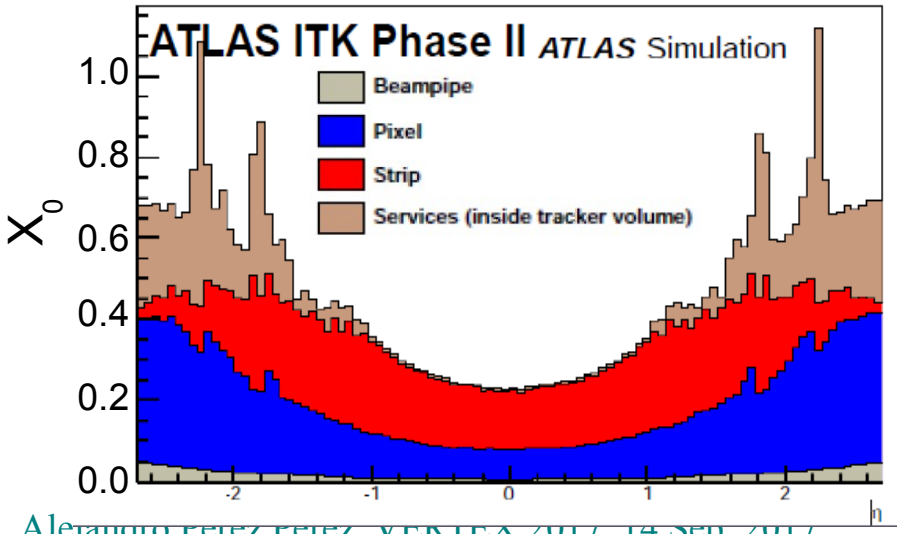


Targeted Tracking System Material Budget

X_0 vs polar angle







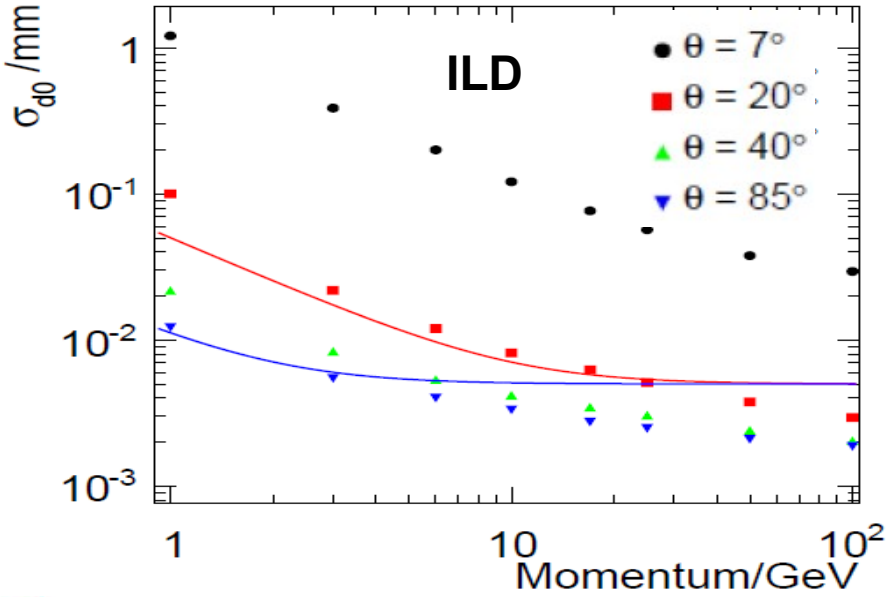
- **Goal ~10% X_0 for complete tracker in barrel region ⇒ very challenging**
- **Comparison with ATLAS barrel region**
  - Current tracker: ~50 % X_0
  - ATLAS ITK: ~30 % X_0

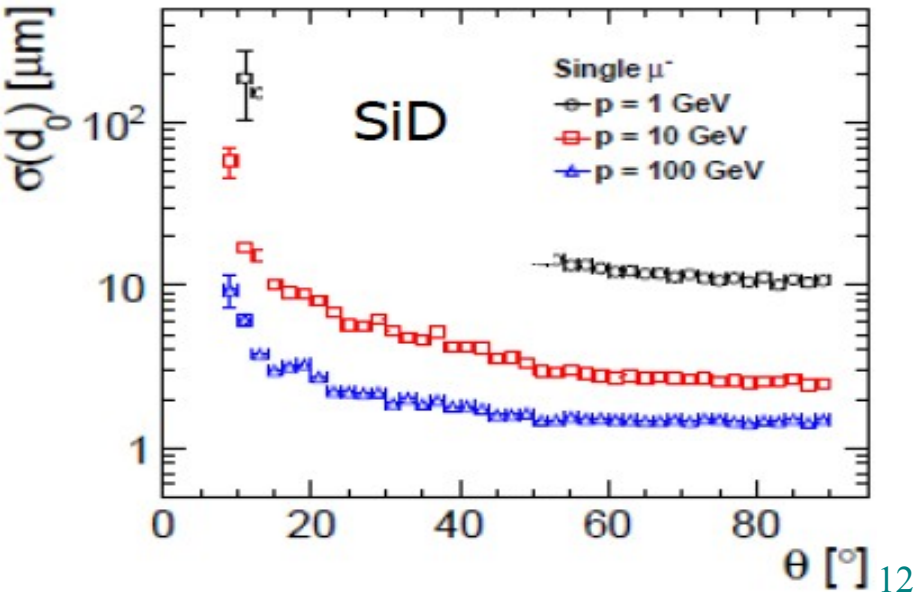
ILC Tracking system expected performances: I.P. resolution

- **Results from full simulation single muon particle gun**
  - σ_{sp} 1st VTX layer ~3 μm
  - Mat. Buget/layer ~0.15% X_0
  - Beam pipe: Be 500 μm (0.14% X_0)
  - Empirical parametrization

ILC: $\sigma(d_0) = a \oplus b/p\beta \sin^{3/2}\theta$ μm

	LEP	SLC	LHC	RHIC	ILC
a (μm)	25	8	12	13	5
b (μm GeV/c)	70	33	70	19	10



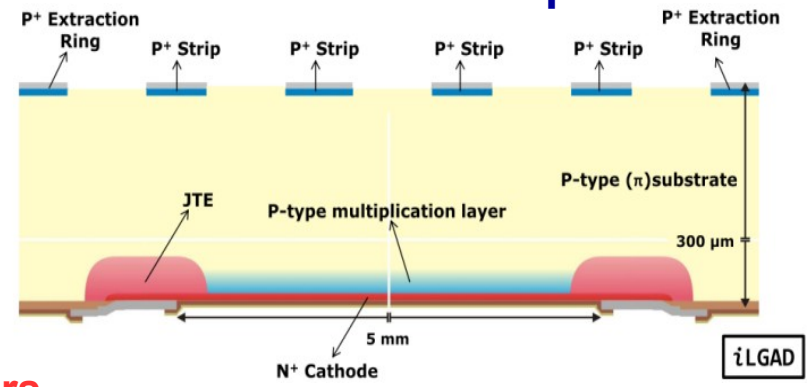


I-LGAD

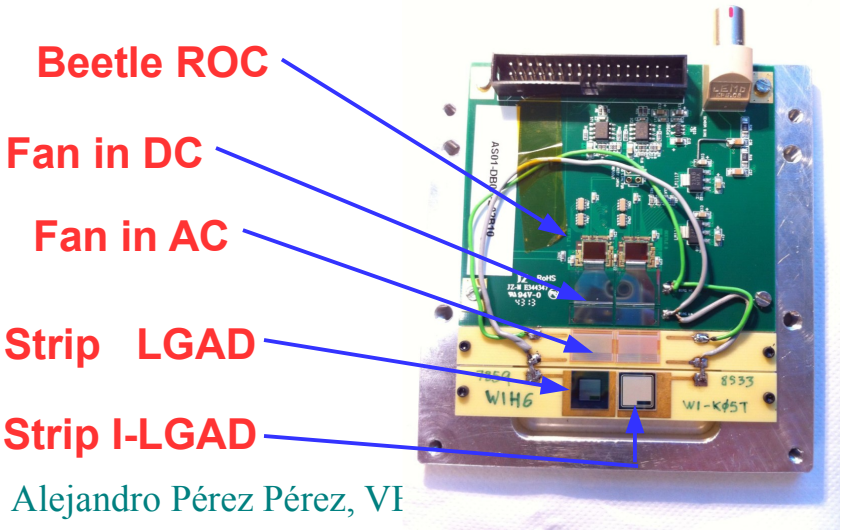
IFCA (Santander)
CNM

- **Solving the fill factor of strips LGAD**
  - No segmentation of multiplication layer
  - Segmentation of ohmic contact ⇒ collect holes
  - Detector could be very thin (35 – 40 μm)
    - Small material budget
    - Good timing (few 10s ps for hole collection)
  - **Interesting application for ILD SIT tracker layers**

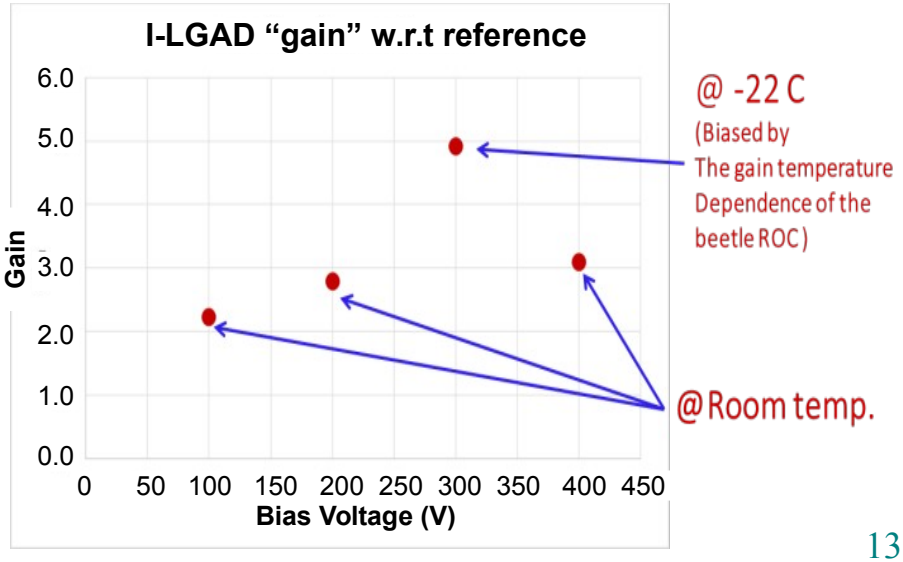
I-LGAD concept



- **First ever multi-channel tracking module based on Strip I-LGAD & LGAD**
  - 160 μm pitch & ~300 μm thickness



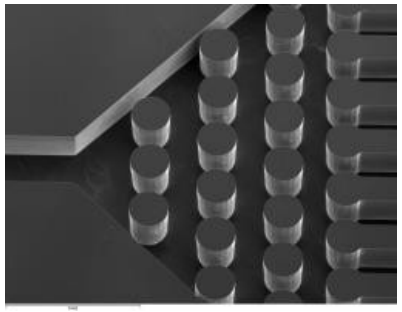
Gain ≡ MPV I-LGAD / MPV reference PIN

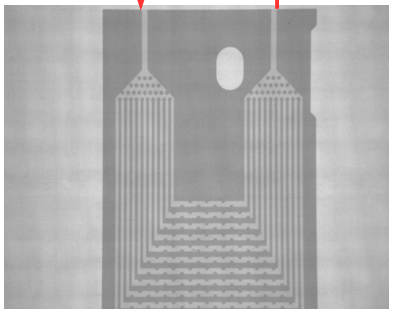


Reducing Material Budget: Technical developments

- **Power consumption & Cooling**
  - Baseline: air cooling (few 10s of W)
    - Goal: $\lesssim$ 20 mW/cm^2
  - Requirements: technology dependent
    - Baseline: air flow (few m/s) + power pulsing
    - DEPFET: FEE μ-channel cooling
    - FPCCD: requires -40°C ⇒ (2 phase-CO_2)
    - CMOS: asynch. r.o.: maybe no power pulsing

Handle wafer
DRIE etching

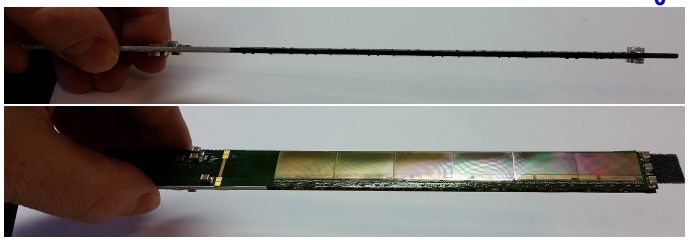




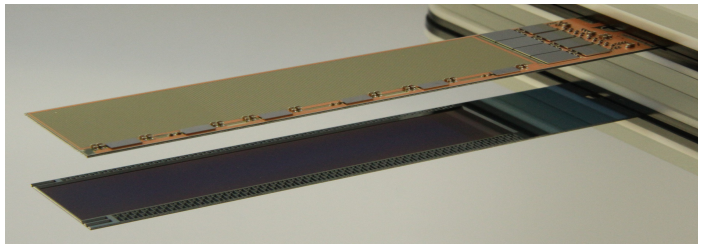
See P. Petagna (Overview), A. Mapelli (NA62), O. Aguilar (LHCb) Talks

- **Sensor integration in ultra-light devices**
  - Beam-pipe: Be 500 μm (0.14% X_0)
  - 50 μm thick sensors routinely produced
    e.g. CMOS, DEPFET, …
  - Today: 0.2 – 0.4 % X_0/layer in acceptance
  - 0.15% X_0/layer seems reachable!

Plume 2: 2 sided ladder: 0.35 % X_0



Belle-II DEPFET module: 0.21 % X_0

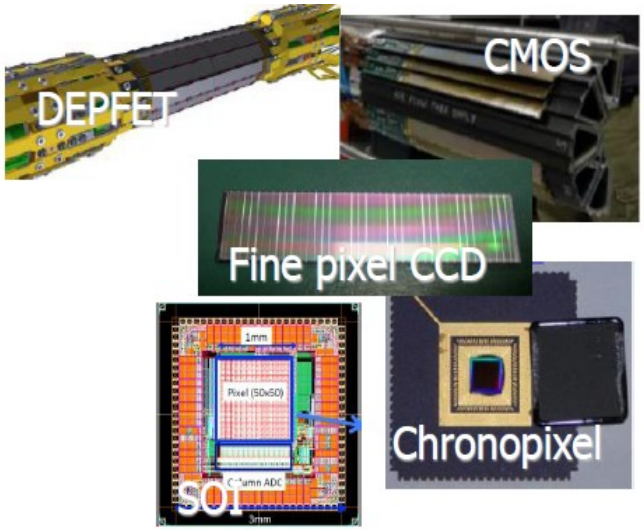


See J. Dingfelder Talk

Vertex detector Technologies

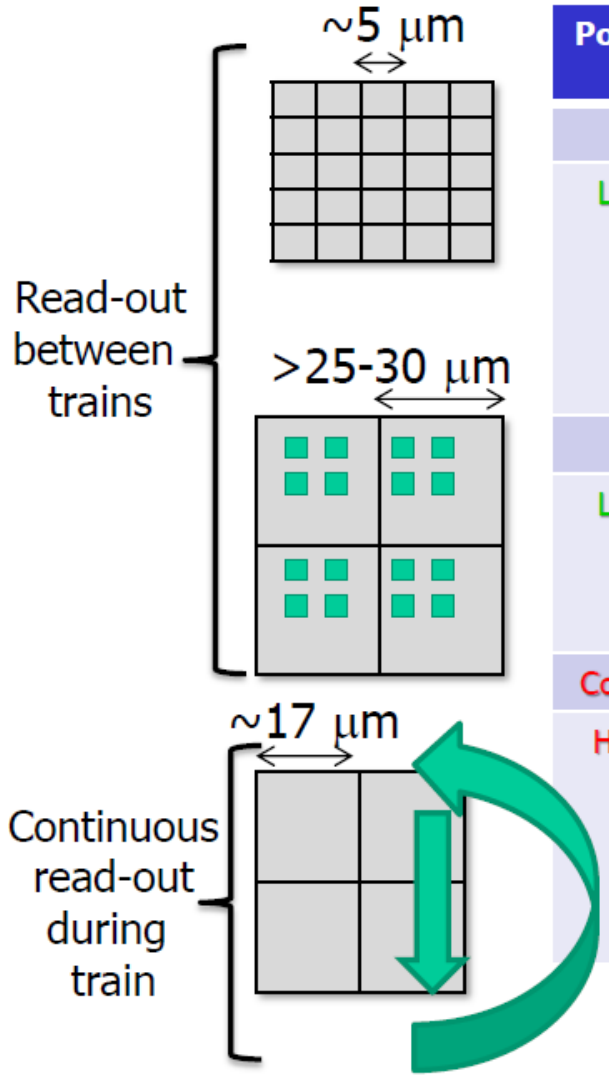
- **ILD & SiD share Vertex Detector R&D**
  - Several mature technos. considered needing more R&D to meet requirements
  - Safety margin uncertainty mainly from beam bkg knowledge
    - Large systematics and depends on beam-energy and IR design

- **No technology yet chosen**
  - Still have some time and all technologies still evolving
  - Selection based on physics benchmarks performances
  - Different geometries are being considered
    - 3 x double-sided-ladders vs 5 single-sided?
    - Long or short barrel + disks?
  - Different r.o. strategies
  - Performances obtained with technology/geometry specific tracking/vertexing algorithms



- **Several options still on the table**

VTX Readout Strategies



Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 μm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 μs)	>~ 5 μm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (5-50 μs)	~ 3 μm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^5 grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

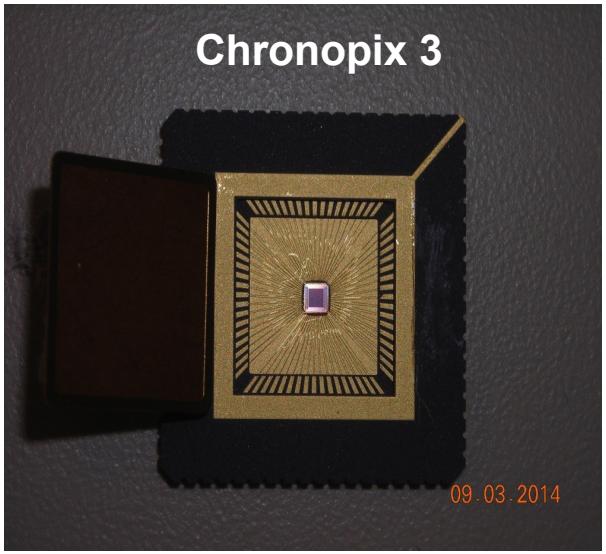
⇨ Figures may evolve significantly with R&D and access to new technologies
e.g. feature size ⇨Power, read-out speed, granularity, etc.
⇨Different options / room for mixed strategies ?
e.g. double sided ladders: 1-fast / 1-precise

Chronopix

- **Design features**
  - Monolithic CMOS pixel detector
  - In-pixel
    - Pre-amp + Discri with offset compensator
    - Time-stamping (bunch-tagging) up to 2 hits (14-bits)
  - Sparsified r.o. between trains

- **R&D efforts**
  - 3 sets of small prototypes since 2008
  - Chronopix 3: 25x25 μm^2 in TSMC 90 nm CMOS (2015)
  - Set of prototypes showed
    - Time-steping better than 300 ns proven
    - Sparsified readout architecture works
    - Power pulsing tested
    - Noise & cross-talk controlled
  - Next steps
    - No show stoppers for full-size prototype
    - Still several optimizations of design

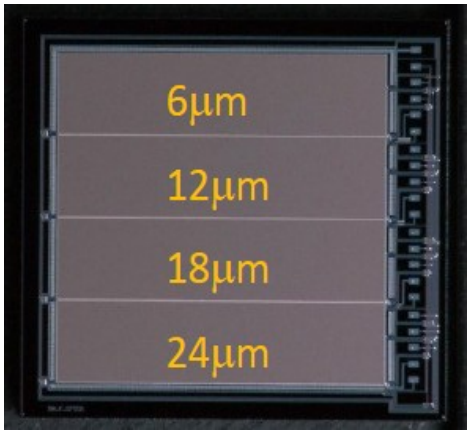
Oregon University
Yale University



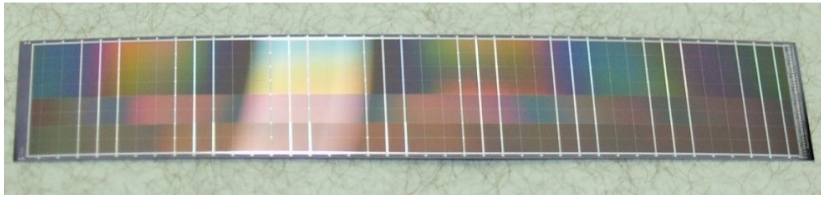
FPCCD

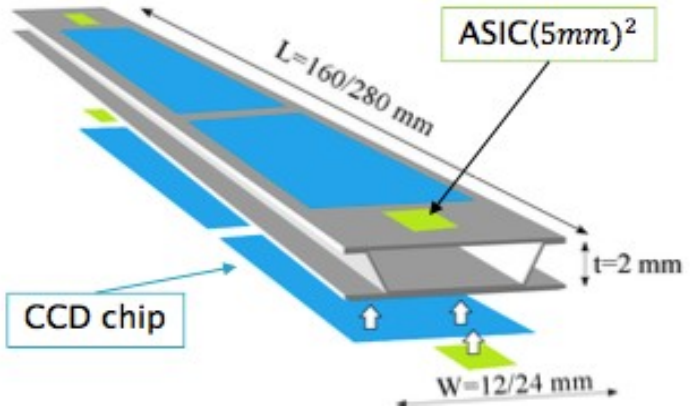
Tohoku University, KEK,
Shinshu University, JAXA

- **Studies with small prototypes with 6x6 μm² pixel**
  - Small prototypes 6x6 mm² thinned to 50 μm
  - 4 channels with diff. register size: 6, 12, 18, 24 μm
  - Prototype sufficiently radiation hard
- **Large prototype**
  - Real size sensor 12.3 x 62.4 mm² for double-sided ladder
  - 125 x 13000 pixels with 16 r.o. nodes
  - Readout ASIC prototype (TSMC 250 nm CMOS)
    - Between train r.o.
    - Amp+LPF+CDS+ADC+LVDS driver
    - 10 MHz r.o., 6 e^- noise, 5.6 mW/channel
  - FPCCD + r.o. chip: 44 e^- noise
  - Mechanics: Carbon fibre and flex
  - Operates @ -40°C: CO_2 cooling
- **Next steps**
  - Beam-tests, ladders assembly + cooling
  - Improve readout speed

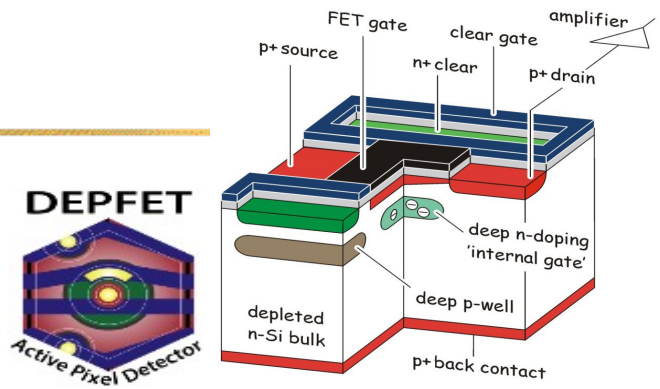


Large prototype: 12.3 mm × 62.4 mm × 50 μm

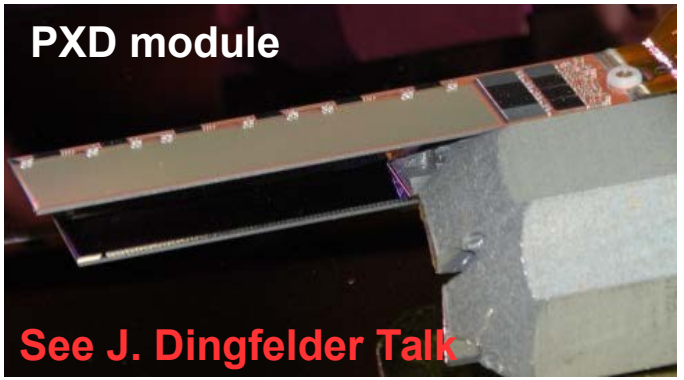




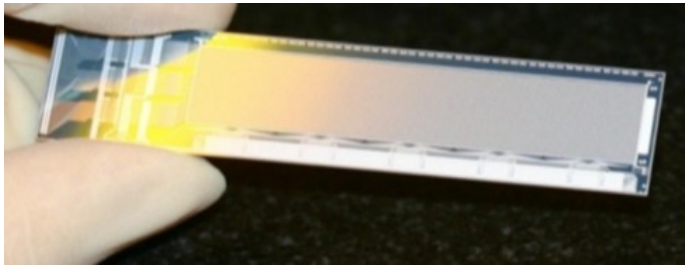
DEPFET



- **Development driven by Belle-II PXD**
  - Ladder assembly qualified
  - PXD modules currently in 1st pre-production batch
  - SuperKEKB commissioning phase 2 (low lumi)
    - One sector of PXD will be installed
    - Machine bkg measurements & system validation



- **Thin DEPFET for ILC**
  - ILC prototypes manufactured
  - 0.15% X_0 seems achievable: including switcher chips
  - Resolution studies in simulation and Beam-test
  - μ-channel cooling under development
  - Interest in pixelated FTD, and maybe VTX
  - Next Steps: r.o. speed and integration

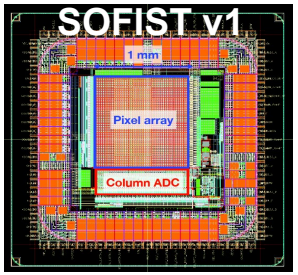


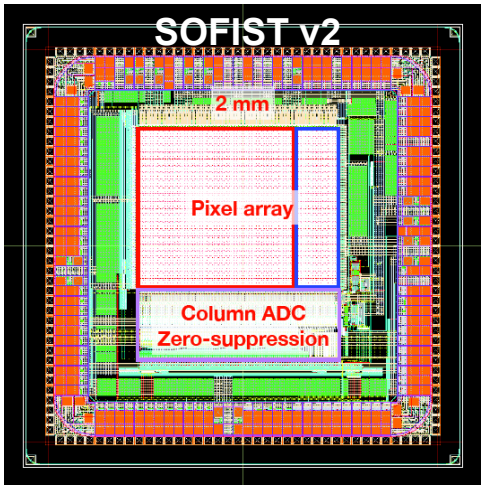
SOFIST: SOI sensor for Fine measurement of Space and Time

- **Goal:** fine pixels (~20x20 μm^2) & bunch time-stamping
- **SOFIST v1: delivered Dec. 2015**
  - Chip size 2.9x2.9 mm^2 (pixel 20x20 μm^2)
  - Pre-amp (CSA) + Analog memories (2 hits)
  - Column ADC (8 bits)
  - FZ n-type (single SOI)
  - TB @ Fermilab: σ_{sp} ~ 1.5 μm
- **SOFIST v2: delivered Jan. 2017**
  - Chip size 4.5x4.5 mm^2 (pixel 25x25 μm^2)
  - Pre-amp + Comp + Shift register + Analog memories (2 hits)
  - Column ADC (8 bits) + Zero-suppression
  - Cz p-type (double SOI)
  - Under evaluation
- **SOFIST v3 & 4: under design, submission June 2017**
  - Chip size 6x6 & 4.5x4.5 mm^2 (pixel 30x30 & 20x20 μm^2)
  - Pre-amp + Comp + Shift register + Analog memories (3 hits)
  - Column ADC (8 bits) + Zero-suppression
  - FZ p-type (double SOI)

See K. Hara Talk for SOI recent developments

Osaka University, Tsukuba University, Tohoku University, KEK

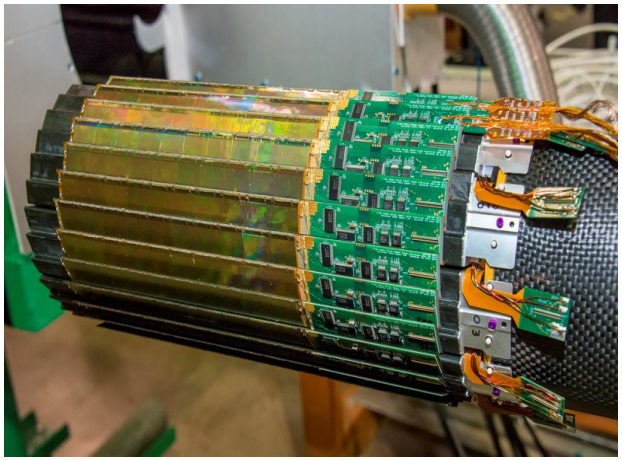




CMOS Pixel Sensors (CPS)

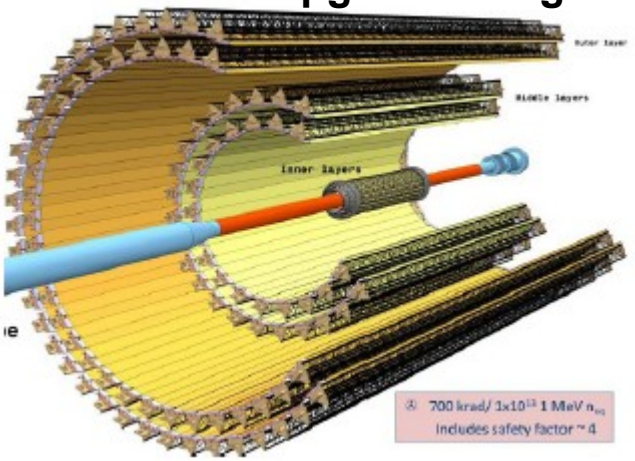
- **CPS for ILC**
  - Exploit potential of available CMOS technologies
  - R&D performed in synergy with several applications
    - EUDET-BT, STAR, ALICE & CBM
  - CPS is unique technology being simultaneously
    - Granular, thin, integrating full FEE, industrial & cheap
  - Address trade-off between spatial resolution & r.o. speed
- **Current developments**
  - Driven by ALICE-ITS and CBM-MVD
    - Tower-Jazz 180 nm CMOS process
    - In pixel pre-amp + discrim. & asynchronous r.o.
  - Focus on increased r.o. speed: few μs ⇒ bunch tagging
    - To comply with beam bkg uncertainties
  - Keep low power consumption
    - Potential to avoid power pulsing
  - Radiation tolerance >> needed for ILC
  - Potential use for trackers (large surfaces)
    - Large pixels detection efficiency demonstrated

START-PXL



See G. Contin Talk

ALICE-ITS upgrade design



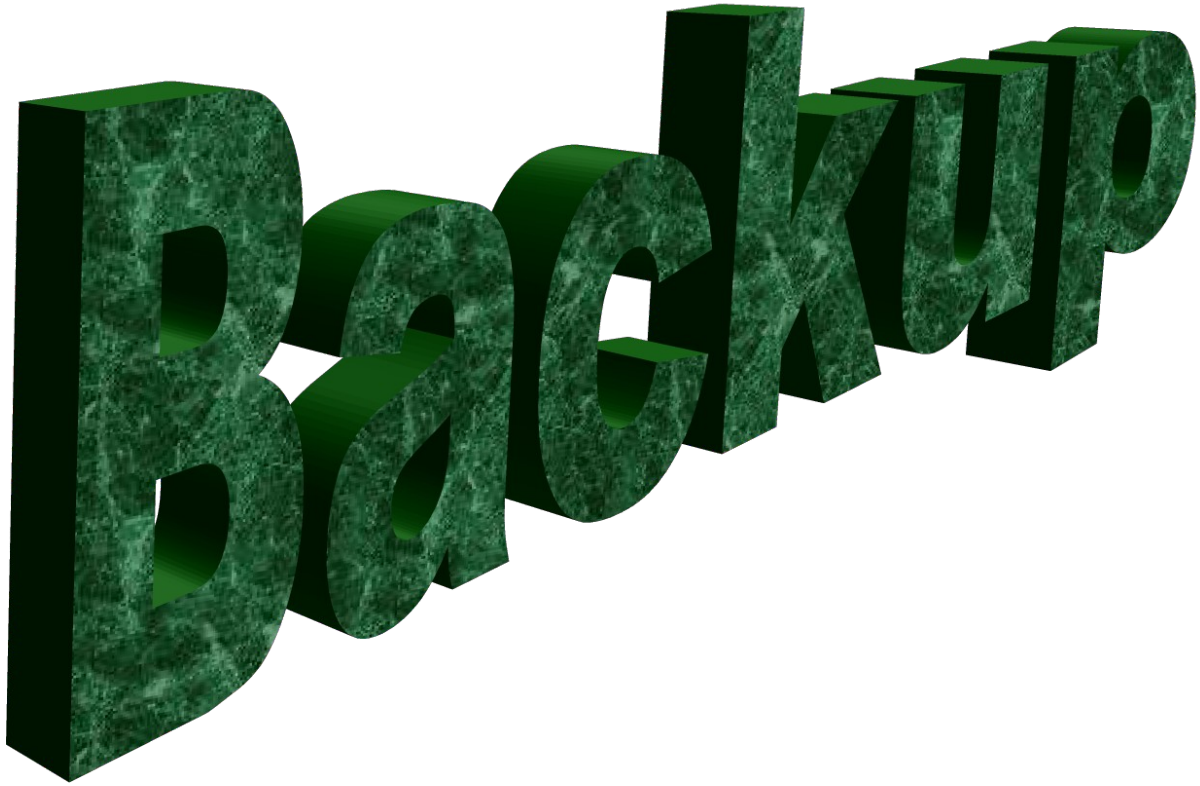
See A. Alici Talk

Summary and Outlook

- **ILC is a Mature Project**
  - Accelerator TDR
  - ILD & SiD: feasibility of detectors demonstrated in DBD document in 2012

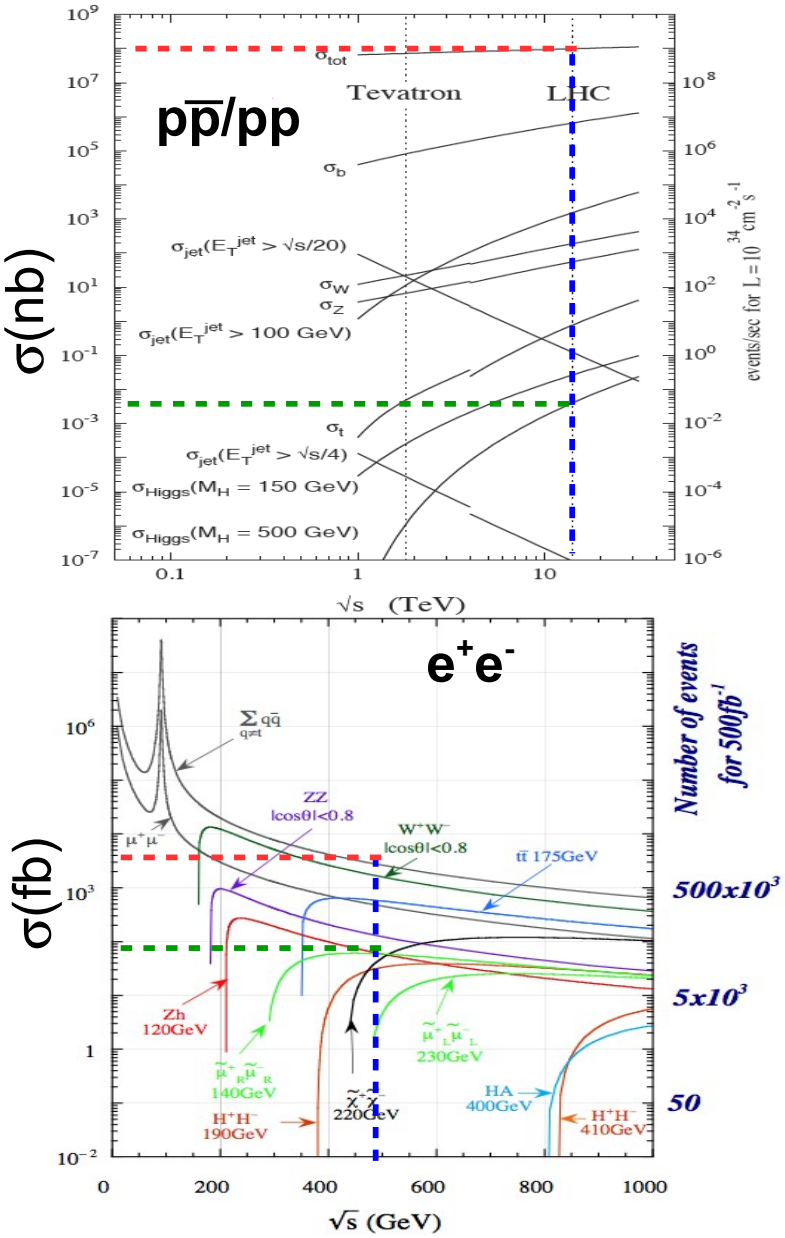
- **Vertex and Tracking Detectors**
  - Many options still available: technologies, r.o. architecture, geometries, …
  - Several experiments already approaching ILC specifications: ALICE, CBM, Belle-II, …
  - R&D still very active
    - Detector performances
    - Robustness w.r.t beam background & $\sqrt{s}$ program
    - Careful mechanical integration studies
    - Tracking & Vertexing performances

- **What's next?**
  - Scientific environment & political opportunities for Japan $\Leftrightarrow$ rest-of-the-world
  - Coming years
    - Refine requirements & prioritize physics goals
    - On the road for ILD & SiD TDR


Backup

Physics @ ILC: Key Features

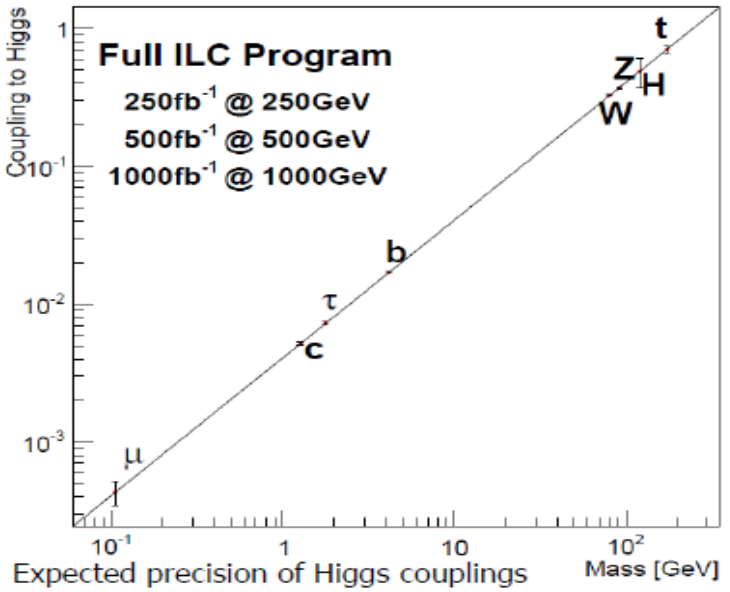
- **Clean Environment**
  - No QCD background ⇒ no pile up
  - Well known initial state
  - Fully reconstructible channels (even fully hadronic)
- **Precise Theoretical Predictions**
  - Radiative corrections O(1%)
  - Theoretical uncertainties O(0.1%)
- **Tunable √s ⇒ Threshold scans & flexibility**
- **Beam polarization ⇒ S/N enhancement**
- **Cross sections**
  - Globally small (σ_{ZH} ~ 100 fb) but ...
  - Higgs production @ LHC: $1/10^{10}$ events
  - Higgs production @ ILC: $1/10^{2}$ events
- **Advantages**
  - Triggerless
  - Low backgrounds
  - Most measurements statistically limited



Physics @ ILC: Goals

- **Very rich physics program**
  - Top physics
  - EW precision measurements
  - Direct/indirect BSM searches
- **Higgs sector**
  - O(1%) precision of Higgs mass/width/spin & couplings
  - Model independent measurements
    - Access σ and σ×Br
    - Probe BSM, model disentangling
- **Very important role of Vertex detector**
  - Favour tagging (b, c, τ)
  - Low momentum tracking (as lows as 200 MeV/c)
  - Jet charge determination

Energy	Reaction	Physics Goal
91 GeV	$e^+e^- \to Z$	ultra-precision electroweak
160 GeV	$e^+e^- \to WW$	ultra-precision W mass
250 GeV	$e^+e^- \to Zh$	precision Higgs couplings
350–400 GeV	$e^+e^- \to t\bar{t}$	top quark mass and couplings
	$e^+e^- \to WW$	precision W couplings
	$e^+e^- \to \nu\bar{\nu}h$	precision Higgs couplings
500 GeV	$e^+e^- \to f\bar{f}$	precision search for Z'
	$e^+e^- \to t\bar{t}h$	Higgs coupling to top
	$e^+e^- \to Zhh$	Higgs self-coupling
	$e^+e^- \to \tilde{\chi}\tilde{\chi}$	search for supersymmetry
	$e^+e^- \to AH, H^+H^-$	search for extended Higgs states
700–1000 GeV	$e^+e^- \to \nu\bar{\nu}hh$	Higgs self-coupling
	$e^+e^- \to \nu\bar{\nu}VV$	composite Higgs sector
	$e^+e^- \to \nu\bar{\nu}t\bar{t}$	composite Higgs and top
	$e^+e^- \to \tilde{t}\tilde{t}^*$	search for supersymmetry



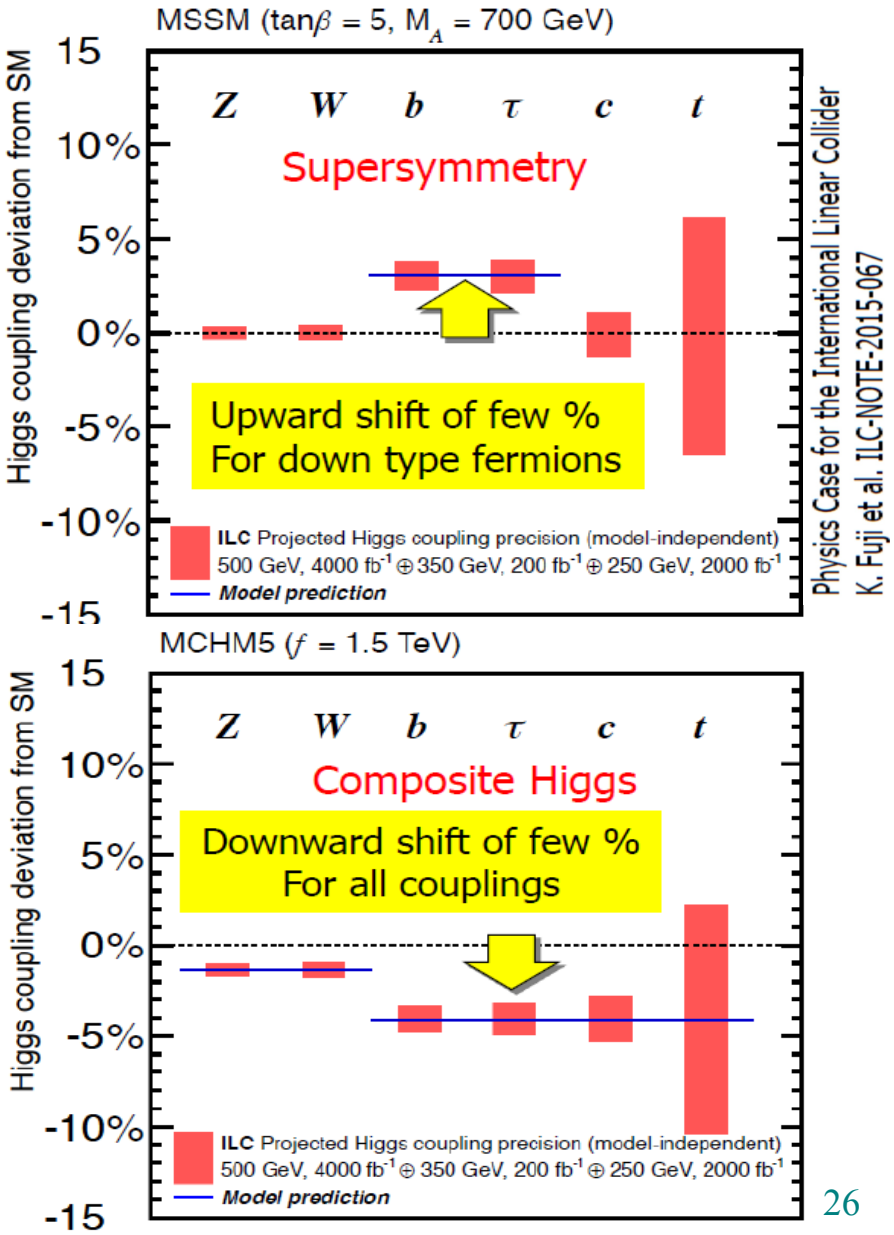
Physics @ ILC: BSM example

- **Is the O(1%) precision on Higgs couplings enough**
- **Size of deviation depends on BSM mass scale**

$$\frac{g_{hbb}}{g_{h_{SM}bb}} = \frac{g_{h\tau\tau}}{g_{h_{SM}\tau\tau}} \simeq 1 + 1.7\% \left(\frac{1\ \text{TeV}}{m_A}\right)^2$$

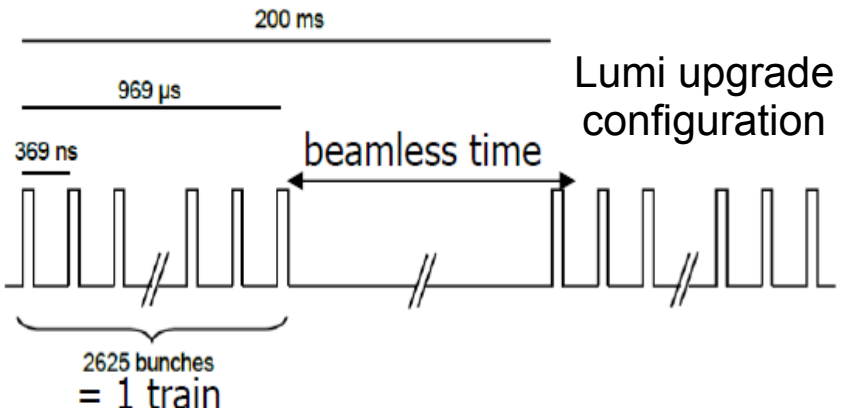
heavy Higgs mass

- **Correlations of Higgs couplings deviation from SM allows to disentangle new physics models**



ILC Experimental Environment

- **Beam structure**
  - 5 trains/s of ~1300/2600 bunches
  - 1 bunch every 550/370 ns
  - Beam-less time ~ 200 ms
  - Operation strategies
    - Full detector readout (r.o.) ⇒ triggerless
    - Possible r.o. during beam-less time
    - Power pulsing ⇒ reduced power

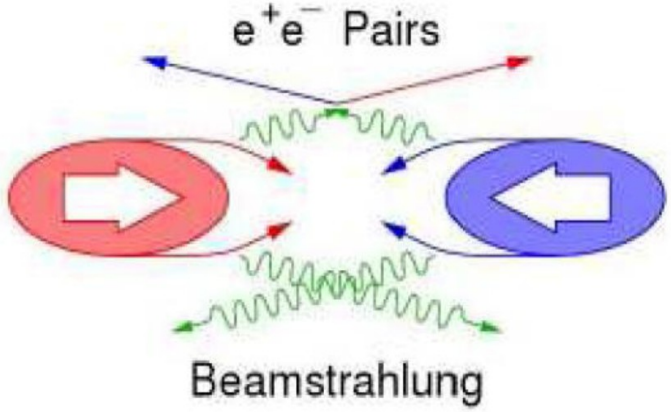


Lumi upgrade configuration

- **Beam induced bkg: Beamstrahlung**
  - Beam energy loss: ~1% @ 250 GeV
  - Radiation level: ~100kRad ⊕ 10^{11} n_{eq}/cm^2

    (HL-LHC: ~1GRad ⊕ 10^{16} n_{eq}/cm^2)
  - Main source of occupancy
    - Drives VTX r.o. speed & minimum radius
    - Physics cross section negligible (~ 1 evt/s)

Bunches have electric space charge
⇨ particles deflected
⇨ photons emissions
⇨ e^+e^- pairs ("beamstrahlung")



ILC Experimental Environment: Beam Bkg on ILD

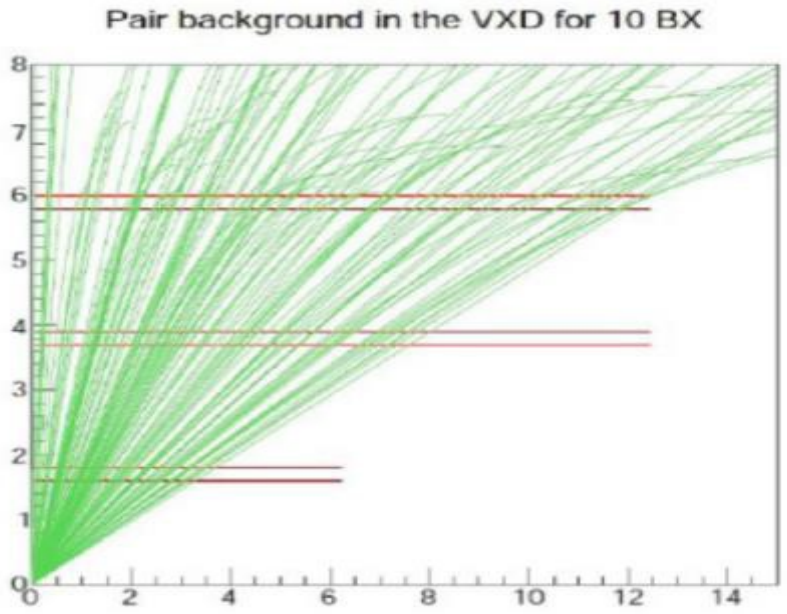
- **Beam Bkg Simulation (Guinea Pig)**
  - e^+e^- pairs production
  - √s dependent rates
  - ~20% rates due to back scatterers
  - Stat-only error, systematics much higher

Sub-detector	Units	Layer	TDR ws 500 GeV	B1b ws 1000 GeV
VTX-DL	hits/cm^2/BX	1	6.320 ± 1.763	11.774 ± 0.992
		2	4.009 ± 1.176	7.479 ± 0.747
		3	0.250 ± 0.109	0.431 ± 0.128
		4	0.212 ± 0.094	0.360 ± 0.108
		5	0.048 ± 0.031	0.091 ± 0.044
		6	0.041 ± 0.026	0.082 ± 0.042
SIT	hits/cm^2/BX	1	0.0009 ± 0.0013	0.0016 ± 0.0016
		2	0.0002 ± 0.0003	0.0004 ± 0.0005
FTD	hits/cm^2/BX	1	0.072 ± 0.024	0.145 ± 0.024
		2	0.046 ± 0.017	0.102 ± 0.016
		3	0.025 ± 0.009	0.070 ± 0.009
		4	0.016 ± 0.005	0.046 ± 0.007
		5	0.011 ± 0.004	0.034 ± 0.005
		6	0.007 ± 0.004	0.024 ± 0.006
		7	0.006 ± 0.003	0.022 ± 0.006
SET	hits/BX	1	0.196 ± 0.924	0.588 ± 2.406
		2	0.239 ± 1.036	0.670 ± 2.616
TPC	hits/BX	-	216 ± 302	465 ± 356
ECAL	hits/BX	-	444 ± 118	1487 ± 166
HCAL	hits/BX	-	18049 ± 729	54507 ± 923

R = 1.6 cm

R = 6.0 cm

E. Avetisyan, LC-REP-2013-002

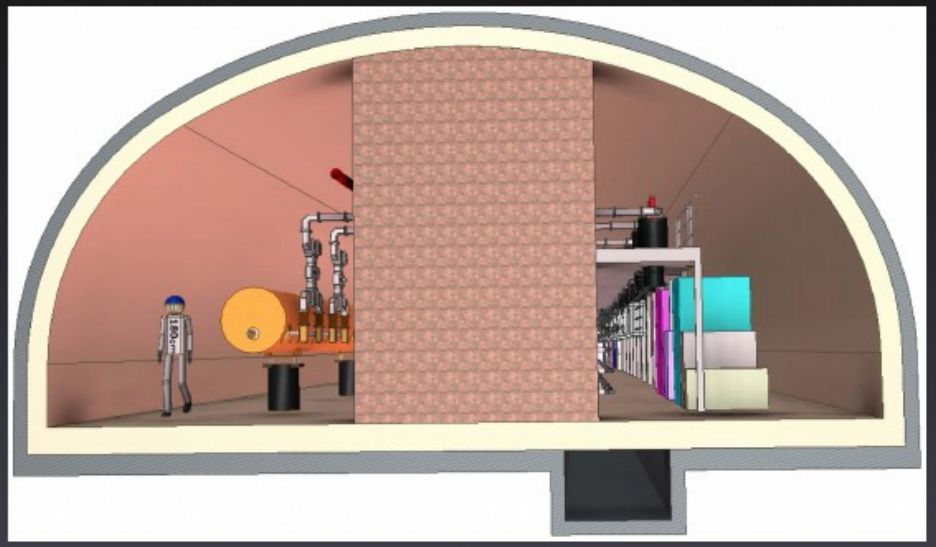


- **Some features**
  - Low momentum (10 – 100 MeV/c) real tracks!
  - Typical rate of ~ 6 hits/cm^2/BX on innermost VTX layer
  - Very sensitive to IR design
  - Large systematic uncertainty

    ⇒ Safety factor of at least x5 needed

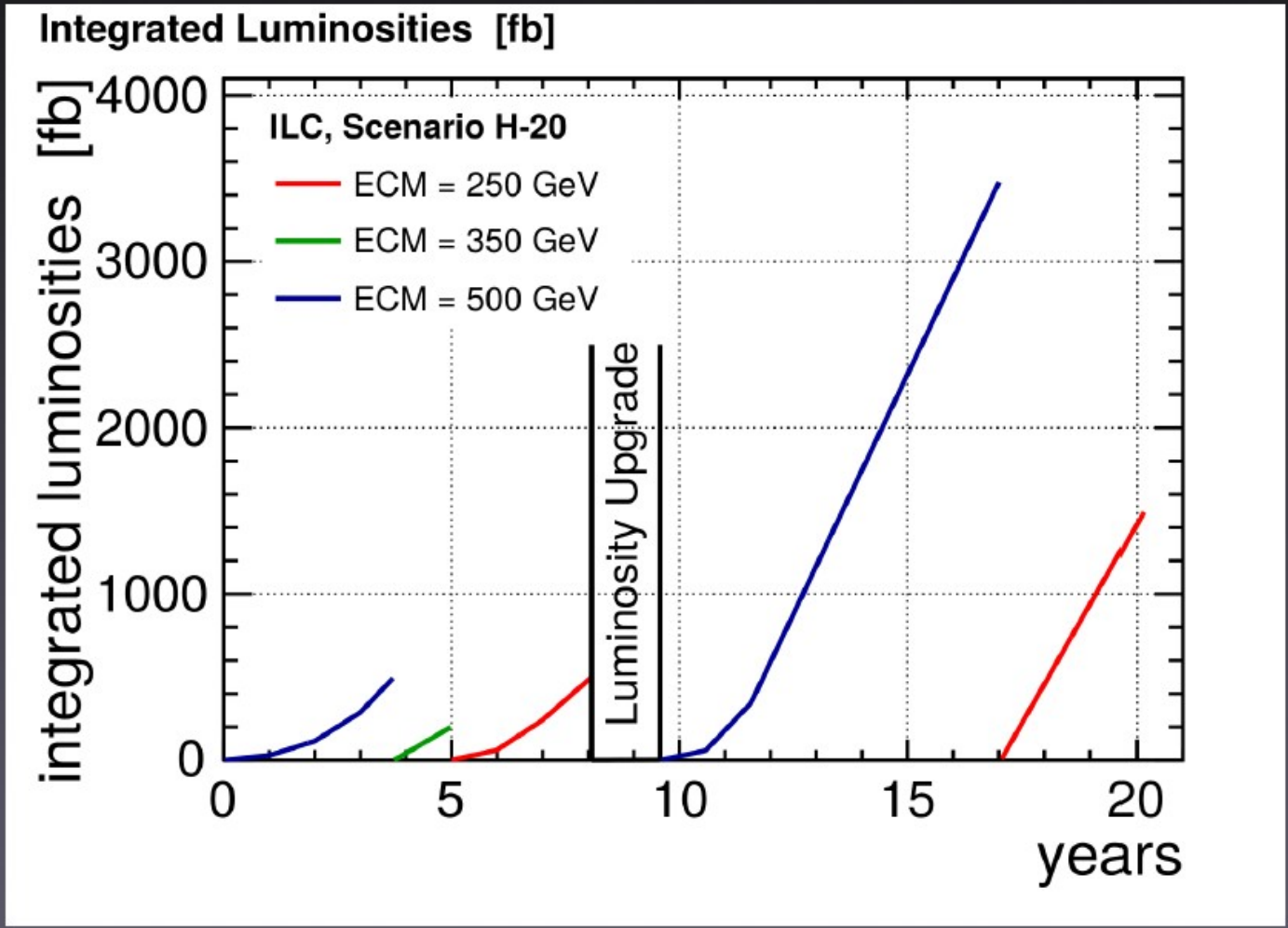
The ILC Machine

- 500 GeV Linear collider
  - 31 km long
- Acceleration
  - 7400 superconducting Cavities in 850 Cryo Modules
  - Gradient 31.5 MV/m
  - 1.3 GHz RF
  - 163 MW power consumption
- Beam parameters
  - 2×10^{10} particles/bunch
  - 554 ns spacing
  - $L = 1.8 \times 10^{34}\ cm^{-2}s^{-1}$
  - Polarization 80/30 (e^-/e^+)
  - Nanometer-scale beam spot

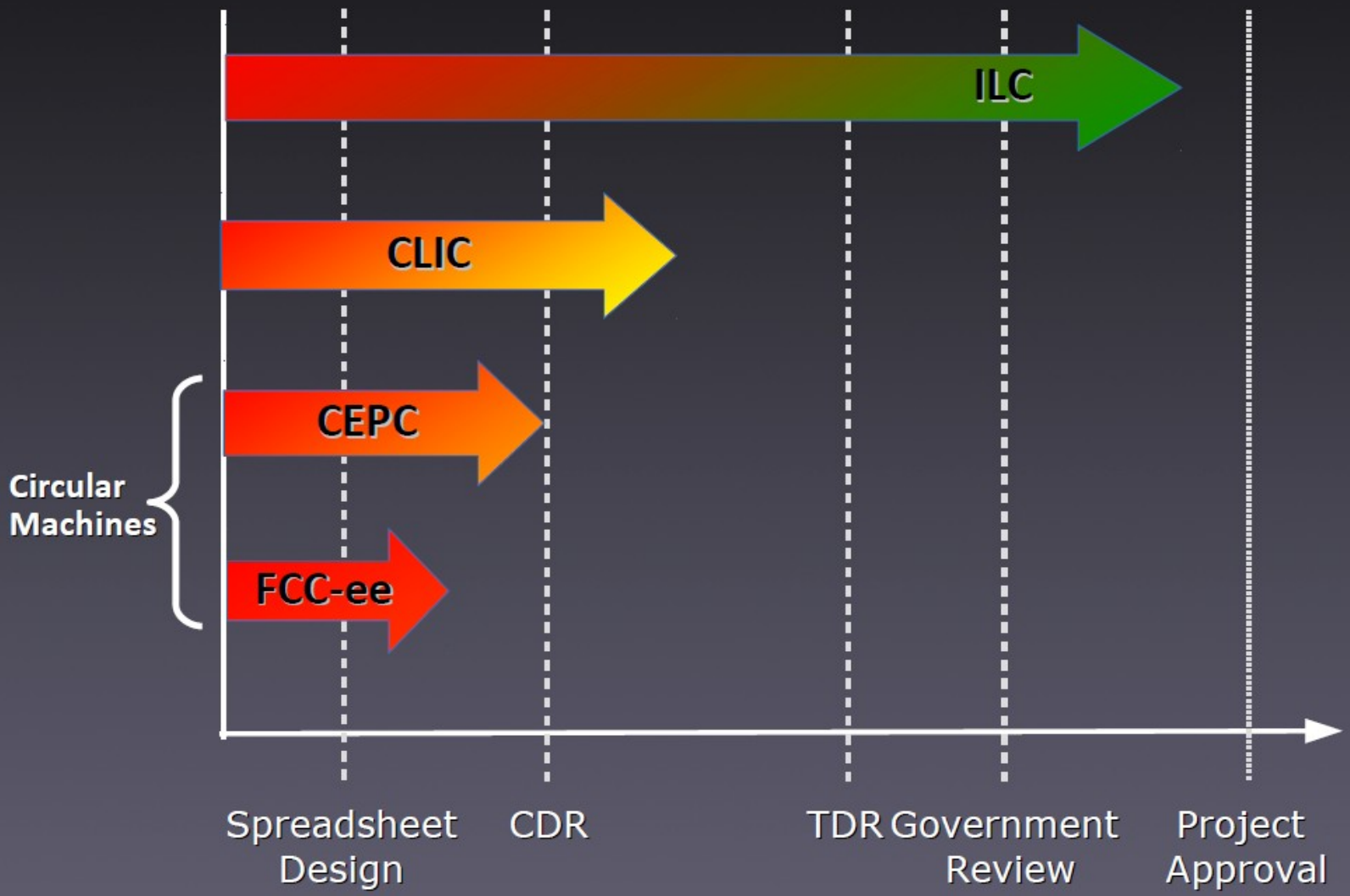


ILC Site – Kitakami Mountains

ILC baseline program

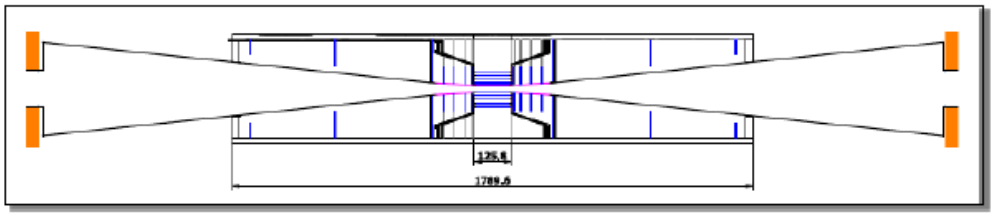


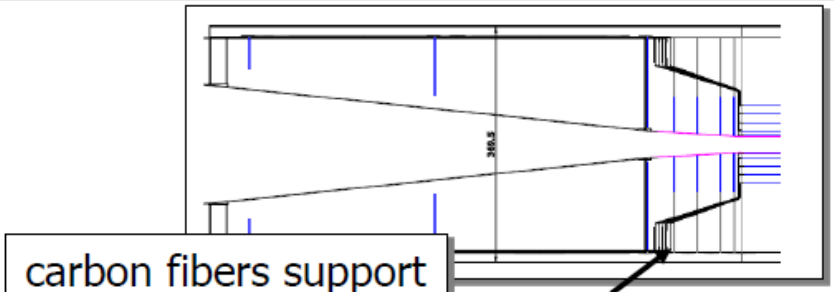
Project Readiness Comparison



SiD: vertex detector

- Layout:
  - Short barrel approach
  - Barrel: 5 silicon pixels layers
  - Forward disks
    - 4 disks at short distance
    - 3 disks at longer distance
- Technology options
  - Baseline
    - pixels pitch: 20 x 20 μm^2
  - CMOS based Chronopixels
    - In pixel 12 bits time stamping
    - Read-out between trains
    - Reduce beam background
    - Allows tracking with VTX seeding
    - Requires very advanced technology (90 nm)
  - 3D vertical integrated silicon
    - Even more challenging





carbon fibers support

cable routes

Barrel	R	z_{max}
Layer 1	14	63
Layer 2	22	63
Layer 3	35	63
Layer 4	48	63
Layer 5	60	63

Disk	R_{inner}	R_{outer}	z_{center}
Disk 1	14	71	72
Disk 2	16	71	92
Disk 3	18	71	123
Disk 4	20	71	172

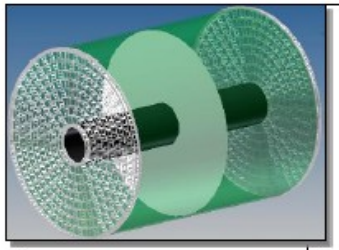
Forward Disk	R_{inner}	R_{outer}	z_{center}
Disk 1	28	166	207
Disk 2	76	166	541
Disk 3	117	166	832

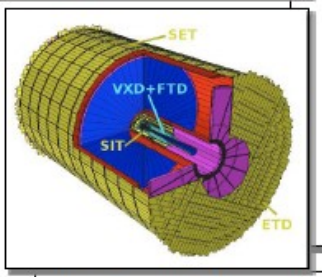
(in mm)

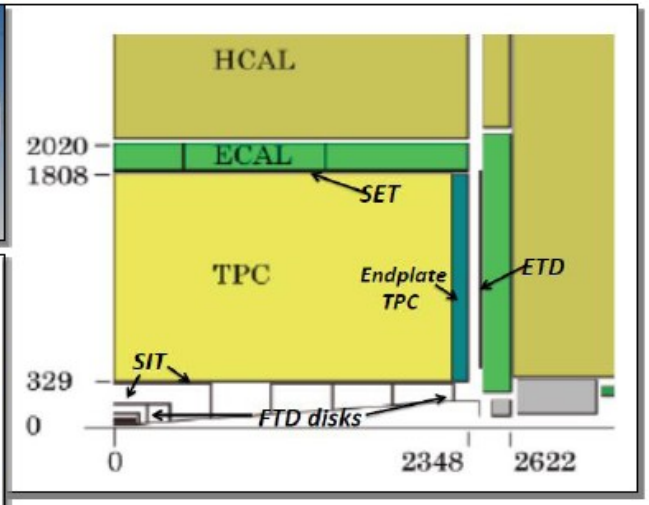
ILD tracking system: TPC + silicon (1)

- Main system: TPC
  - 2 options: GEMs/Micromegas
- Silicon Strip detectors
  - 200μm thick silicon, 50 μm pitch, 10x10cm^2 sensors, edgeless, 7μm sp.res.
  - 4 components
    - Silicon inner Tracker (SIT)
    - Silicon External Tracker (SET)
    - End cap Tracker (ETD)
    - Forward Tracker (FTD)

    (2 inners with pixels + 5 with strips)
  - Goals:
    - Improves resolution
    - Linking VTX-Tracker-ECal
    - Improves calibration, alignement
    - Allows time stamping
  - Challenges and R&D:
    - maintain the mat.budget small
    - push pull compatible
    - minimize power (power pulsing)





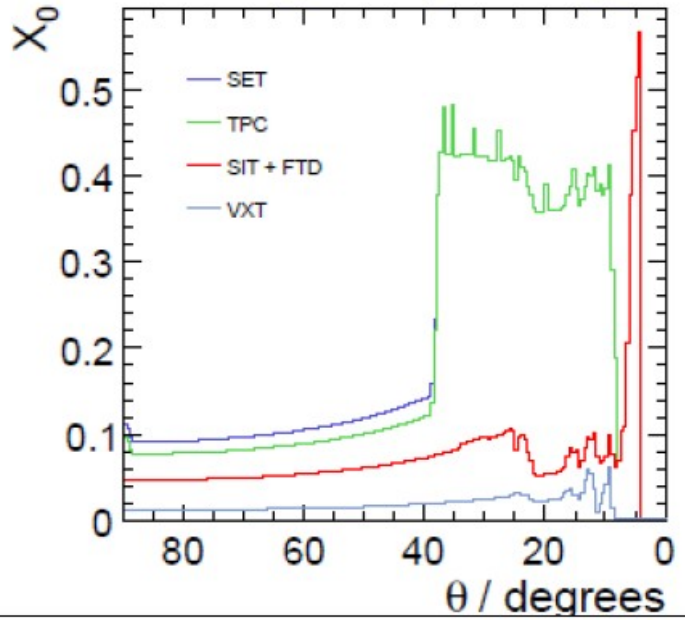


Performance/Design Goals	
Momentum resolution[a] at B=3.5T	$\delta(1/p_t) \simeq 10^{-4}$/GeV/c TPC only
Solid angle coverage	Up to $\cos\theta \simeq 0.98$ (10 pad rows)
TPC material budget	$\simeq 0.05\,X_0$ including the outer field cage in r
	$< 0.25\,X_0$ for readout endcaps in z
Number of pads/timebuckets	$\simeq$ 1-2×10^6/1000 per endcap
Pad pitch/no.padrows	$\simeq$ 1 mm×4-10 mm/≃200
σ_{point} in $r\phi$	$< 100\mu$m (avg for straight-radial tracks)
σ_{point} in rz	$\simeq 0.4 - 1.4$ mm (for zero – full drift)
2-hit resolution in $r\phi$	$\simeq$ 2 mm (for straight-radial tracks)
2-hit resolution in rz	$\simeq$ 6 mm (for straight-radial tracks)
dE/dx resolution	$\simeq$ 5 %
Performance	> 97% efficiency for TPC only (p_t > 1GeV/c)
	> 99% all tracking (p_t > 1GeV/c)
Background robustness	Full efficiency with 1% occupancy,
Background safety factor	Chamber prepared for 10–20% occupancy
	(at the linear collider start-up, for example)

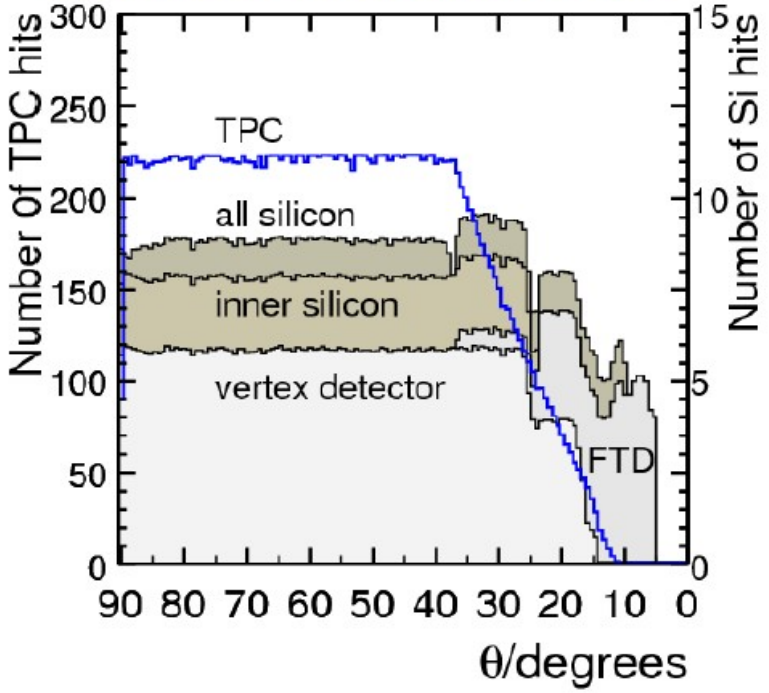
[a]The momentum resolution for the combined central tracker is $\delta(1/p_t) \simeq 2 \times 10^{-5}$/GeV/c

ILD tracking system: TPC + silicon (2)

Radiation length vs polar angle



Number of hits vs polar angle



Goal: ~10% X_0 for the complete tracker

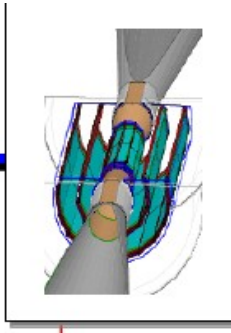
SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65

SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1811	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65

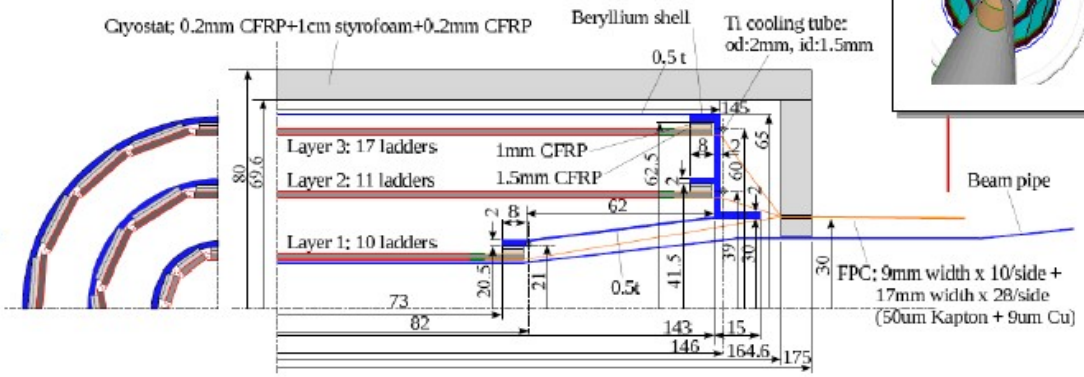
ETD characteristics (current baseline = single-sided Si micro-strips, same as SET ones)				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
419.3-1822.7	2420	0.985-0.799	x:σ=7.0	0.65

FTD characteristics (design baseline: pixels for two inner disks, microst				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
39-164	220	0.985-0.802		0.25-0.5
49.6-164	371.3	0.991-0.914	σ=3-6	0.25-0.5
70.1-308	644.9	0.994-0.902		0.65
100.3-309	1046.1	0.994-0.959		0.65
130.4-309	1447.3	0.995-0.998	σ=7.0	0.65
160.5-309	1848.5	0.996-0.986		0.65
190.5-309	2250	0.996-0.990		0.65

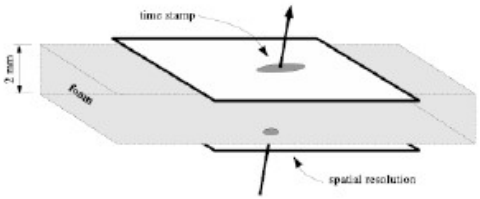
ILD: Vertex detector

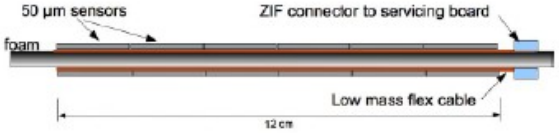


- Layout (DBD geometry):
  - Long Barrel approach
  - Radius: ~15 mm – 60mm
  - 3 x double sided ladders
    - Optimize material budget / alignment.
    - Stand alone tracking improvment
    - Background tagging capabilities
    - Other option: 5 single sided layers
  - Layers 1 & 2:
    - Priority to read-out speed & spatial resolution
    - Small pixels: 17 x 17 / 33 μm^2
    - Binary charge encoding
    - Read-out time ~ 50 / 8 μs
    - σ_{sp} ~ 3 / 5 μm
  - layers 3 – 6
    - Optmized for power comsumption
    - Large pixels (25/35 x 35 μm^2)
    - 3-4 bits charge encoding
    - Read-out time ~ 60 μs
    - σ_{sp} ~ 4 μm



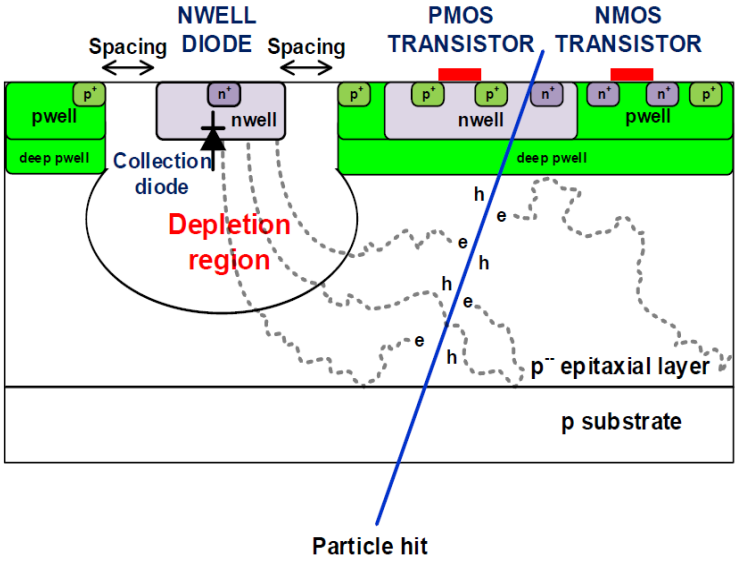
	R (mm)	$\lvert z \rvert$ (mm)	$\lvert \cos\theta \rvert$	σ (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	50
Layer 2	18	62.5	0.96	6	10
Layer 3	37	125	0.96	4	100
Layer 4	39	125	0.95	4	100
Layer 5	58	125	0.91	4	100
Layer 6	60	125	0.9	4	100





CMOS Pixel Sensors (CPS): Main features

- **Assets of CPS**
  - Signal processing integrated on sensor substrate
    ⇒ downstream electronics & syst. Integration
  - Standard fabrication process
    ⇒ low cost & easy prototyping, many vendors, …
  - High granularity ⇒ excellent spatial resolution (O(μm))
  - Signal generated in thin (10-40μm) epi-layer
    ⇒ usual thinning up to 50 μm total thickness

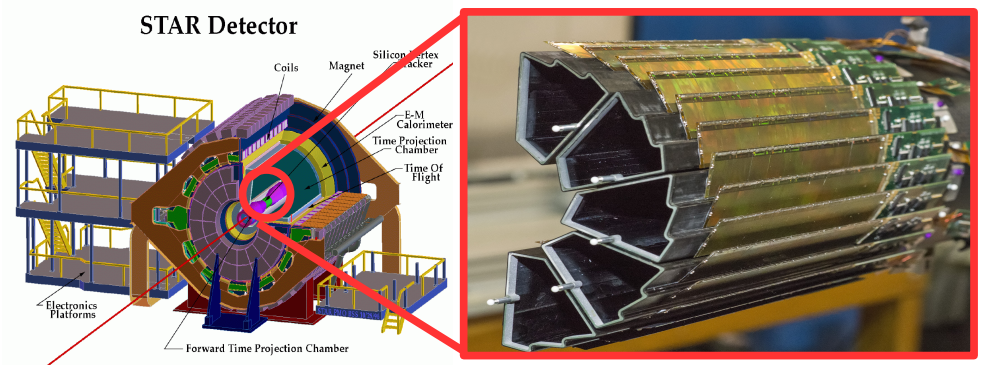


- **Application domain widens continuously** (existing/foreseen/potential)
  - **Heavy-ion collisions**
    - STAR-PXL, ALICE-ITS, CBM-MVD, NA61…
  - **e^+e^- collisions**
    - BES-III, ILC, Belle II (BEAST II)
  - **Non-collider experiments**
    - FIRST, NA63, Mu2e, PANDA, …
  - **High-precision beam-telescopes** (adapted to medium/low energy e^+ beams)
    - Few μm resolution @ DUT achievable with EUDET-BT (DESY), BTF-BT (Frascati)

CPS State-of-the-Art in operation: STAR-PXL detector

STAR-PXL @ RHIC

1st CPS @ a collider experiment !

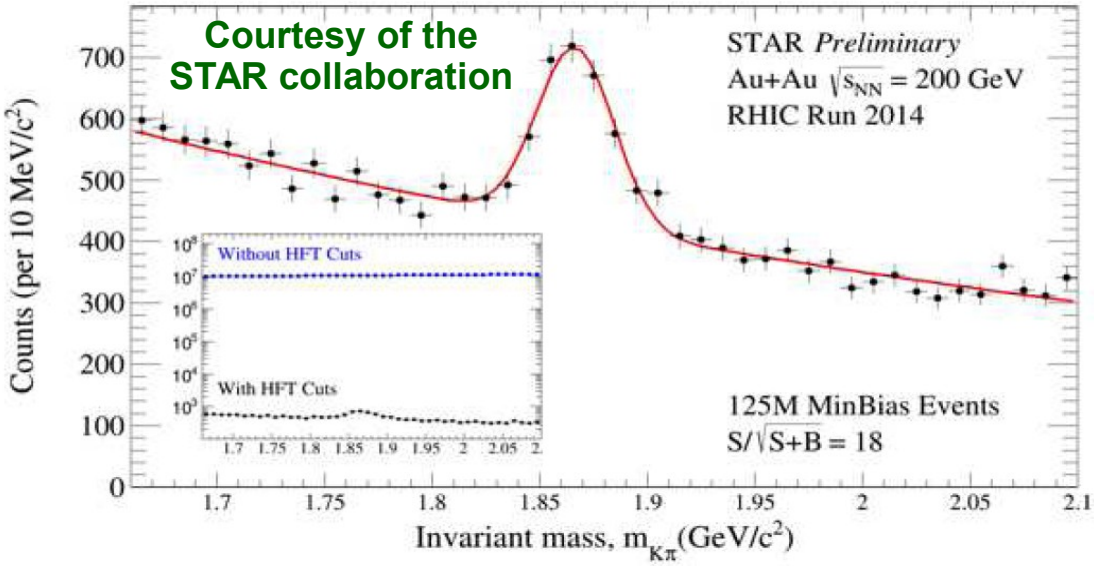


ULTIMATE Sensor (Mimosa28)

- Rolling shutter r.o. ($t_{r.o.} \lesssim 200\ \mu s$)
- $T_{op} = 30 - 35^{o}C$
- $\varepsilon_{det} \gtrsim 99.9\%$ $\sigma_{sp} \gtrsim 3.5\ \mu m$ & $f_{rate} \lesssim 10^{-5}$
- Rad. hard up to 150kRad $\oplus$ $3\times10^{12} n_{eq}/cm^2$

STAR-PXL HALF-BARREL (180M pixels)

- 2 layers @ r = 2.8, 8 cm
- 20 ladders (10 sensors) (0.37% X_0)



Several Physics-runs

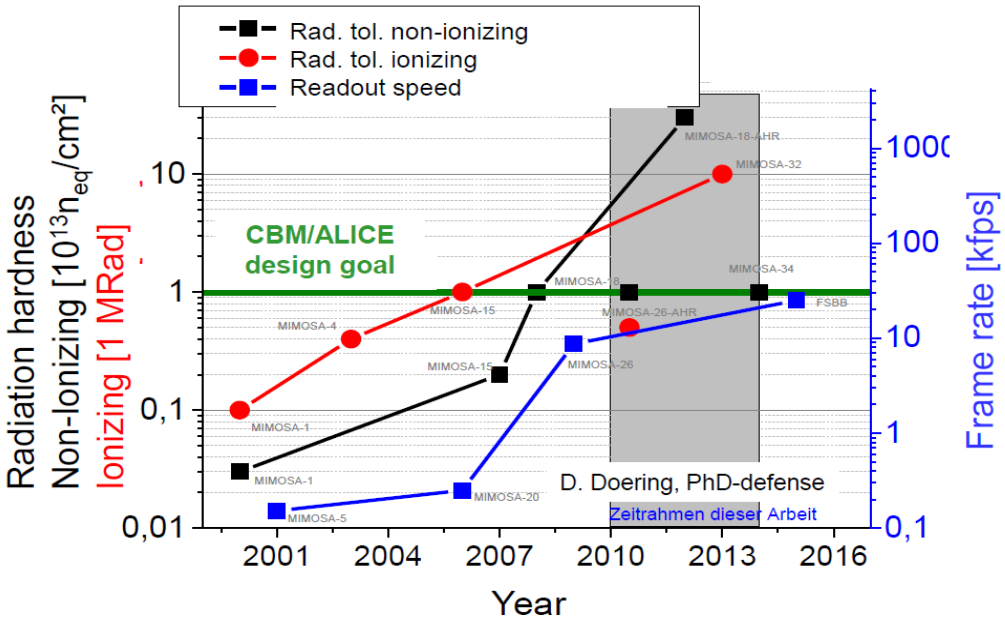
- **1st /2nd run in 2014 & 2015**
- **Preparation for 3rd run (Jan. 2016)**
- **$\sigma_{ip}(p_T)$ matching requirements**

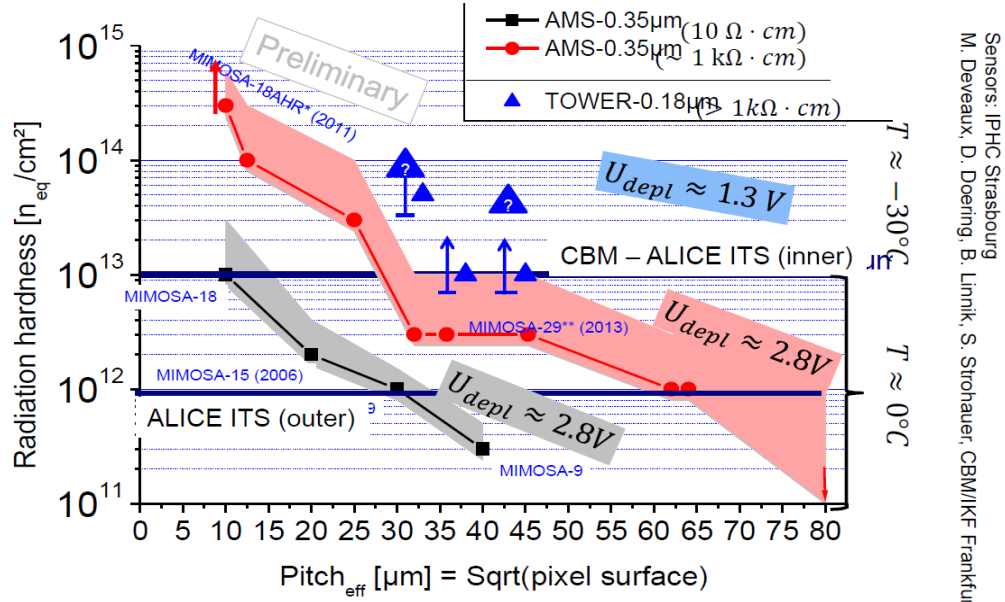
  ~40 μm @ 600 MeV/c for $\pi^{\pm}$/$K^{\pm}$

Observation of D^0 production

- **STAR:** peak significance = 18
- **ALICE:** peak significance = 5

CPS performances: r.o. speed & rad. hardness





Sensors: IPHC Strasbourg
M. Deveaux, D. Doering, B. Linnik, S. Strohauer, CBM/IKF Frankfurt

- **15 years of experience of PICSEL group in developing CPS**
- **Strong collaboration with ADMOS group at Frankfurt**

- **r.o. speed evolution**
  - Two orders of magnitude improvement in 15 years of research

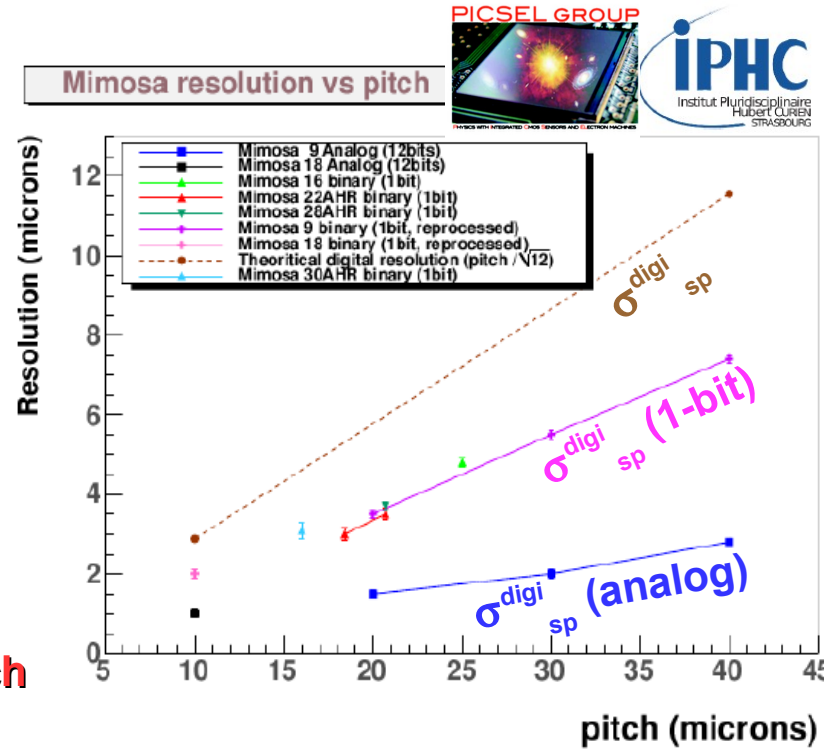
- **Radiation tolerance**
  - Significant improvement with time
  - Validation up to 10MRad ⊕ $10^{14} n_{eq}/cm^2$
  - Adequacy to ALICE-ITS and CBM applications

CPS performances: Spatial Resolution (σ_{sp})

- **Several parameters govern σ_{sp}**
  - **Pixel pitch**
  - **Epi-layer:** thickness & ρ
  - **Sensing node:** geometry & electrical properties
  - **Signal-encoding resolution:** Nb of bits
  - **σ_{sp} function of:**

    pitch ⊕ SNR ⊕ charge-sharing ⊕ ADCu ⊕ ...

- **Pixel-pitch impact (analogue output)**
  - Pitch = 10 (40) μm ⇒ σ_{sp} ~ 1 μm (≲ 3 μm)
  - **Nearly linear improvement in σ_{sp} vs pixel pitch**

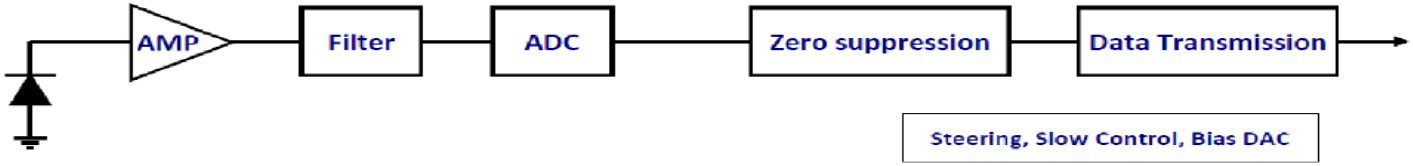


- **Signal-encoding impact (digital output)**
  - σ^{digi}_{sp} = pitch/$(12)^{1/2}$

    ⇒ e.g. σ^{digi}_{sp} ~ 5.7 μm for 20 μm pitch
  - **Significant improvement in σ_{sp} by increasing signal encoding resolution**

Nb of bits	12	3-4	1
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$

ALICE-ITS: Readout chain components

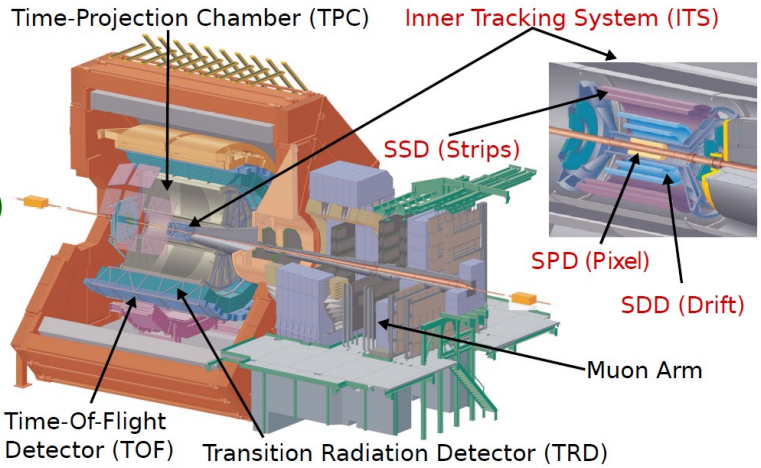


- **Typical readout components**
  - **AMP:** in-pixel low noise pre-amplifier
  - **Filter:** in-pixel filter
  - **ADC** (1-bit ≡ discriminator): may be implemented at end-of-column or pixel level
  - **Zero suppression** (SUZE): only hit pixel info is retained and transferred
    - Implemented at sensor periphery (usual) or inside pixel array
  - **Data transmission:** O(Gbps) link implemented at sensor periphery

- **r.o. alternatives**
  - Rolling shutter (synchronous): || column r.o. reading N-lines at the time (usually N = 1-2)
  - data-driven (asynchronous): only hit pixels are output upon request (priority encoding)

- **Rolling shutter:** best approach for twin-well process
  - Trade-off between performance, design complexity, pixel dimensions, power, …
    e.g.: Mimosa-26 (EUDET-BT), Mimosa-28 (STAR-PXL)

Next challenge: ALICE-ITS upgrade



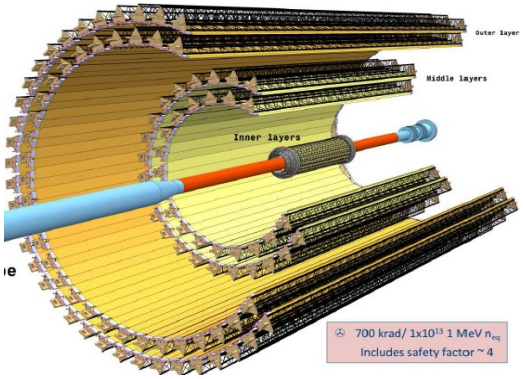
- **Upgraded ITS entirely based on CPS**
  - **Present detector:** 2xHPD/2xDrift-Si/2xSi-strips
  - **Future detector:** 7-layers with CPS (25-30k chips)

    ⇒ 1st large tracker (~ 10 m^2) using CPS
  - ITS-TDR approved on March 2014

    (Pub. In J.Phys. G41 (2014) 087002)

- **New ALICE-ITS requirements**

	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4\ \mu m$	$< 200\ \mu s$	150 kRad	$3 \cdot 10^{12}$ n_{eq}/cm^2	30-35°C	160 mW/cm^2	0.15 m^2
ITS-in	$\lesssim 5\ \mu m$	$\lesssim 30\ \mu s$	2.7 MRad	$1.7 \cdot 10^{13}$ n_{eq}/cm^2	30°C	$<$ 300 mW/cm^2	0.17 m^2
ITS-out	$\lesssim 10\ \mu m$	$\lesssim 30\ \mu s$	100 kRad	$1 \cdot 10^{12}$ n_{eq}/cm^2	30°C	$<$ 100 mW/cm^2	$\sim$ 10 m^2

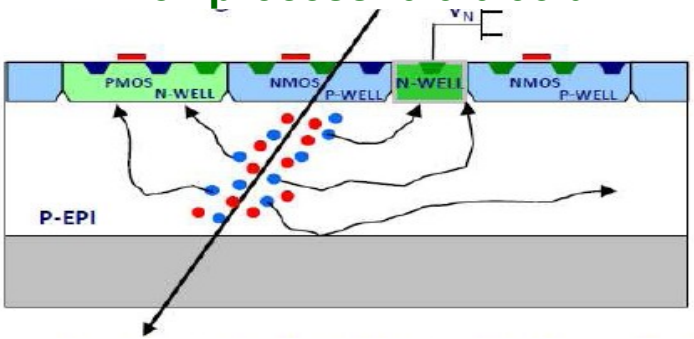


- **Different requirements on inner & outer layers calls for different chips designs!**

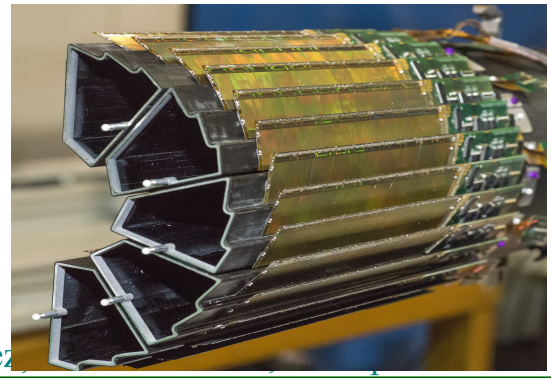
⇒ **0.35 µm CMOS process (STAR-PXL) marginally suited to this r.o. speed & rad. hardness**

CMOS Process Transition: STAR-PXL → ALICE-ITS

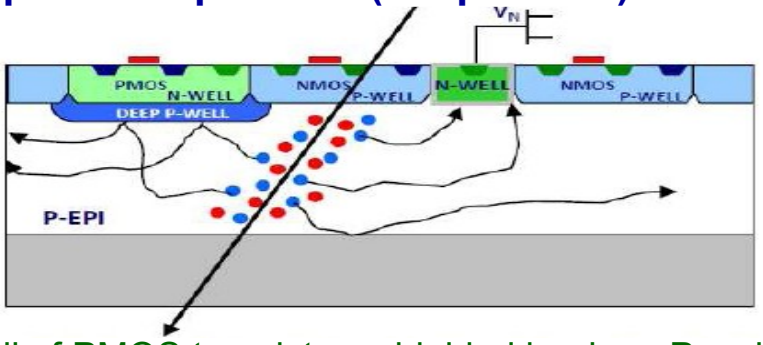
Twin well process: 0.6-0.35 um



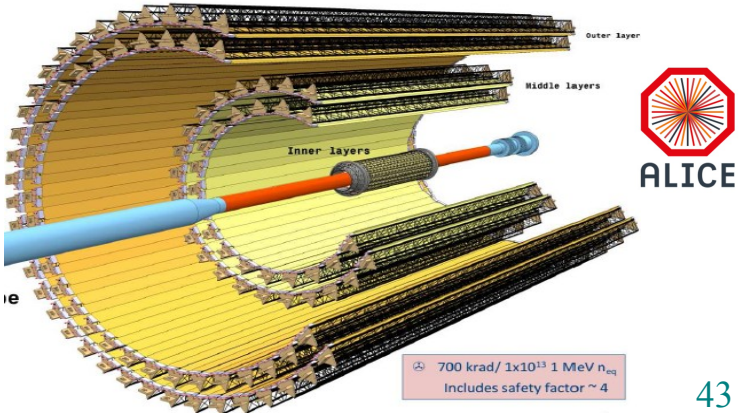
- PMOS in pixel array not allowed
  ⇒ parasitic q-collection of additional N-well
- Limits choice of readout architecture strategy
- Already demonstrated excellent performances
  - **STAR-PXL:** Mi-28 (AMS 0.35 μm process)
    ⇒ ε_{det} > 99.5%, σ_{sp} < 4μm
  - 1st CPS detector @ collider experiment



Quadrupole well process (deep P-well): 0.18 um



- N-well of PMOS transistors shielded by deep P-well
  ⇒ both types of transistors can be used
- Widens choice of readout architecture strategies
  - **New ALICE-ITS:** 2 sensors R&D in || using TowerJazz CIS 0.18 um process (quadru. well)
    - **Synchronous Readout R&D:**
      proven architecture ⇒ safety
    - **Asynchronous Readout R&D:** challenging

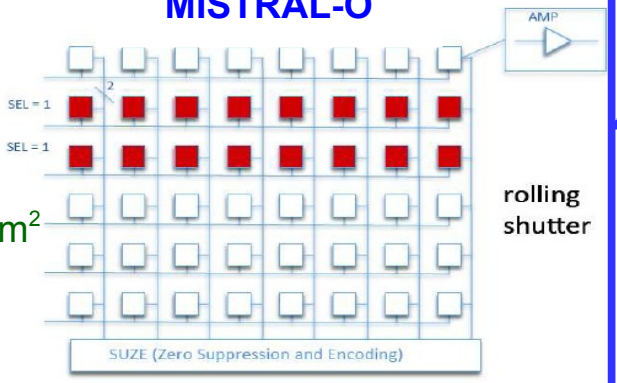


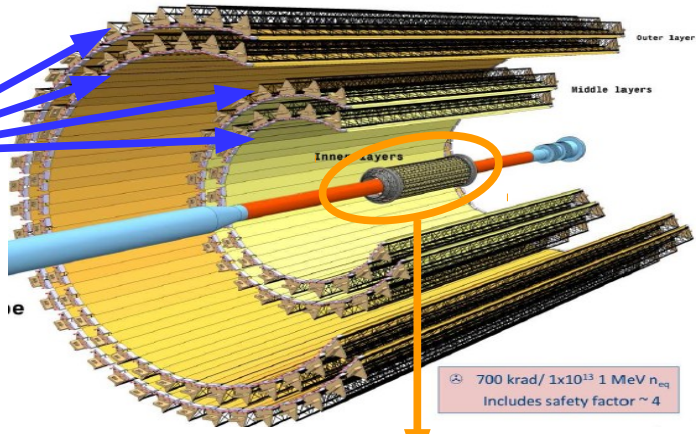
ALICE-ITS: Two Architectures for the pixel chip

PICSEL GROUP

MISTRAL-O

Pixel pitch: 36x64 µm²
Time resolution: ~ 20 µs
W: 80 mW/cm²
Max hit rate: ~0.8 MHz/cm²
Dimension: 15 x30 mm²
Dead area: 1.5x30 mm²

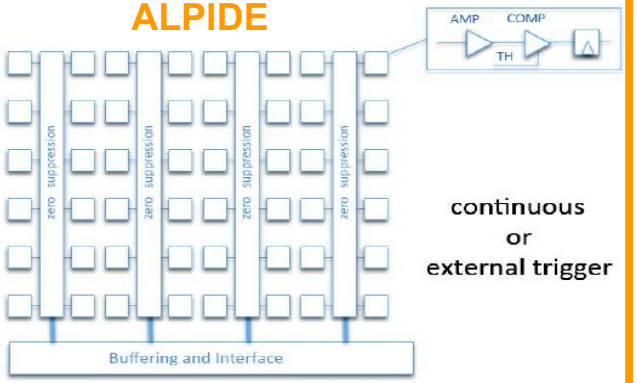




Goal: early available and reliable solution

- **Conservative design based on STAR-PXL**
- Big pixel ⇒ low power & high speed
- Moderate rad. hardness & σ_{sp} ~10 µs ⇒ OK

ALPIDE



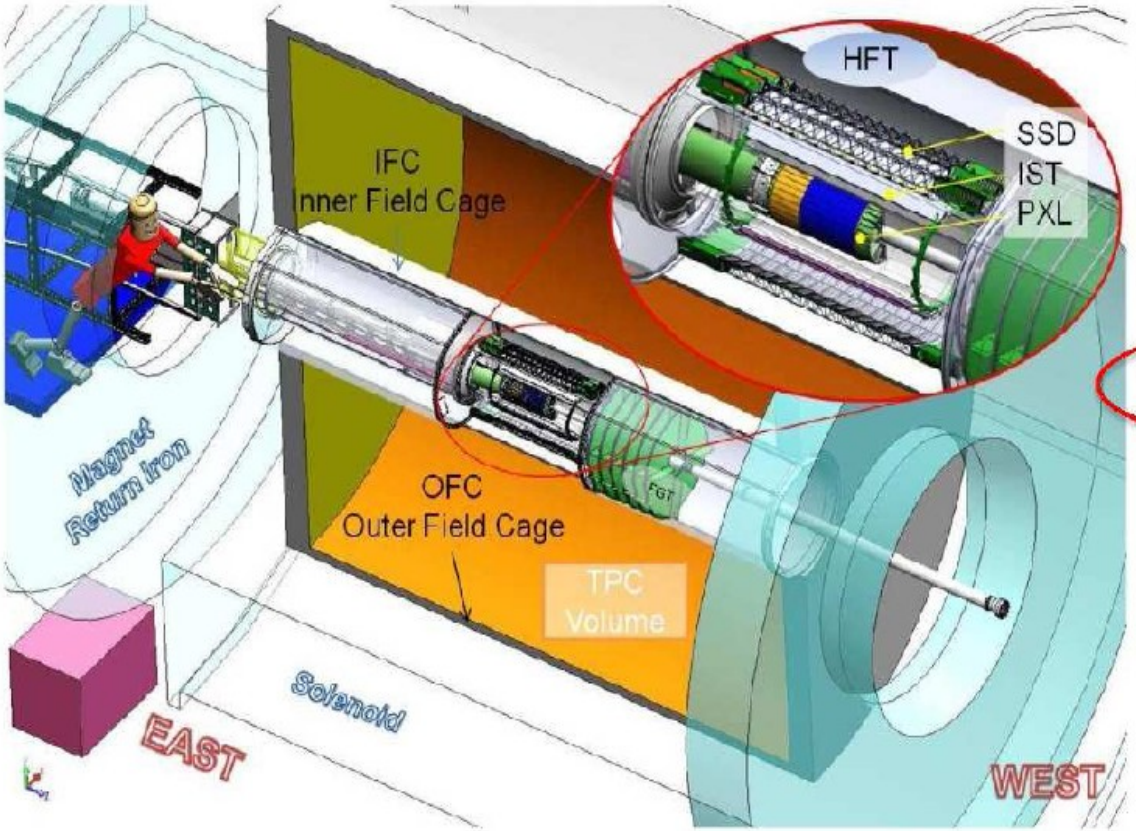
Pixel pitch: 28x28 µm²
Time resolution: ≲ 5 µs
W: 39 mW/cm²
Max hit rate: ~ 3MHz/cm²
Dimension: 15 x30 mm²
Dead area: 1.1x30 mm²

Goal: high performance, accept risks

- **Aggressive design**
- In-pixel discrimination
- Data-driven r.o. (priority encoder)

- **Both chips have same physical & electrical interfaces**
- **Base-line solution: ALPIDE for all ITS layers**

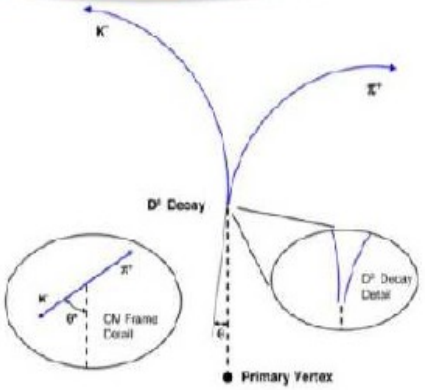
PXL in STAR Inner Detector Upgrades



TPC – Time Projection Chamber
(main tracking detector in STAR)

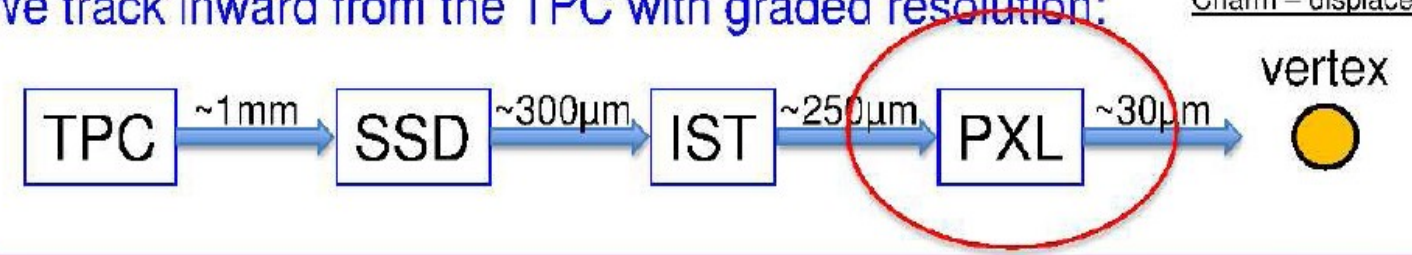
HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
  - r = 22 cm
- IST – Inner Silicon Tracker
  - r = 14 cm
- PXL – Pixel Detector
  - r = 2.8, 8 cm



Direct topological reconstruction of
Charm – displaced verticies

We track inward from the TPC with graded resolution:

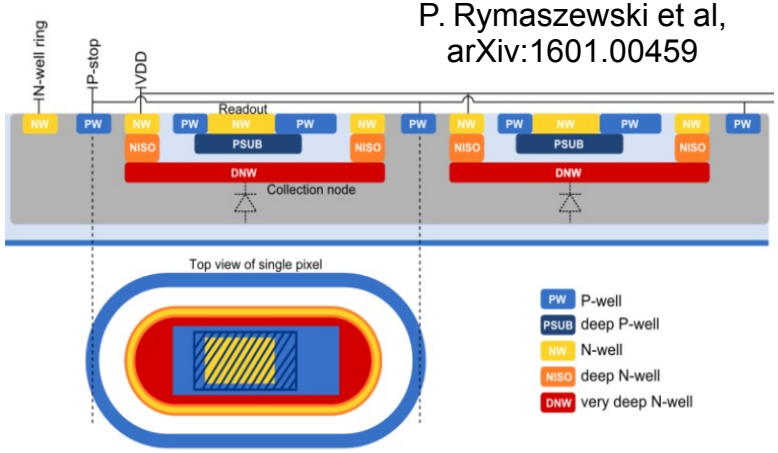


L. Greiner
(CPIX-14)

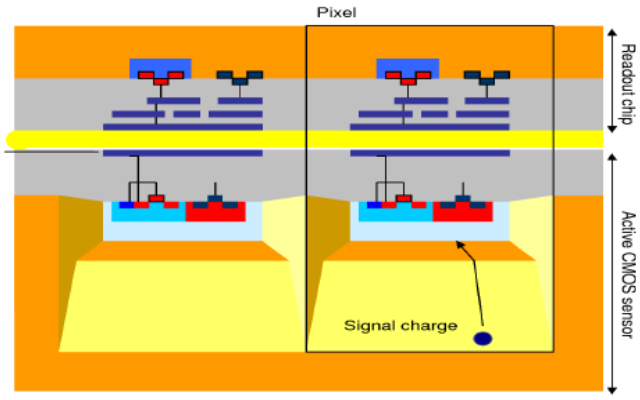
Technology Perspectives for Performance Improvements

- **HV/HR-CMOS sensors:** $d_{dep} \sim 0.3 \sqrt{\rho_{sub} \times U_{bias}}$
  - Extend sensitive volume & improved q-collection
    ⇒ Faster signal & stronger rad. tolerance
  - Not bound to CMOS processes using epi-layers
    - Easier access to VDSM (< 100 nm) process
    - Higher in-pixel μ-circuitry density
  - Unanswered questions
    - Minimal pixel dimensions (σ_{sp}) ?
    - Uniformity over large sensitive area & production yield?

P. Rymaszewski et al, arXiv:1601.00459



- **2-tiers chips**
  - Signal sensing (front-end) & processing (r.o.) parts distributed over two interconnected tiers (AC coupling)
  - Smart sensor ⇒ 1 r.o. pixel addressing N pixel-front-ends
    ⇒ Reduce density of interconnections
  - Can combine 2 diff. CMOS processes: front-end/r.o.
  - **Benefits:** small pixels ⇒ resolution, speed, data-compression and robustness
  - **Challenges:** interconnection technology (reliability & cost)

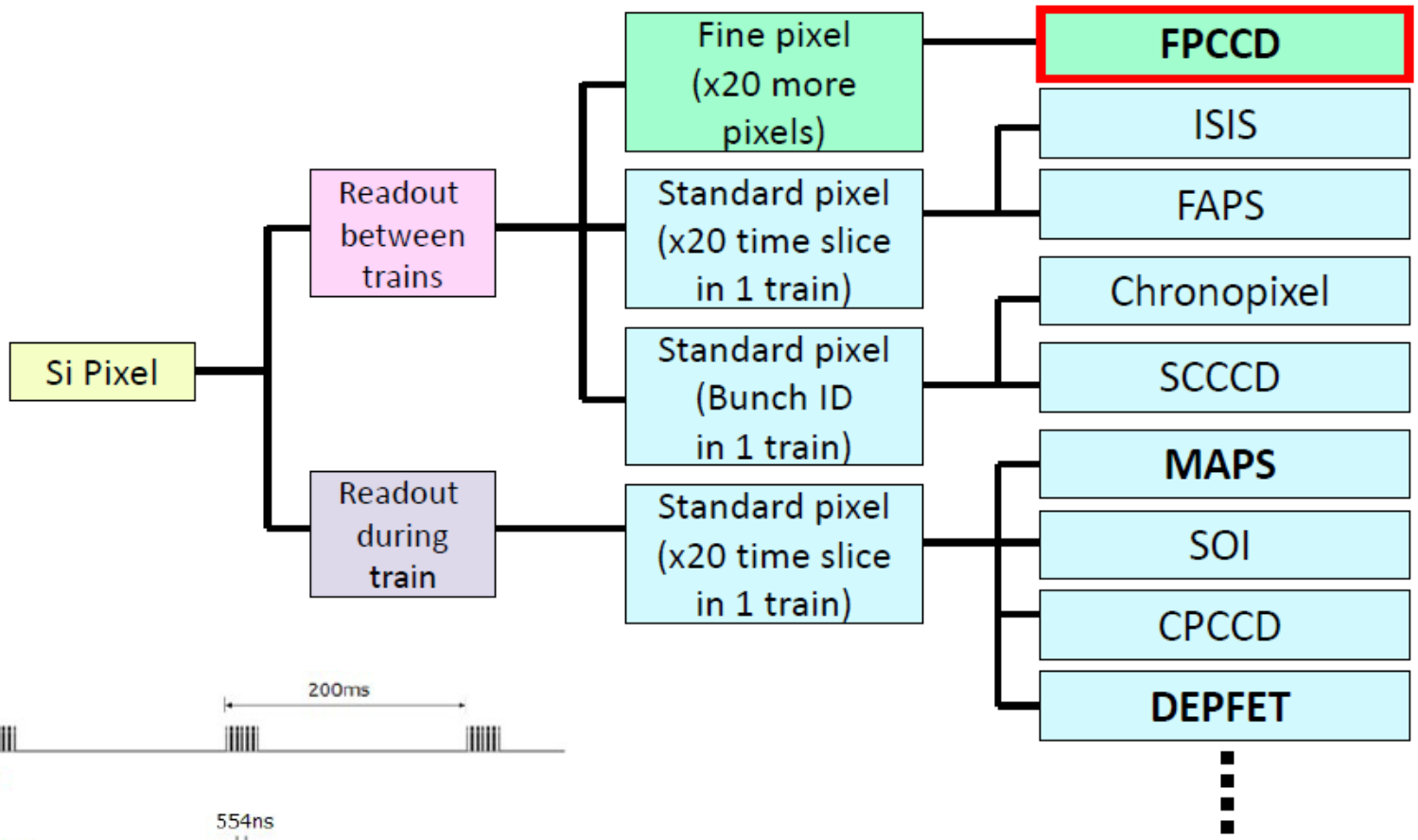


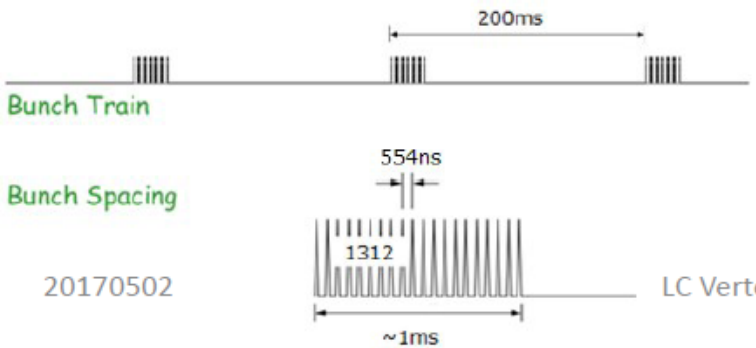
Ivan Peric: CPIX14, Bonn, 2014

Y. Sugimoto (KEK)

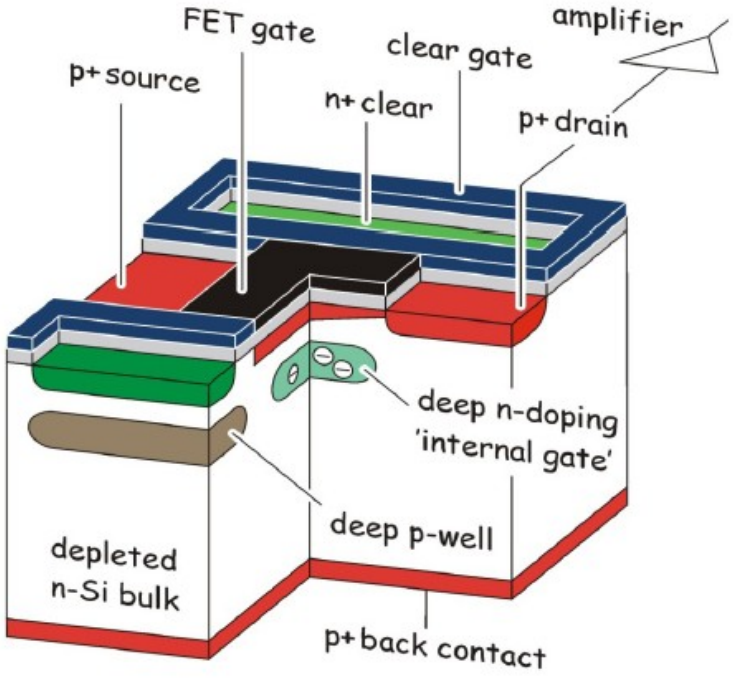
Sensor technologies

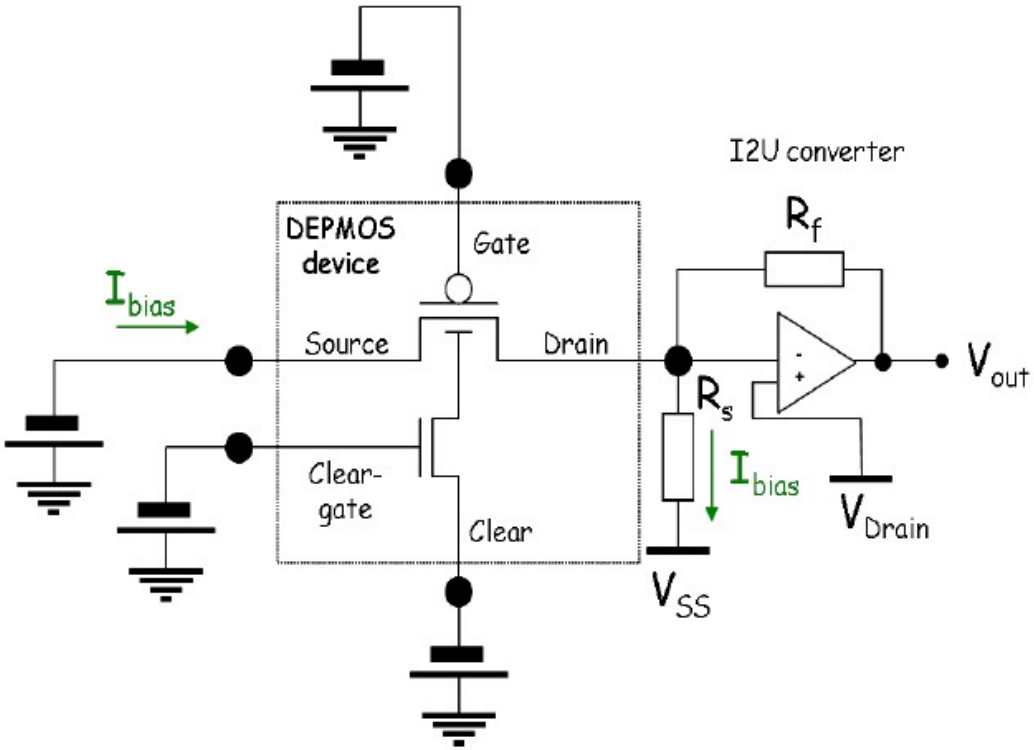
- Technologies proposed so far





DEPFET Active Pixels





DEPFET all-silicon module for Belle II

DCDB (Drain Current Digitizer)

Analog front-end

Amplification and digitization of DEPFET signals.

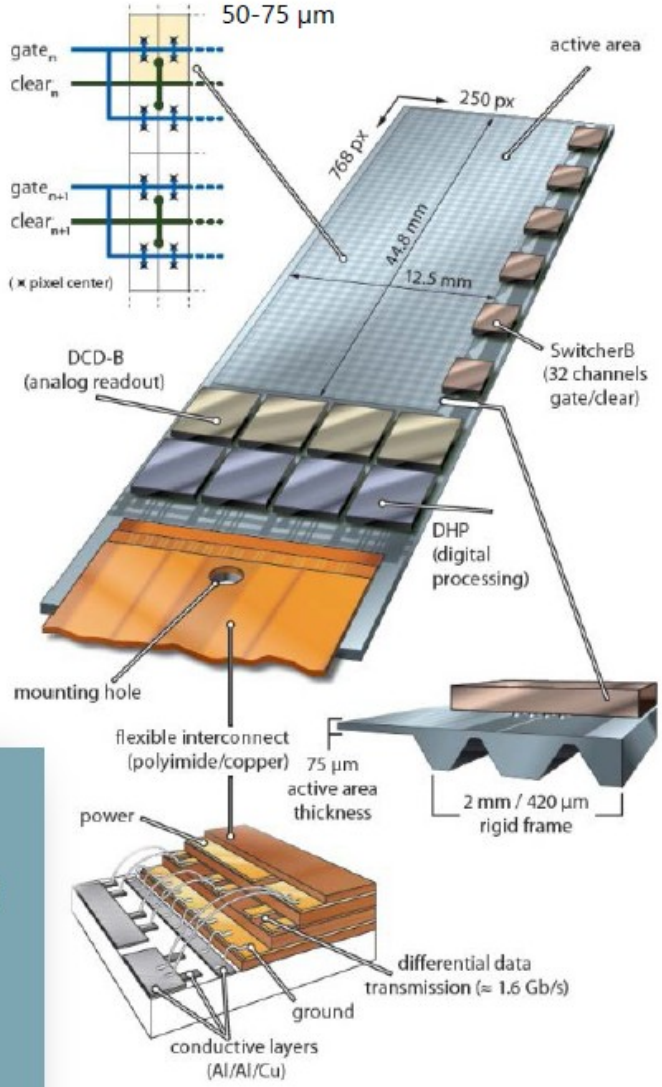
256 input channels

8-bit ADC per channel

92 ns sampling time

UMC 180 nm

Rad hard design



Key to low mass vertex detectors

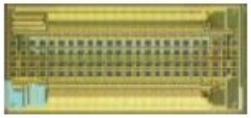
→ MCMs w/ highest possible integration!

↳ Thin sensor area

↳ EOS for r/o ASICs

↳ Thin (perforated) frame w/ steering ASICs

SwitcherB - Row Control



AMS/IBM HVCMOS 180 nm

Size 3.6 × 1.5 mm^2

Gate and Clear signal

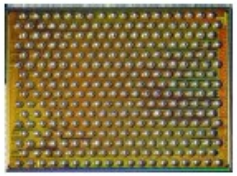
32x2 channels

Fast HV ramp for Clear

Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)

First data compression



TSMC 65 nm

Size 4.0 × 3.2 mm^2

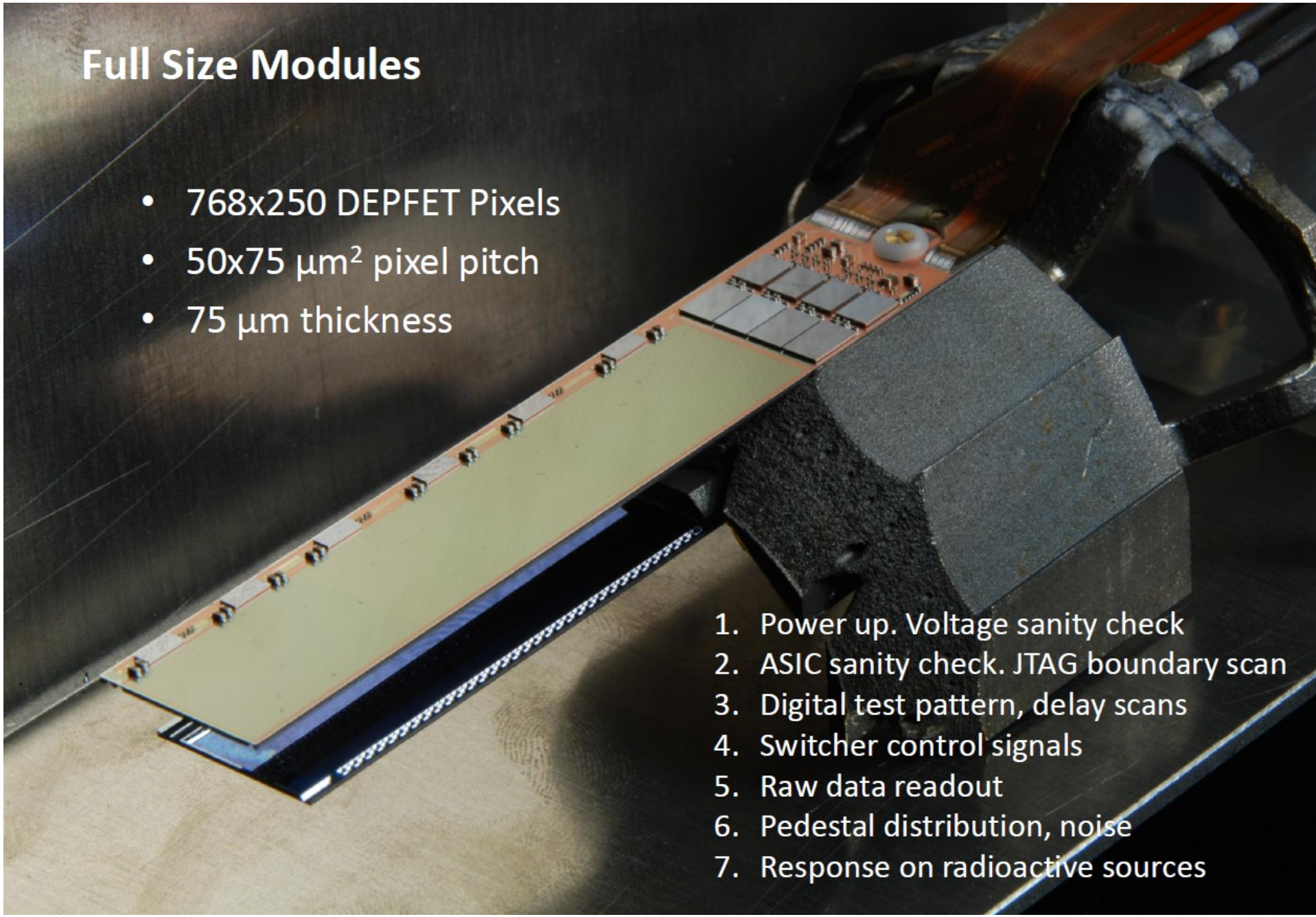
Stores raw data and pedestals

Common mode and pedestal correction

Data reduction (zero suppression)

Timing and trigger control

Rad. Hard proved (100 Mrad)


Full Size Modules
• 768x250 DEPFET Pixels
• 50x75 µm² pixel pitch
• 75 µm thickness
1. Power up. Voltage sanity check
2. ASIC sanity check. JTAG boundary scan
3. Digital test pattern, delay scans
4. Switcher control signals
5. Raw data readout
6. Pedestal distribution, noise
7. Response on radioactive sources

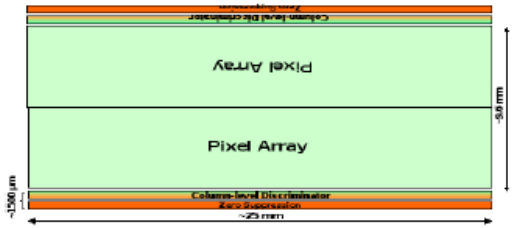
CMOS Pixel Sensors for the ILD-VXD (2/2)

- **From the STAR-PXL to the ILC-VXD :**

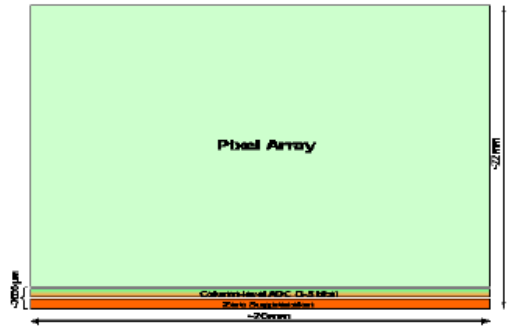
Detector	σ_{sp}	t_{int}	Dose (30°C)	Fluence (30°C)
STAR-PXL	$\gtrsim 3.5\ \mu m$	190 μs	150 kRad	$3{\cdot}10^{12}$ n_{eq}/cm^2
ILD-VXD/In	$< 3\ \mu m$	50/10 μs	< 100 kRad	$\lesssim 10^{11}$ n_{eq}/cm^2
ILD-VXD/Out	$\lesssim 4\ \mu m$	100 μs	< 10 kRad	$\lesssim 10^{10}$ n_{eq}/cm^2

- **Final "500 GeV" CPS prototypes :** fab. in Winter 2011/12 **(0.35 μm process for economic reasons)**

  - **MIMOSA-30:** inner layer prototype with 2-sided read-out
    - ↪ one side : 256 pixels ($16\times16\ \mu m^2$)
      other side : 64 pixels ($16\times64\ \mu m^2$)



  - **MIMOSA-31:** outer layer prototype
    - ↪ 48 col. of 64 pixels ($35\times35\ \mu m^2$)
      ended with 4-bit ADC

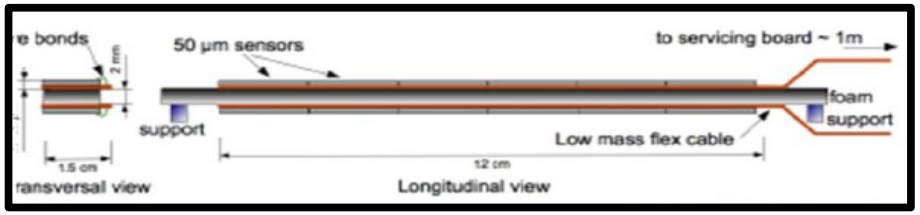


Potential of MIMOSIS

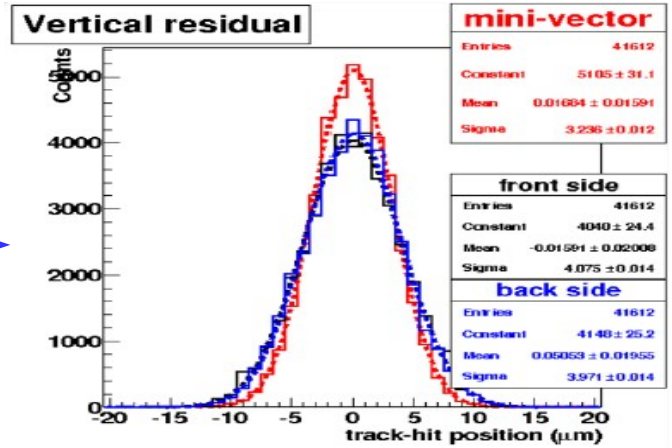
- **Extension of MIMOSIS to an ILC vertex detector**
  - Reoptimise trade-off between requirements (relax rad. tolerance & hit rate capability)
  - Shrink pixel dimensions to minimum
  - Reshuffle read-out structure
  - Translate to smaller feature size: TowerJazz 110/180 nm, 150 or 130 nm technologies
- **Sensor target performances:**
  - Spatial resolution $\lesssim 4\ \mu m$
  - Time resolution $\sim$ 2–4 μs
  - Non-sensitive side-band width reduced $to\sim$ 1 mm
- **MIMOSIS prototyping (1 MPW, 3 ER until 2020) allows for ILC prototyping**

Sensor Integration in Ultra-Light devices

- **PLUME collaboration (Britol, DESY, IPHC)**

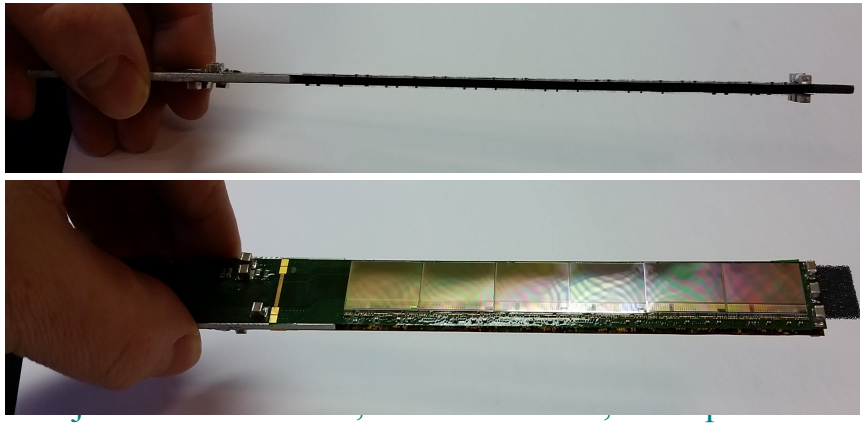


- **Plume 01 prototype** (fabricated in 2012)
  - 2x6 Mi26 sensors on 2 mm thick foam SiC (0.6% X_0)
  - Air cooling
  - Validated in beam @ CERN (2011)
  - New test-beam @ DESY in April 2016



- **Plume 02 prototype:** 6 ladders for 2016
  - Reduced material budget: → 0.35/0.42 % X_0 (Al/Cu flex PCB)

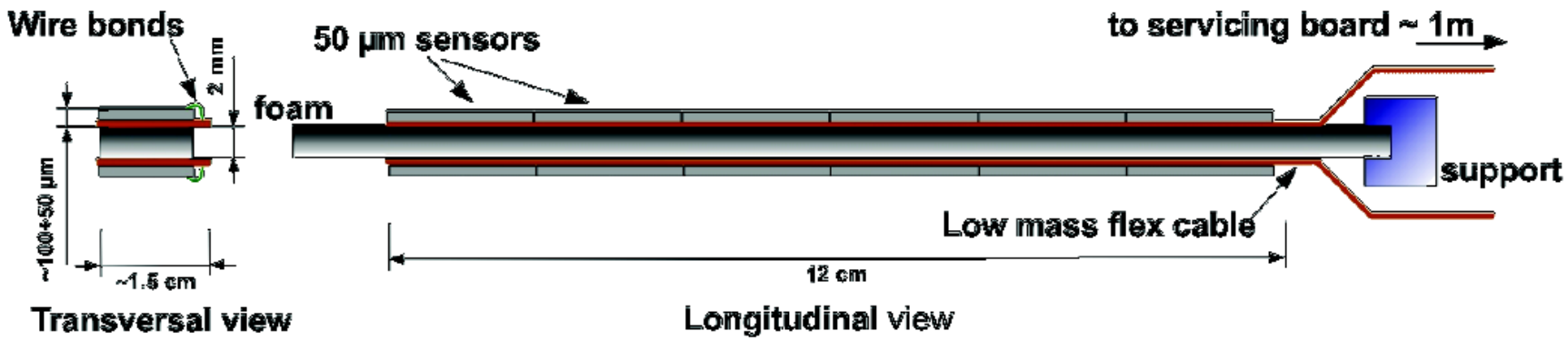
Plume 02 fully functional prototype



Application outside ILC

- Beam-bkg measurement @ Belle II
- 2 Plume 02 ladders will be installed inside Belle II inner volume in 2017
- FOOT

Design concepts: PLUME

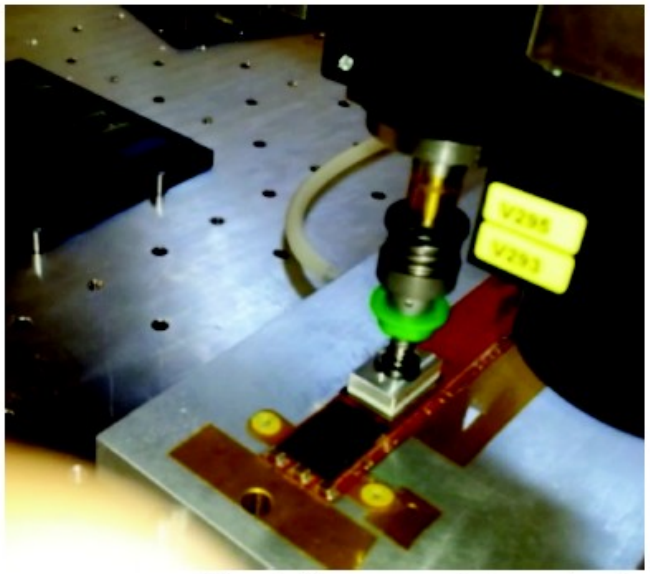


- PLUME initial choices
  - Double-sided
  - Thinned ensors (50 µm)
    - Start with a CPS → might change if other options available
    - MIMOSA-26: single point resolution 3 µm, integration time 115 µs
  - Spacer
    - Silicon Carbide foam, 2 mm thickness, few % density
  - Air cooling
    - Sensor to sit on top
  - Sensitive length 125 mm → 6 MIMOSA-26 per side
  - Connexions with wire bonding

Design Concepts: assembly

- Step 1
  - Aligning & gluing sensors to FPCs
  - Automatic placement machine
- Step 2
  - Wire bonding on individual FPCs

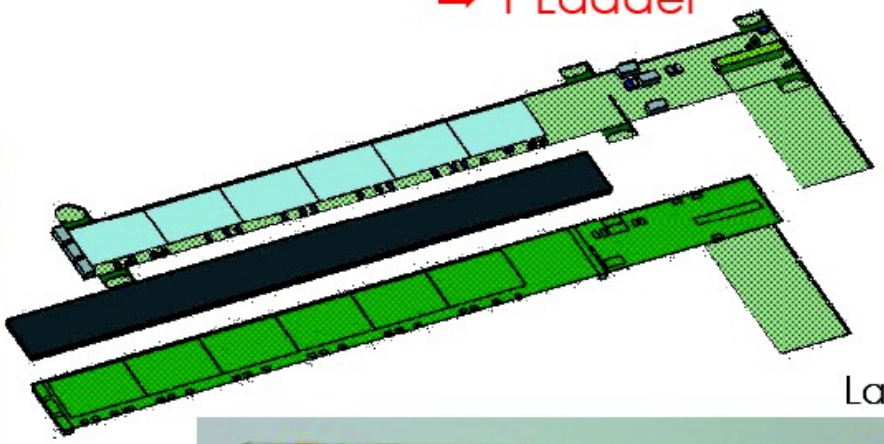
➡ 2 Modules



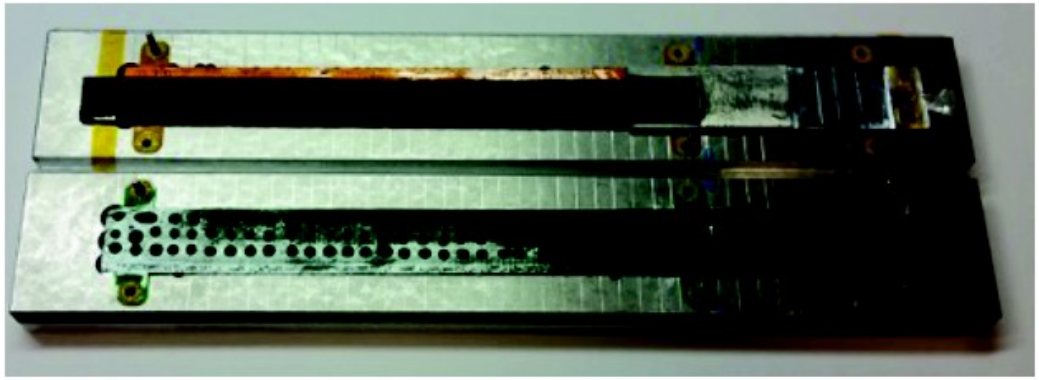
Module assembly robot

- Step 3
  - Gluing 2 modules simultaneously on both sides of a SiC foam
  - Manually with a dedicated jigs

➡ 1 Ladder

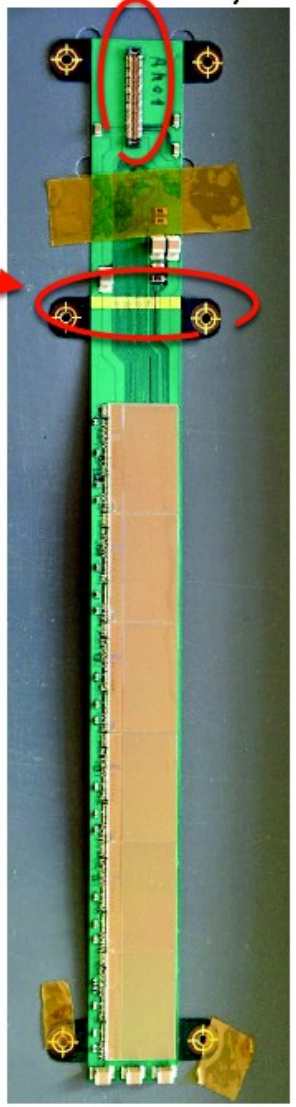


Ladder assembly jigs

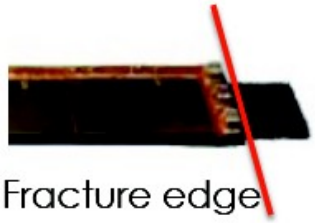


Outputs of PLUME-2

- **Aluminium FPC more fragile**
  - Quality of metal traces OK in sensor area
  - BUT SMD connector mounting badly reliable
    - All 4 Al modules have unstable connexion
  - Possible fix:
    - use bonding to connect cable to outside
    - Probable impact on ladder assembly → still not yet done



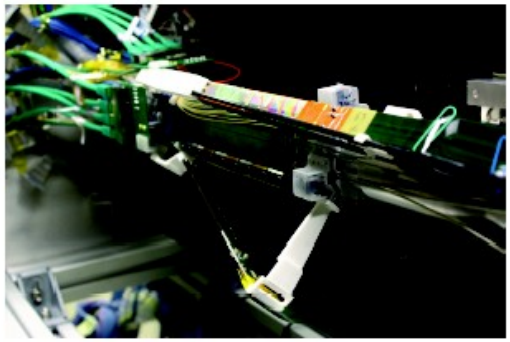
- **Narrow 4% SiC foam is brittle**
  - Need extra-car / transportation
    - Two proto-ladders had the part sticking out for support broken

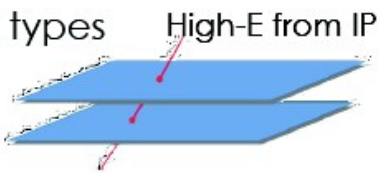


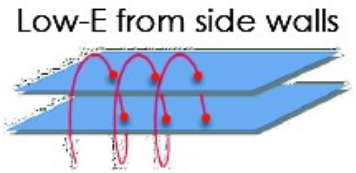
- **Tests with Cu version**
  - Only in-lab characterization so far
    - No suspicious behaviour
  - Metrology survey / deformation
    - In preparation at Bristol/Oxford
  - Beam tests @ DESY 2017/18
  - Test in a collider (SuperKEKB) in 2018

PLUME outside ILC

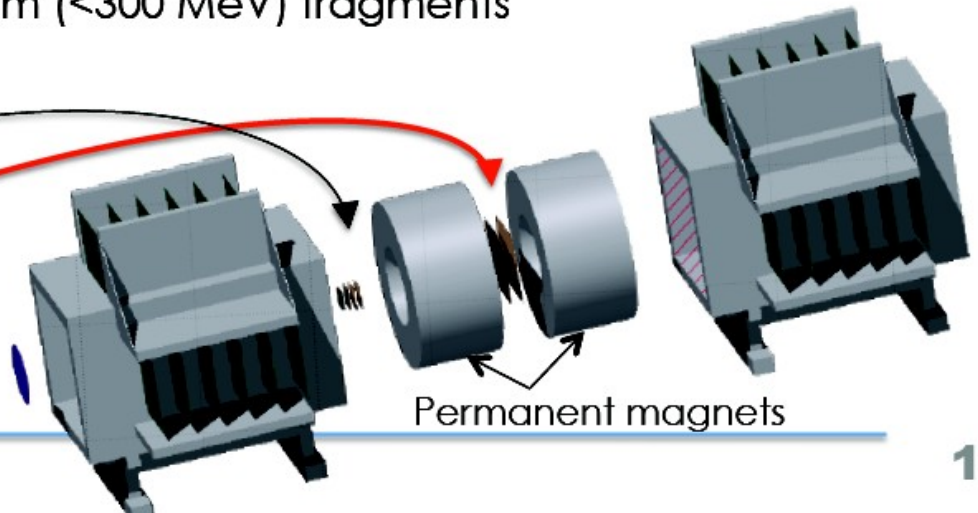
- **Beam-induced background @ SuperKEKB**
  - BEAST II will measure up to 1×10^{34} cm^2/s^{-1}
    - dedicated setup PRIOR the final Belle II full vertex detector
    - Feb-Jun 2018 = data taking
  - 2 PLUME-2 ladders at various radius and angles
    - Assess hit rate online
    - Exploit 2-sided info to recognize bkgrnd types







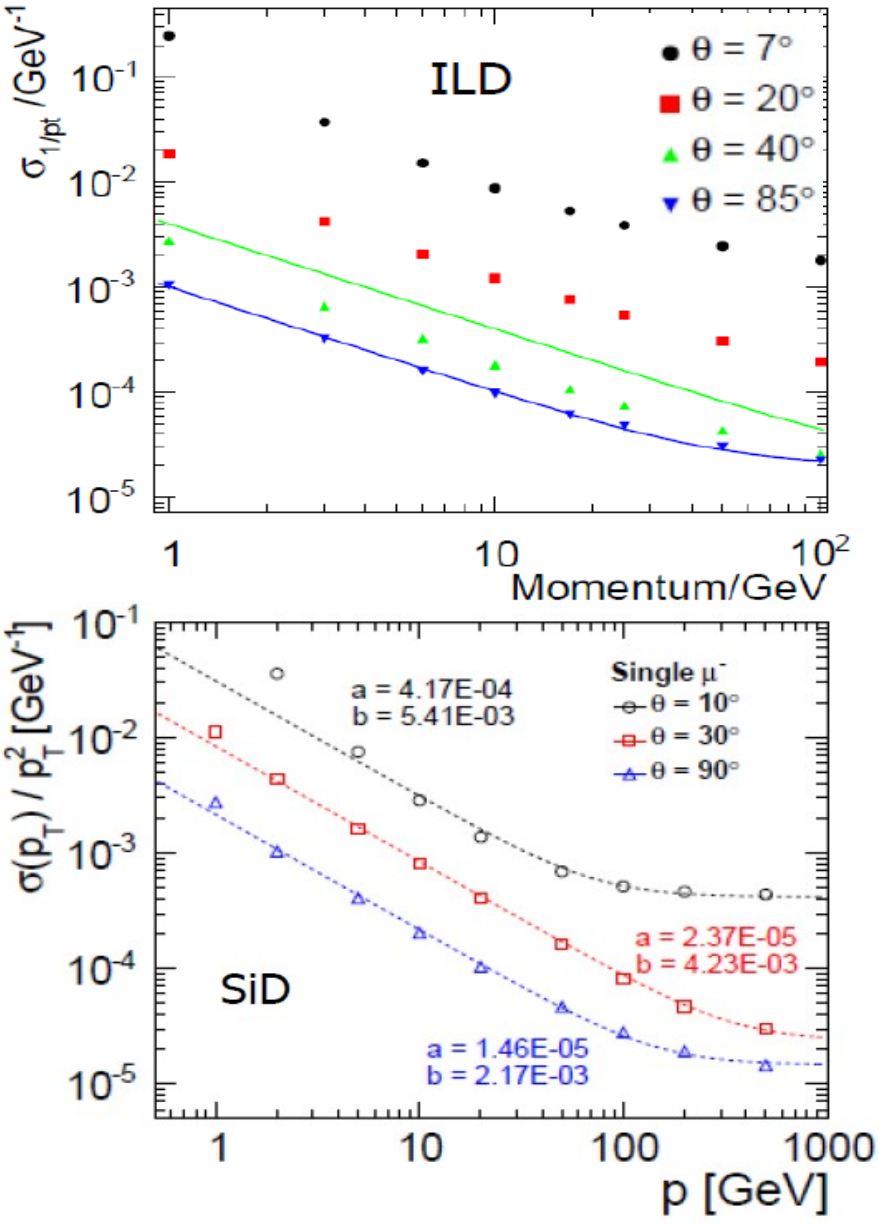
- **FOOT (INFN) project**
  - Measures nuclear fragmentation of interest for hadrontherapy
    - 2017: final design, 2018: final approval, 2020: data taking
  - Need tracker for low momentum (<300 MeV) fragments
    - Requirement $\sigma_p/p \sim 3\%$
  - Tracker in 2 parts
    - 1st station = individual sensors
    - 2nd station = 8x8 cm^2 = 4 new PLUME-type ladders (exploit MIMOSA-28)
    - Design with LNF (E. Spiriti)



ILC Tracking system expected performances: p_T resolution

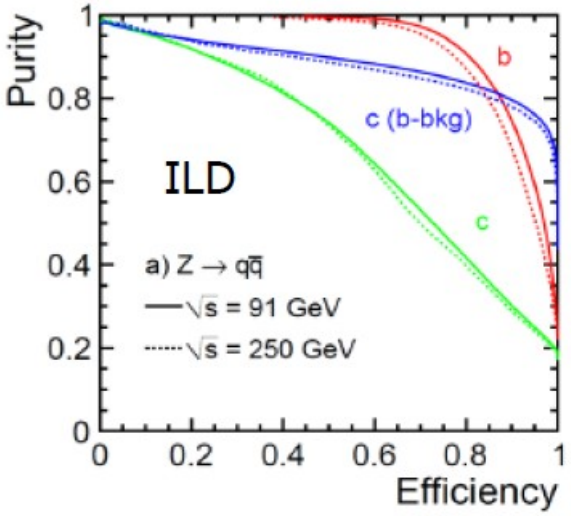
- **Results from full simulation single muon particle gun**
  - Empirical parametrization

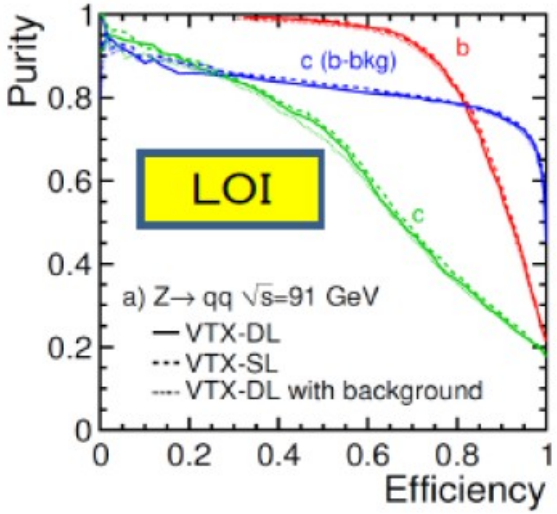
    $\sigma(1/p_T)$ a $\oplus$ b/p_T sinθ GeV^{-1}
  - SiD
    - a = (2 – 4)×10^{-5}, b = (2 – 5)×10^{-3}
    - Better @ high p_T
    - Robustness in high density track environment
  - ILD
    - a = ~2×10^{-5}, b ~ 1×10^{-3}
    - Better @ low p_T
    - dE/dx capabilities (TPC)

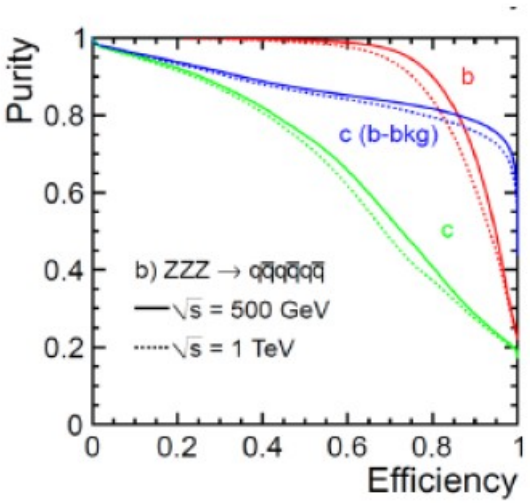


ILC Tracking system expected performances: Flavour tagging

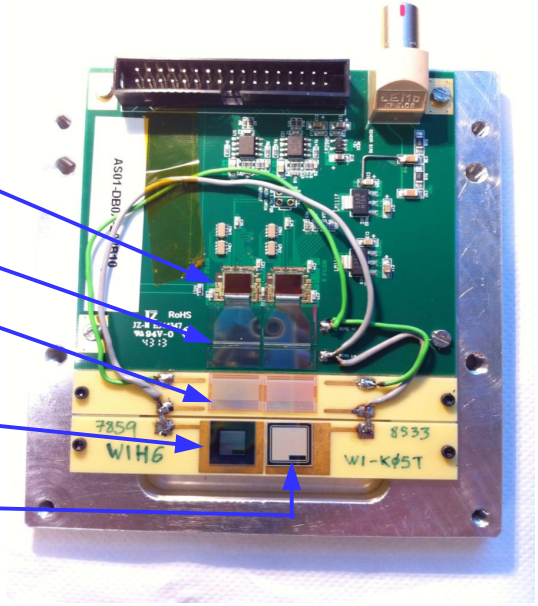
- ILD example
- Full simulation
- Multi-variable tagging algorithm (BDT)
  - LCFIplus
- Continuous improvements







I-LGAD: Test beam results

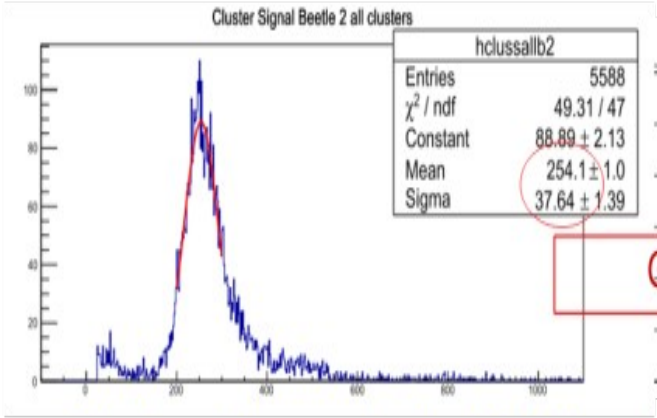


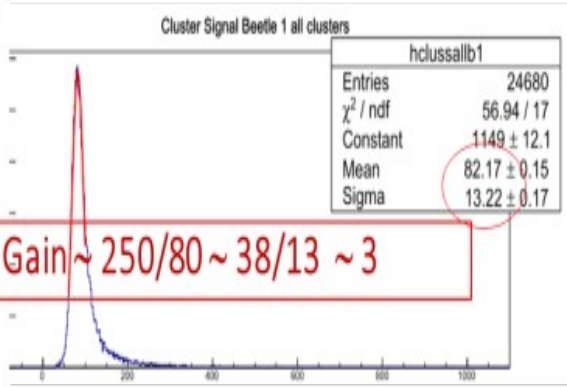
I-LGAD

(Room temp. 400 Volts)

Standard Strip

(Room temp. 200 Volts)





Cluster Charge (arb. Units)

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