# Upgrade of the ATLAS hadronic Tile Calorimeter for the High luminosity LHC

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On behalf of the ATLAS Tile Calorimeter System

Calorimeters for the High Energy Frontier 2017
Lyon, France. 2-6 October

Supported by the Spanish MINECO and the European Regional Development Fund (ERDF), grant FPA2015-65652-C4-2-R (MINECO/FEDER)

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- LHC and ATLAS
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- Upgrade Phase II
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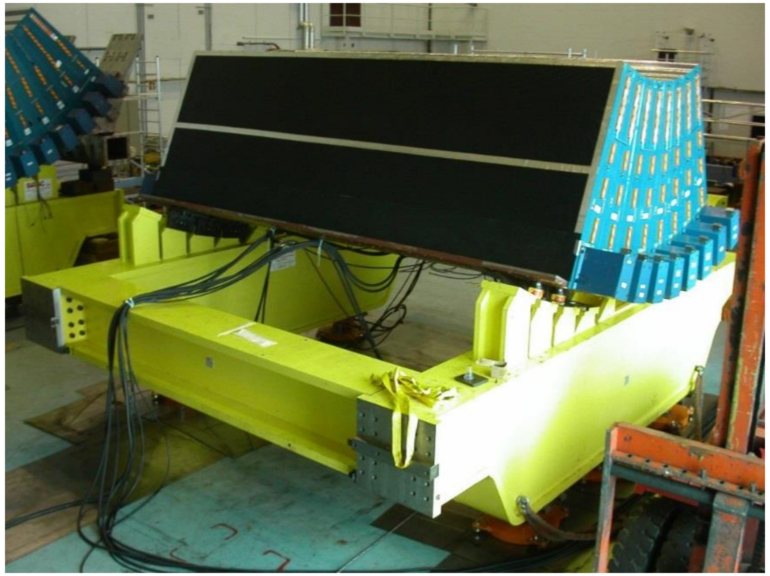
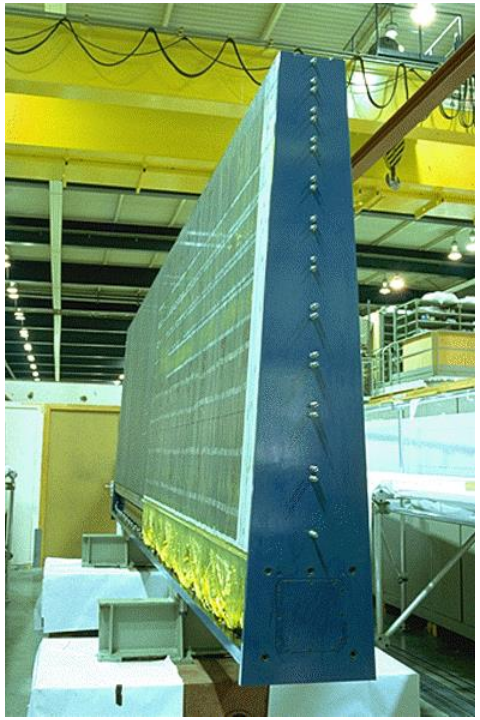
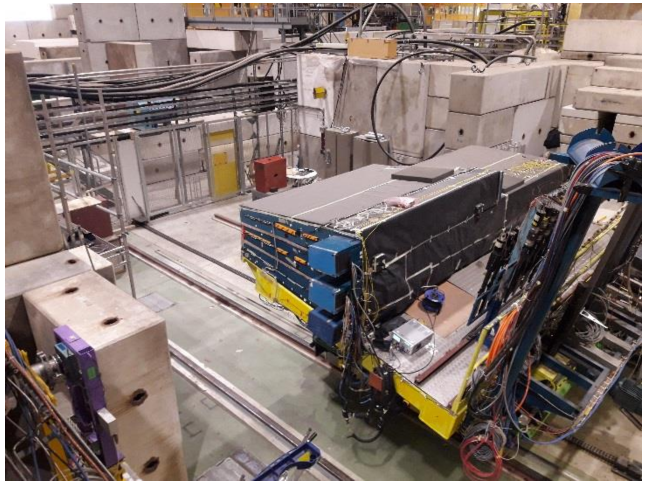
  - Objectives
  - Results





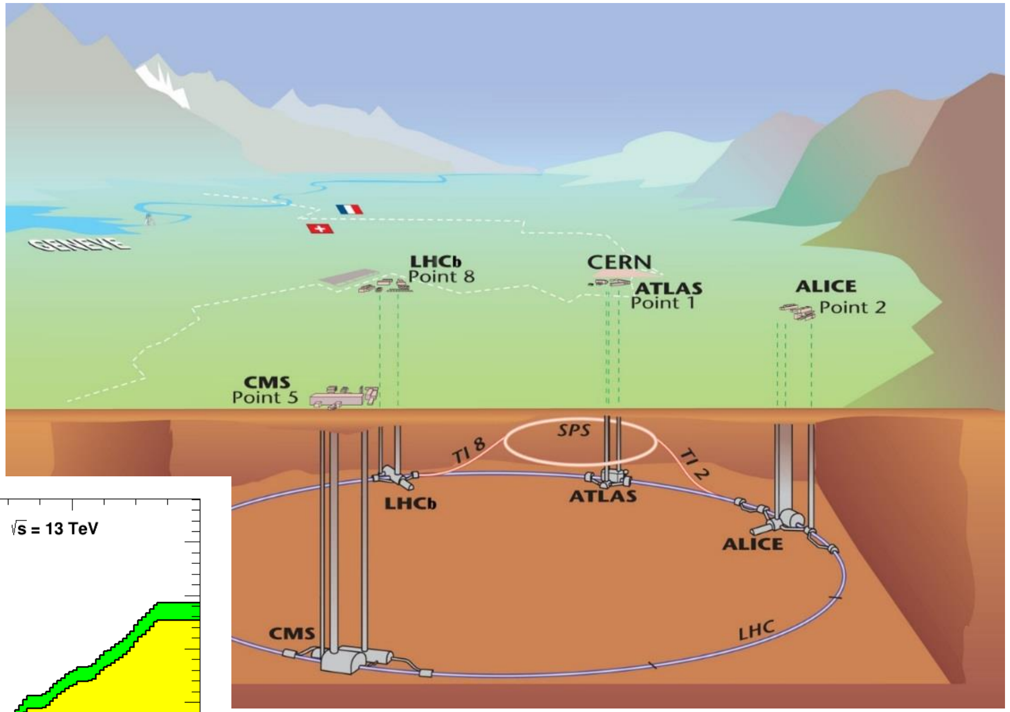


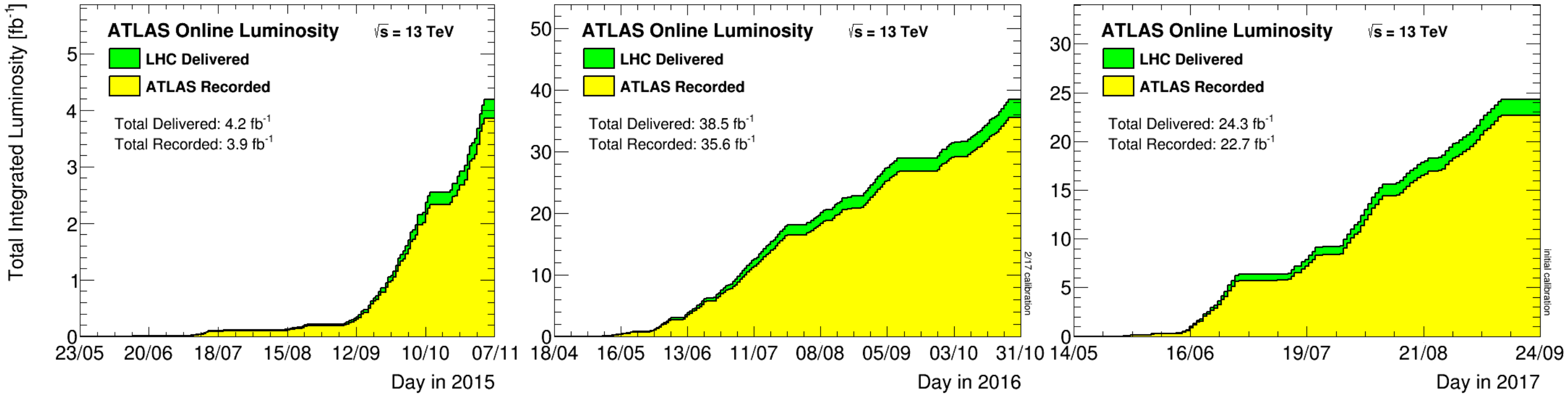
# Introduction: LHC

The largest particles collider in the world is the Large Hadron Collider situated in the French-Swiss border near Geneva. The LHC is an accelerator ring of a circumference of 27 Km, designed to collide two proton beams with a center of mass energy of 14 TeV, located 100 meters underground. At nominal luminosity is of $10^{34}$ cm $^{-2}$ s $^{-1}$, the bunch spacing is 25 ns( $\sim$7 m) and each bunch contains about $10^{11}$ protons.

For Run-2:

- Center of mass energy: $\sqrt{s} = 13$ TeV
- Number of bunches: 2808 bunches
- Bunch space: 25 ns
- Total recorded luminosity : ≈62 fb $^{-1}$
- Record instantaneous luminosity: $17.4 \cdot 10^{33}$ cm$^{-2}$ s$^{-1}$

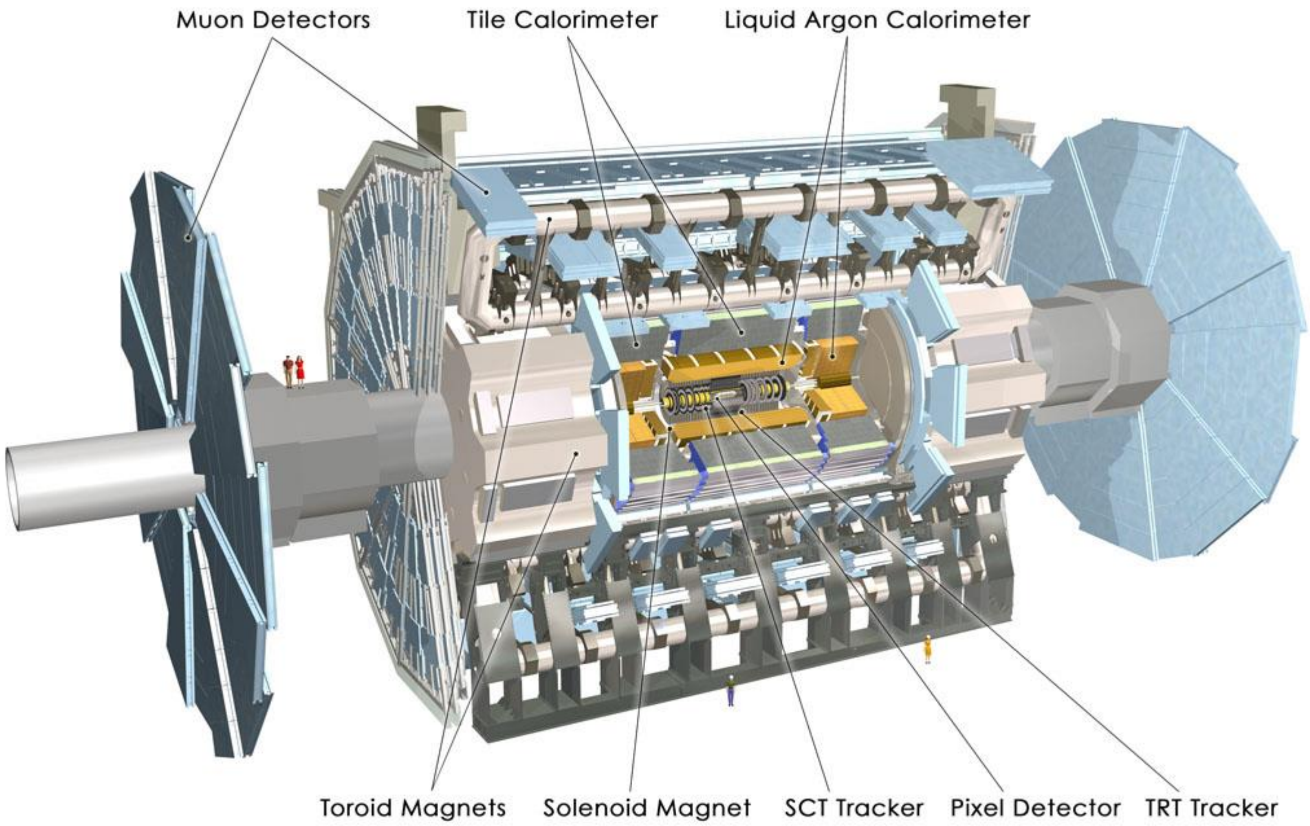


# Introduction: ATLAS

One of the two general-purpose experiments located at the LHC is ATLAS (A Toroidal LHC Apparatus). The ATLAS detector is 44 meters wide, 22 meter high and weights nearly to 7000 Tons. The ATLAS detector consists of three main components:

- **Inner detector:** momentum resolution $\frac{\sigma}{p_T} = 0{,}05\% p_T \oplus 1\%$, with a coverage $|\eta| < 2{,}5$.
- **Calorimeters**: LAr calorimeter with resolution $\frac{\sigma}{E} = 10\%/\sqrt{E} \oplus 0{,}7\%$ , and TileCal with precision $\frac{\sigma}{E} = 50\%/\sqrt{E} \oplus 3\%$
- **Muon Spectrometer**: where the main function is the precise measurement of the muon tracks, $\frac{\sigma}{p_T} = 10\%$ at $p_T = 1$ TeV

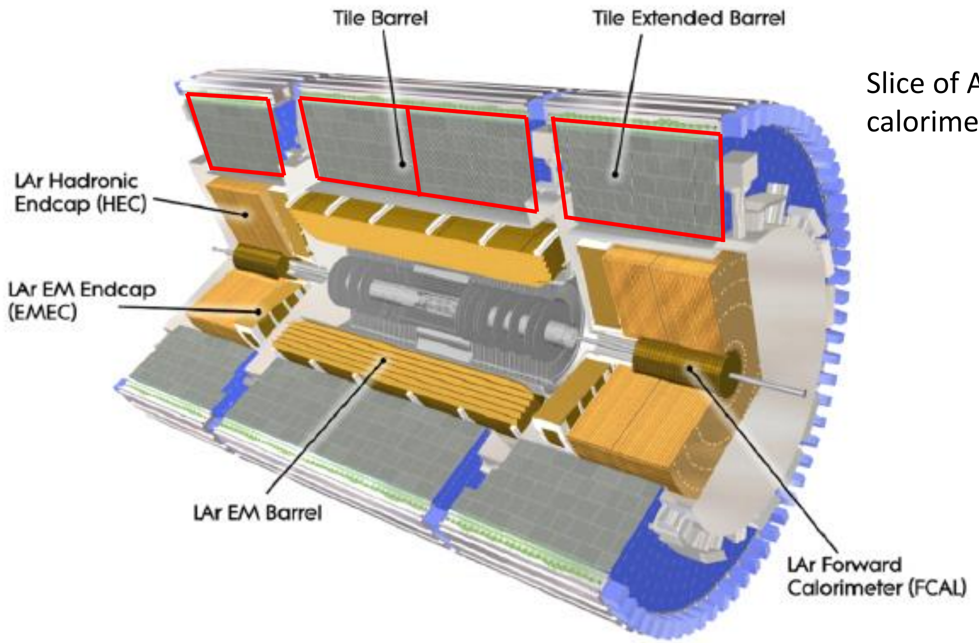





*All resolutions are referred to design values

# Tile Calorimeter

TileCal is the hadronic calorimeter of ATLAS. TileCal measures the light produced by charged particles in the plastic scintillators. The purpose is to measure the energy and directions of hadrons, $\tau$-jets and leptons and contribute to the measurement of the missing transverse energy.

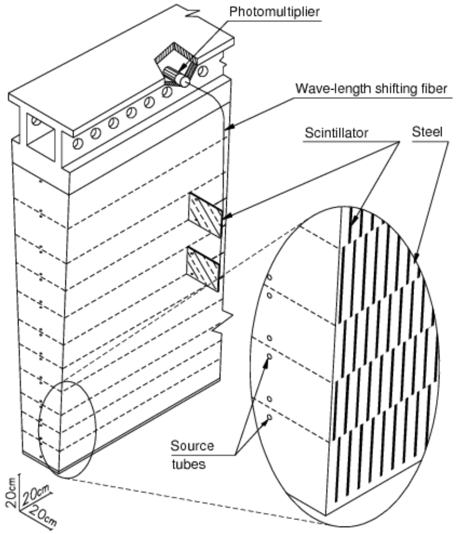


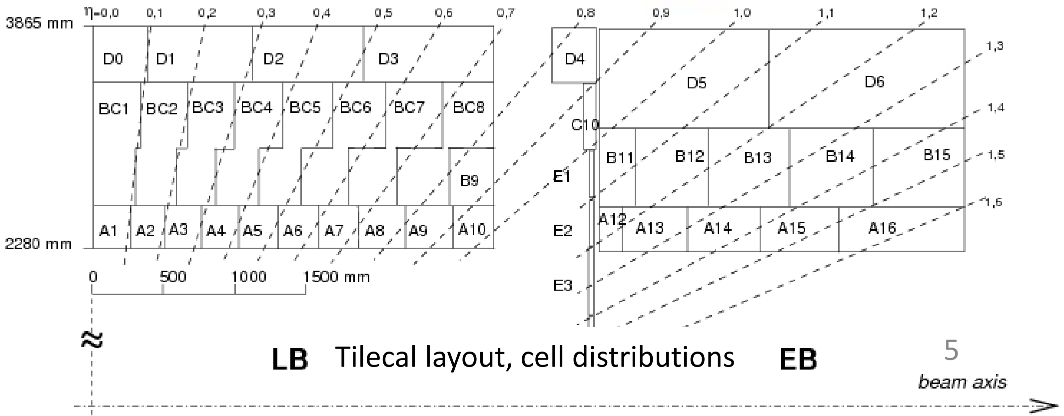

Slice of ATLAS calorimeters

Each cylinder has 64 independent modules, and each module is compounded by two Extended barrel ($0{,}8 < |\eta| < 1{,}7$) and a Long barrel ($|\eta| < 1{,}0$) divided in two section.

Each module is made of alternating thin steel plates and scintillator tiles.

Wavelength-shifting fibers are coupled to the tiles (there are redundancy, readout from both sides of the tiles/cells), collecting the light from the scintillator and send it to the photomultipliers (PMT)



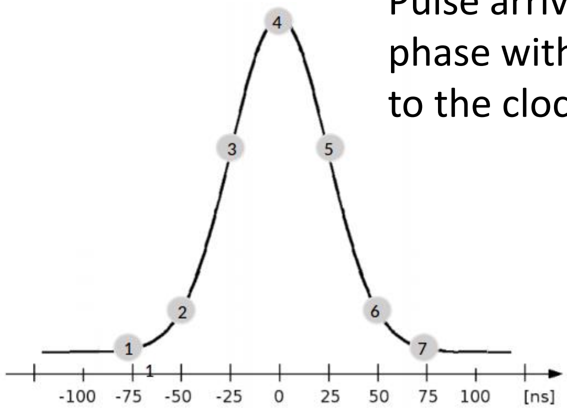




**LB** Tilecal layout, cell distributions **EB**

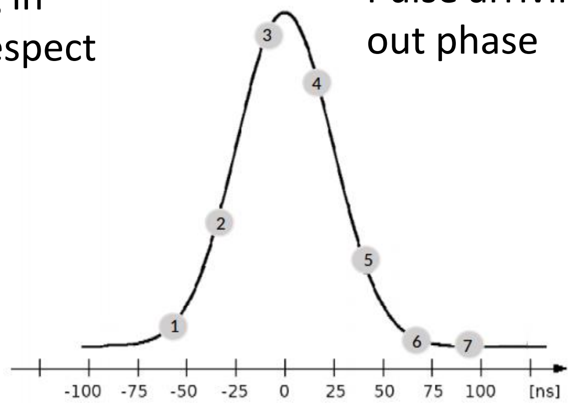
# Signal Reconstruction

The signal coming from the PMT is shaped and sampled every 25ns

As the electronics is not synchronized with the clock, pulses arrive with a random phase with respect to the clock. For that reason, and knowing that we only have 7 samples, the phase is defined as the offset of sample number 4 from the peak of the pulse.




Pulse arriving in phase with respect to the clock



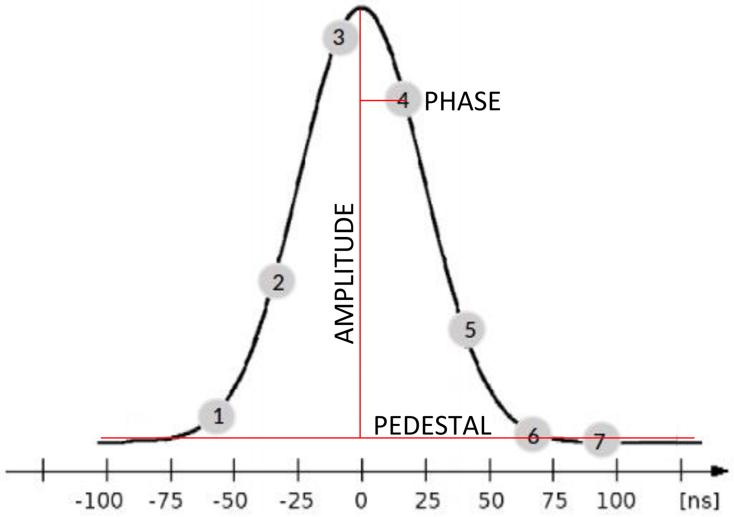

Pulse arriving out phase

Two methods exist to reconstruct the amplitude A (energy), the phase $T$ (timing) and the quality factor QF.

- Fit method: fitting the pulse with the formula: $f(t) = Ag(t-T)+c$

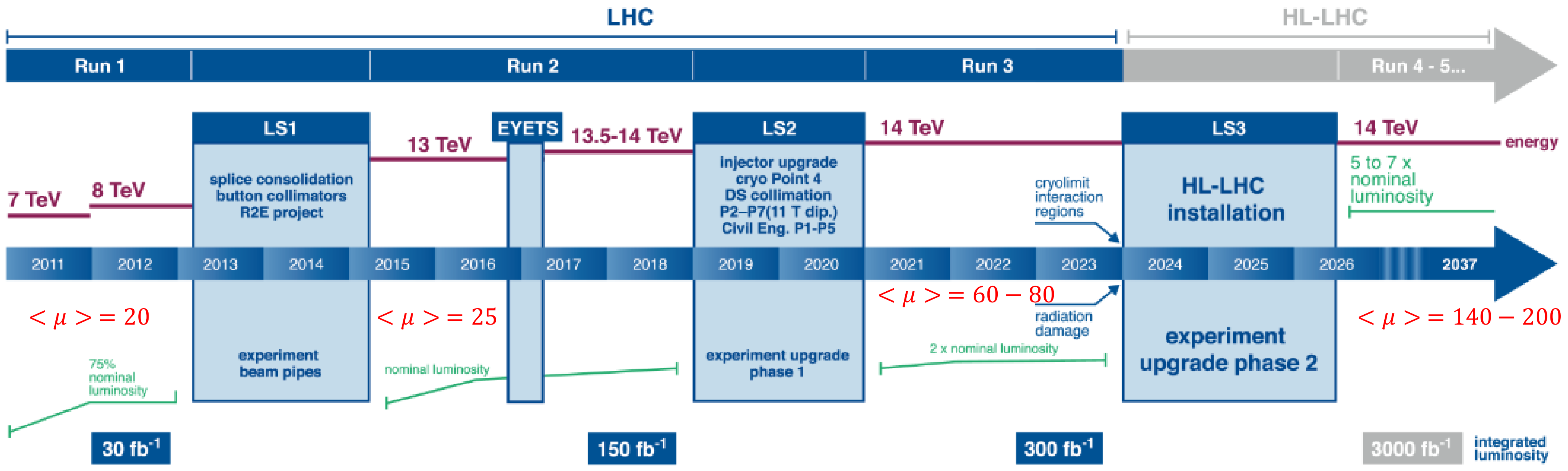
- Optimal filter method: $A = \sum_{i=1}^{7} a_i S_i$ ; $AT = \sum_{i=1}^{7} b_i S_i$ ; $QF = \sum_{i=1}^{7} abs(S_i - Ag_i)$

Where $S_i$ is the $i^{th}$ sample.



# Upgrade Phase II

The HL-LHC will start in the middle of 2026 and is going to increase 5-7 times the nominal instantaneous luminosity. This means a challenging pileup, up to 200 collisions per bunch crossing, overlapping vertices and high pileup noise in the calorimeters.




Concerning TileCal for the upgrade, most components of the Tile detector (PMTs, scintillating tiles, absorbers , fiber optics) are in good condition and there is no need to replace them. However, motivation for the upgrade are the replacement of readout in order to provide output digital data at 40 MHz (instead of the current 100 kHz that are present in the detector), due to the digital L0 trigger at 1 MHz (current electronics can not support the new rate) and improvement in the radiation tolerance.

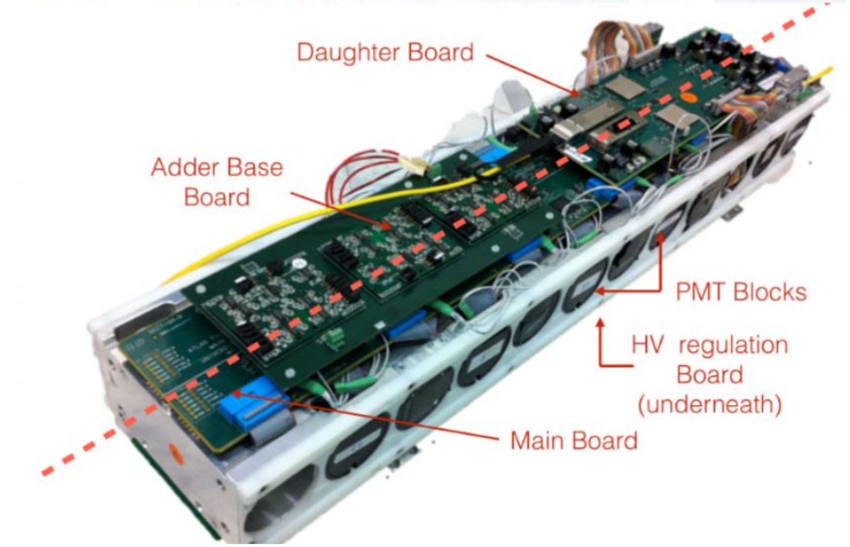
# Upgrade Phase II

The demonstrator project was defined in order to assess the long term performance of the upgraded system. Now 45 PMTs are taken care by one super-drawer and we are going to replace that s-drawer by four independent mini-drawers (12 PMTs each).

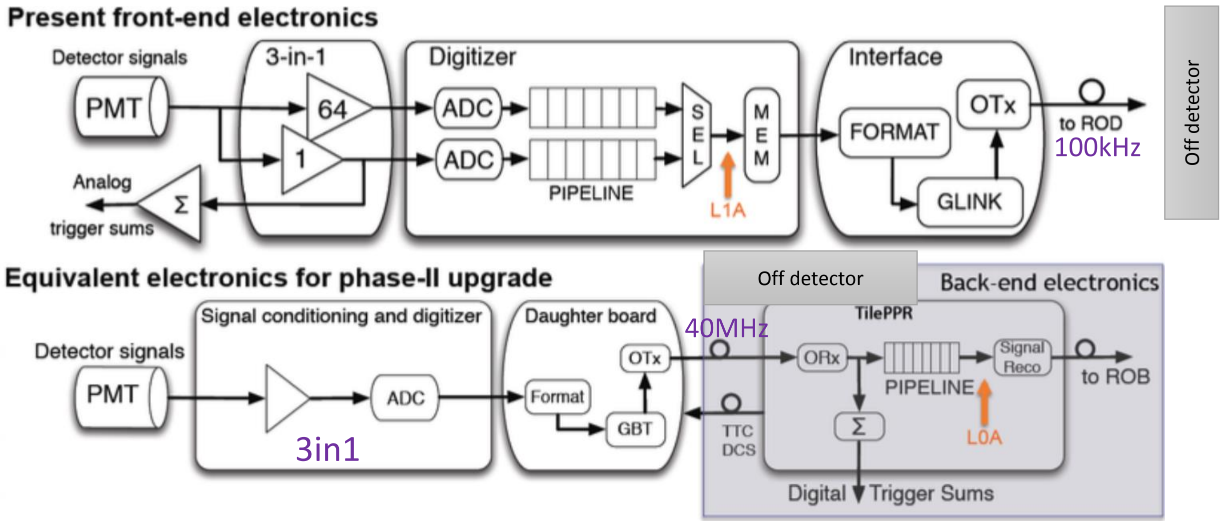
- Main Board (MB) collects data from the front-end boards (FEB)

- Daughter Board (DB) provides high speed communication between back-end and front-end through optical links (x2 gains every 25 ns) to Pre-Processor unit (PPr).

Tile "mini-drawer" Demonstrator




Three different FEB have been considered for the upgrade and have been evaluated in the lab during the test beam campaigns:

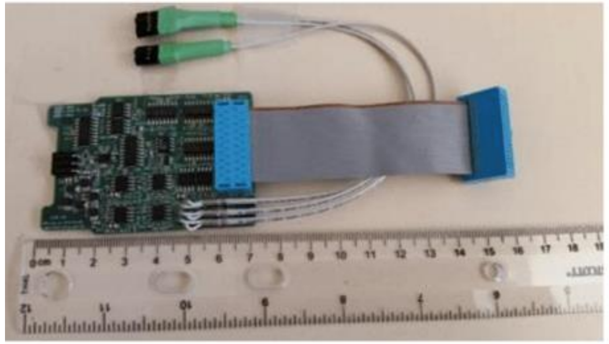



- ➢ Front-end ATLAS Tile Integrated Circuit (FATALIC)
- ➢ Charge Integrator and Encoder (QIE)
- ➢ Upgraded 3-in-1

Is the chosen option

# 3in1 and PPr

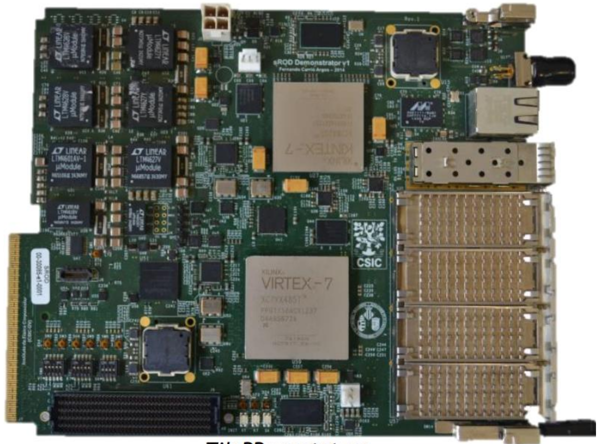
- Upgraded 3-in-1 card, located in the front-end board
  - Design follows the same approach presently used in TileCal with improved performance from experience learned.
  - Signal processing approach uses a shaper circuit to transform a PMT pulse into a digitized waveform pulse whose amplitude is proportional to the total charge of the original PMT pulse (also used now)
  - The shaper circuit performance is well characterized with calibrations procedures.
  - Bi-gain amplification (x1, x32)
  - Reliability in high resolution (12 bits, instead of 10bits)



**3-in-1 FEB**

In the TileCal HL-LHC data acquisition architecture the PMT digital samples will be transferred to the Pre-PRocessors (PPr), located in the back-end (off-detector), for every bunch crossing through optical links from the daughter board.

- The data will be stored in the pipelines buffers waiting for a trigger decision.
- In parallel, the PPr will provide reconstructed data to the trigger system at 40 MHz
- The interface with the on-detector requires bi-directional communication:
  - Uplink transfers the detector data to the PPr ( higher bandwidth)
  - Downlink is used to transmit the LHC clock and control and configuration commands




*TilePPr prototype*

# Test Beam

The objectives of the test beam are:

- Aiming at the physics measurements:
  - Electron (for EM scale)
  - Muons ( Tile tomography)
  - Hadrons (jet/Etmiss performance)

- Provide feedback about all options:
  - Reliability
  - Existing/potential problems
  - Future commissioning efforts

Final decision is the 3-in-1 option card

<table>
<tr><td></td><td></td><td>LEGACY SD</td></tr>
<tr><td></td><td></td><td>EBC65</td></tr>
<tr><td>QIE</td><td>FATALIC</td><td>DEMOSTRATOR</td></tr>
<tr><td colspan="3">LBC65</td></tr>
<tr><td colspan="2">LEGACY SD</td><td>LEGACY SD</td></tr>
<tr><td colspan="3">M0</td></tr>
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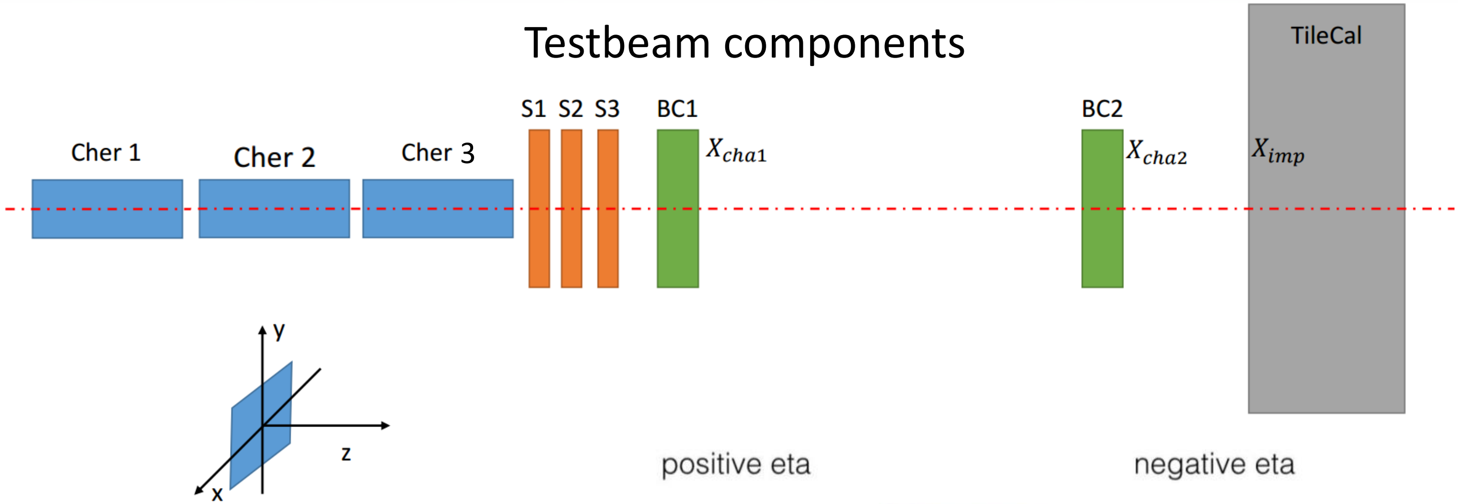
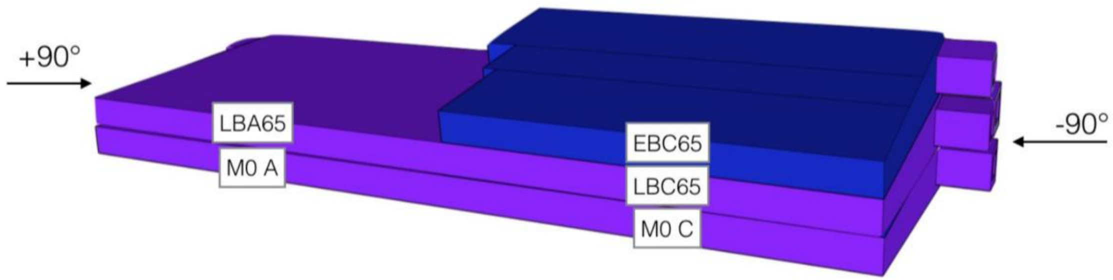
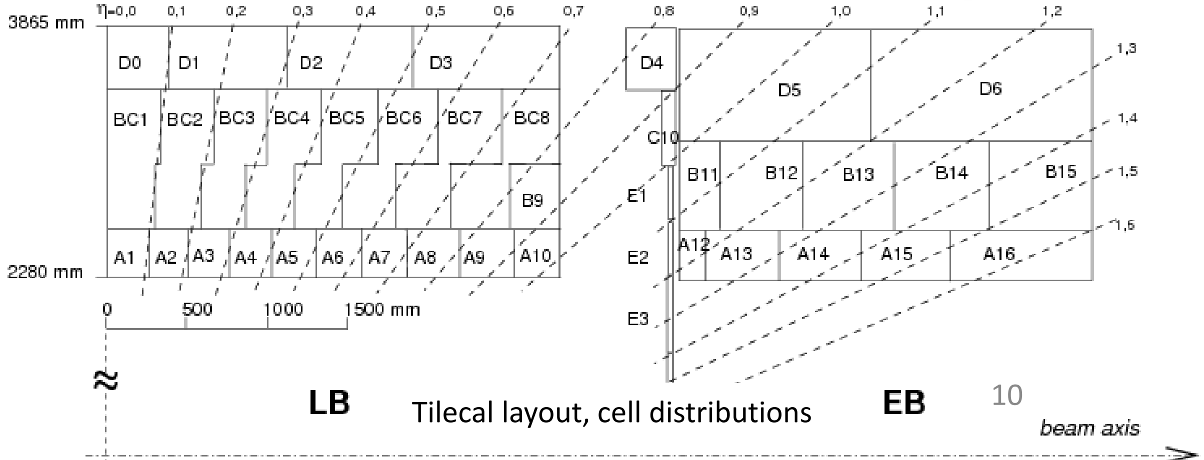
Testbeam components



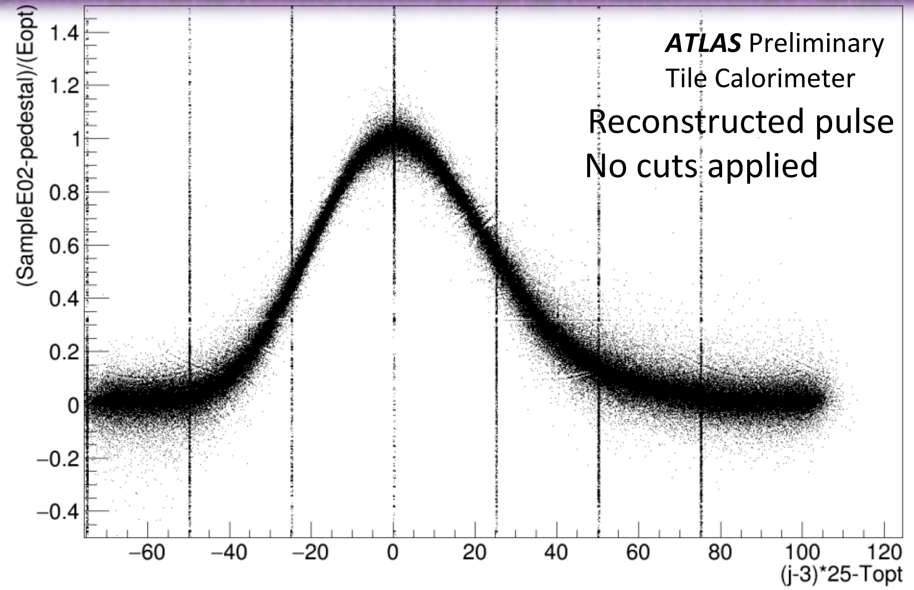

Tilecal layout, cell distributions

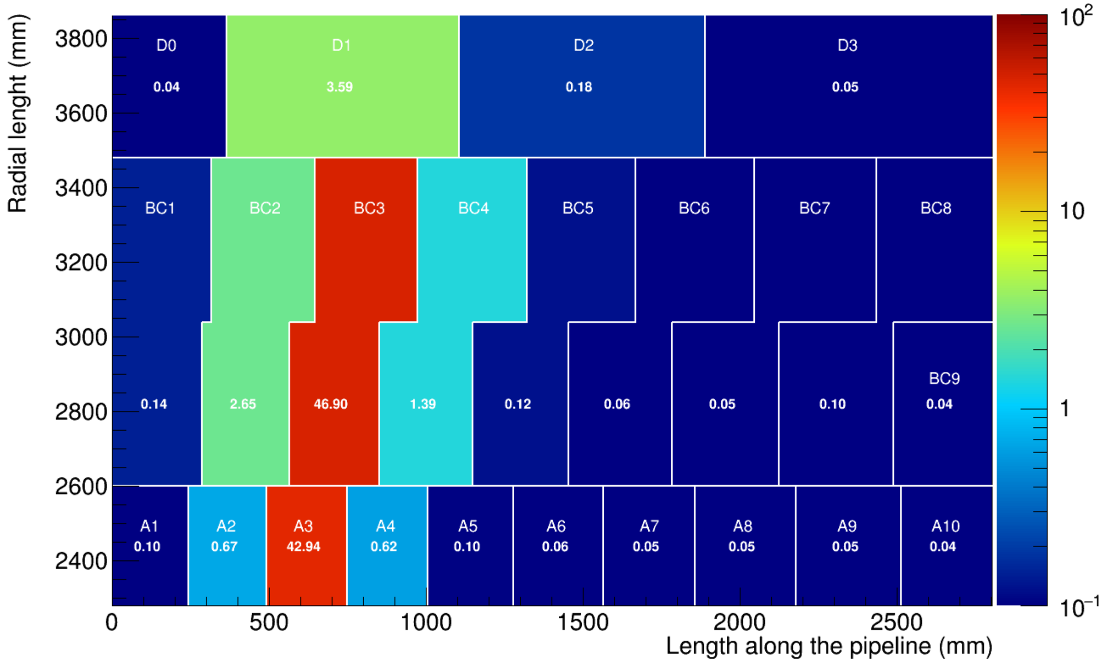
# Test Beam results

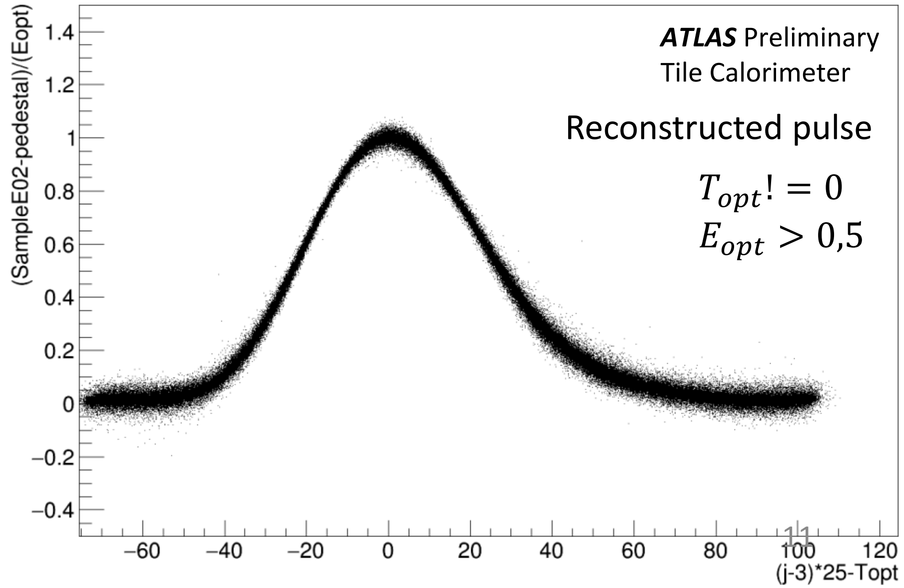
Once data is reconstructed and the calibration factors are applied, it is possible to check the pulse shape offline.

To normalize the samples requires to calculate the pedestal using the average from the distribution of the first sample (pedestal is different for a different channel):

$$pedestal = \frac{1}{n_{entries}} \sum_{i=0}^{entries} Sample_i[pmt][0]$$



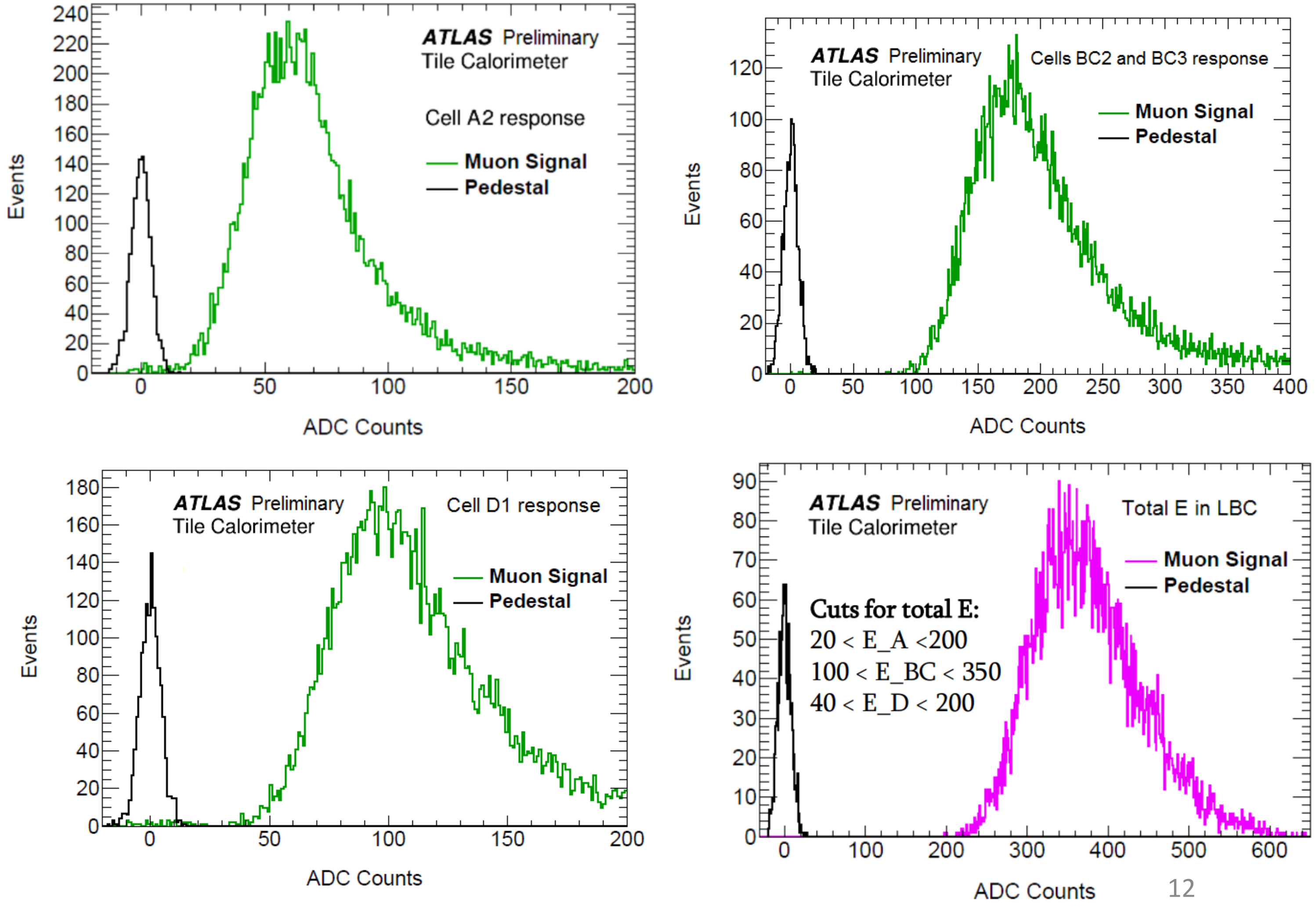



# Test Beam results

One of the capabilities of TileCal is the noise separation from signal using muons. The procedure is to keep only signals after iterative reconstruction method (actually when timing is different than zero, $T_{opt}! = 0$ ) and selecting events which have some signal above noise threshold.

- Plot the total energy in the BC and D cells to select regions where the signal is falling (two top plots)
- Look at the impact cell to see the signal deposited there (bottom left hand side plot)
- Finally applying all cuts in the selected cells the muon signal is separated from the pedestal (bottom right hand side plot)



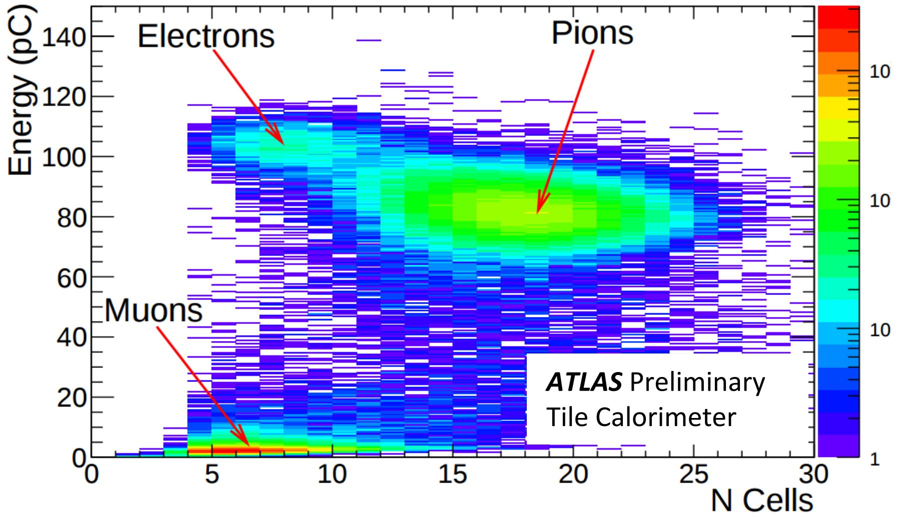
# Test Beam results

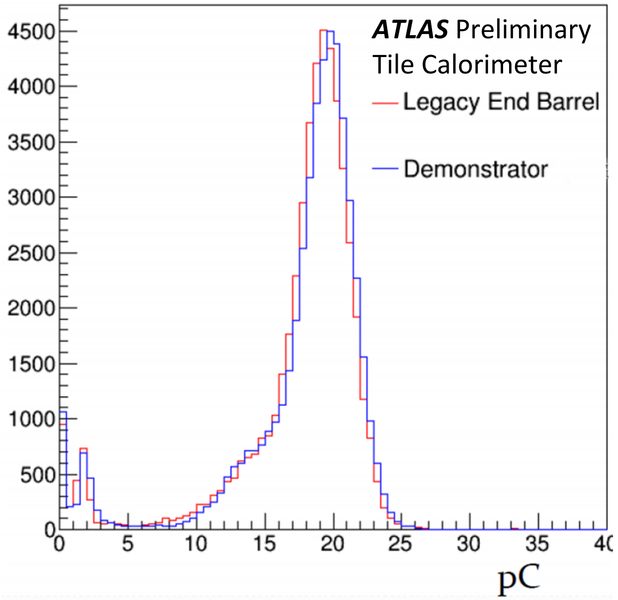
The separation of electrons from muons and pions in the testbeam is accomplished using the two-dimensional figure of pulse amplitude versus the number of cells over a certain threshold.

- Muons runs through the detector depositing energy only on the passed cells

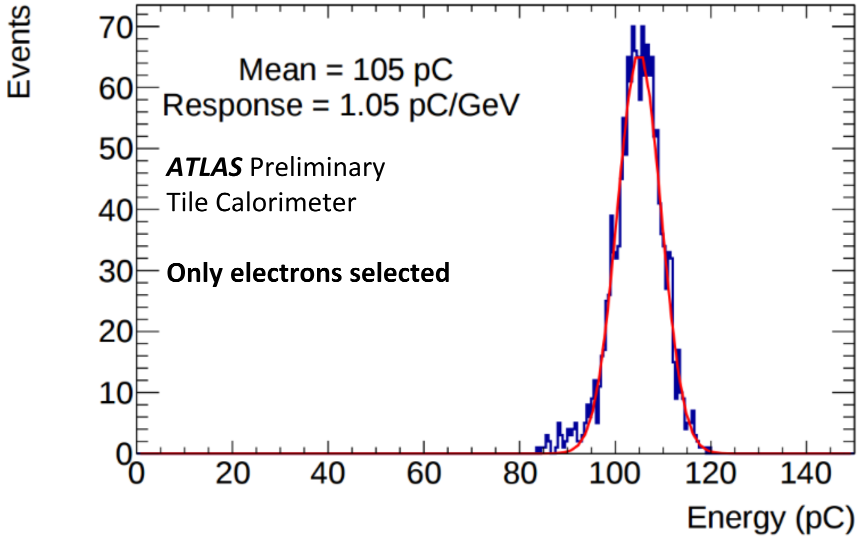
- Instead for hadronic tracks the radius is higher than for the EM jets, therefore the cells above the threshold should be also larger.

- Electrons are the remaining particles in the plot




Energy distribution for 20GeV electrons for Legacy (red) and new system (blue)



# Conclusions

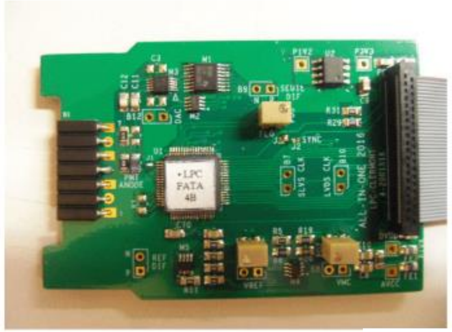
- LHC will reach 200 collision per bunch crossing during the HL-LHC era.
- Complete redesign of the front-end and back-end electronics for Phase II Upgrade, among other things the replacement of double-drawer with four independent mini-drawers.
- An ATLAS compatible demonstrator was build and successfully tested.
- 3in1 front-end technology was successfully evaluated at the testbeam and was chosen for the upgrade for its very advanced development and proven reliability.
- No buffers in the front-end electronics, all data readout at LHC frequency and sent to the back-end
- Implemented redundancy in all front-end elements, wavelength-shifting fiber in both sides of the tile/cell.
- Improving radiation tolerance moving some electronic functions to the back-end, as for instance, the PPr or the HV supplies.
    - Radiation tolerance studies underway, no surprises expected.

# Backup

# FATALIC, QIE and 3in1

## ➢ Front-end ATLAS Tile Integrated Circuit (FATALIC)

- New technology for TileCal implemented as an ASIC aiming for low noise chip
- Is an ADC in a ASIC design
- Has an active pulse shaping
- Tri-gain amplification (x1, x8 and x64) for the signal digitation



FATALIC FEB

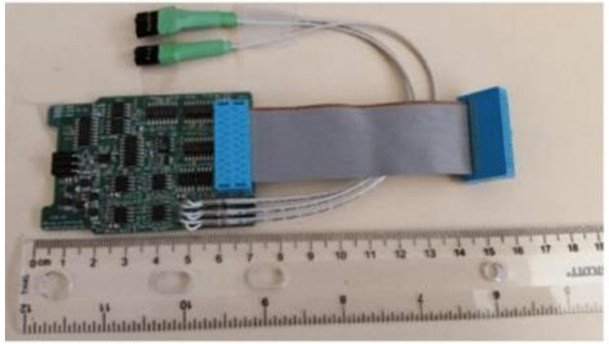
## ➢ Charge Integrator and Encoder (QIE)

- New technology in TileCal but used in other experiments (CMS)
- Is a charge conveyor in a ASIC design
- No pulse shaping for a signal digitization


QIE FEB

## ➢ Upgraded 3-in-1 card, located in the front-end board

- Design follows the same approach presently used in TileCal with improved performance from experience learned.
- Signal processing approach uses a shaper circuit to transform a PMT pulse into a digitized waveform pulse whose amplitude is proportional to the total charge of the original PMT pulse (also used now)
- The shaper circuit performance is well characterized with calibrations procedures.
- Bi-gain amplification (x1, x32)



3-in-1 FEB