The front-end data conversion and readout electronics for the CMS ECAL upgrade

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on behalf of the CMS collaboration
The High Luminosity LHC will provide \( \times 10 \) instantaneous and integrated luminosity w.r.t. LHC.
Barrel numbers:

- $|\eta| < 1.48$
- 36 supermodules, 1700 crystals each
- 2448 readout units made of $5 \times 5$ crystals
- 61200 PbWO$_4$ crystals
Legacy system

MGPA : Multi Gain PreAmplifier
ADC : 12 bits, 40 MS/s
FENIX : data concentrator and trigger primitive generation

Gianni Mazza

CHEF 2017 - Lyon, October 4th 2017
Upgrade motivations

- Increase of Level-1 trigger rate (150 kHz → 750 kHz) and trigger latency (6.4 μs → 12.5 μs)
- Provide 1×1 crystal informations for trigger (present is 5×5)
- Cool photodetectors (18 °C → 9 °C) to reduce noise due to radiation damage
- Improved time resolution (~30 ps timing) → CSA replaced by TIA and sampling frequency increased from 40 MS/s to 160 MS/s
  - Improved rejection of signals from direct hadron interaction in the APD (“spikes”)
  - Deal with pile-up increase to up to 200 events

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**Proposed scheme**

- New TIA-based front-end ASIC (*for better timing performances*) with 50 MHz bandwidth and 2-gains output
- The two TIA outputs are both converted – gain selection based on a time window
- Data compression for bandwidth optimization

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Direct connection to the transceiver (LpGBT)
CATIA

- Design by Irfu/SEDI
- Fully analog design
- Technology: CMOS 130 nm
- 1st prototype submitted on October 2016
- Successfully tested during 2Q2017
- Two versions: 2.5 V and 1.2 V only supply

CG with regulated cascode architecture
LiTE-DTU features

- Two 12 bits, 160 MS/s ADCs for input digitization
- Time window based data selection
- Lossless data compression
- LpGBT-compatible, high speed serial output (1×1.28 Gb/s or 4×320 Mb/s)
- I²C control interface
- CMOS 65 nm technology
- SEU-protected control logic
- First prototype submission foreseen for 2Q2018
ADC requirements

- Sampling rate: 160 MS/s
- Resolution: 12 bits @ Nyquist frequency
- SNDR > 63.2 dB
- DNL < 0.9 LSBs, INL < 1.5 LSBs
- Temperature range: -20 °C ÷ 85 °C
- Power consumption < 30 mW
- TID tolerant up to 20 kGy
- SEU tolerant control logic
ADC features

- CMOS 65 nm technology
- 1.2 V single supply
- Differential analogue input
- 12 bits, 160 MS/s
- Time-Interleaved, Successive Approximation architecture
- Built-in foreground calibration
- I²C configuration interface
Data selection

Gain $\times 10$  Gain $\times 1$

Saturated signals

Data from Verilog simulation
160 MS/s sampling rate
TIA approximated transfer function

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Readout architecture - 1

5×5 channels

4×(7/14/28) channels @ 1280/640/320 Mb/s

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- Direct connections between ADC chip and LpGBT e-links - no need of an extra chip for data routing

- ADC rate (2.08 Gb/s) has to match e-link rate (1×1.28 Gb/s or 4×320 Mb/s)
  - data to be reduced by 39% (+ protocol overhead)
  - can be done without data losses (Huffman coding)

- 1-to-1 match between VFE channels and LpGBT e-links
  - e-link will be available in 65 nm

- 4 LpGBT required per FE board (6 LpGBT minimum w/o compression, probably 7 without a data routing chip)
- e-link @ 1.28 Gb/s
  - 25 e-links from 5 VFE → 28 e-links from 4 LpGBT (3 not connected)
  - minimum number of e-links (simpler interconnection)

- e-link @ 320 Mb/s
  - 100 e-links from 5 VFE → 112 e-links from 4 LpGBT (12 not connected)
  - can be transmitted with the 160 MHz master clock (with DDR)
  - can provide some redundancy if ADC samples are interleaved over the 4 links connected to different LpGBTs
  - compression efficiency is decreased
Probability to transfer more than 6 bits < $2.4 \times 10^{-4}$

Probability to transfer more than 7 bits < $1.4 \times 10^{-5}$

160$\times 10^6$

2157
Data rates

- Total bandwidth without compression: $160 \text{ MS/s} \times 13 \text{ bits} = 2.08 \text{ Gb/s}$
- Probability to have an event with more than 6 bits: $< 2.37 \times 10^{-4}$
- Baseline rate: $160 \text{ MS/s} \times (1-2.37\times 10^{-4}) \times 32 \div 5 = 1.024 \text{ Gb/s}$
- Signal rate: $160 \text{ MS/s} \times 2.37\times 10^{-4} \times 32 \div 2 = 0.61 \text{ Mb/s}$
- Baseline rate close to signal: $160 \text{ MS/s} \times 2.37\times 10^{-4} \times 32 = 1.22 \text{ Mb/s}$
- Protocol overhead (estimated): $50 \text{ Mb/s}$

- **Total bandwidth required per channel**: $1.08 \text{ Gb/s}$
- **Total bandwidth available**: $1.28 \text{ Gb/s} \text{ (distributed over 1,2 or 4 e-links)}$
LiTE-DTU scheme

Diagram showing the LiTE-DTU scheme with ADCs, sample selection, encoding, multiplexer, control unit, and DDR serializers with rates of 320 Mb/s.
Data compression studies

**6-bit data format**

<table>
<thead>
<tr>
<th>01</th>
<th>6 bit</th>
<th>6 bit</th>
<th>6 bit</th>
<th>6 bit</th>
<th>6 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>sample map</td>
<td>6 bit/000000</td>
<td>6 bit/000000</td>
<td>6 bit/000000</td>
<td>6 bit</td>
</tr>
<tr>
<td>001010</td>
<td>13 bit</td>
<td>13 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001011</td>
<td>010101010101</td>
<td>13 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1101</td>
<td># samples - 8 bit</td>
<td>CRC -12 bit</td>
<td># frame - 8 bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td>0101010101010101010101</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**7-bit data format**

<table>
<thead>
<tr>
<th>0001</th>
<th>7 bit</th>
<th>7 bit</th>
<th>7 bit</th>
<th>7 bit</th>
<th>7 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010</td>
<td>sample map</td>
<td>7 bit / 0000000</td>
<td>7 bit / 0000000</td>
<td>7 bit / 0000000</td>
<td></td>
</tr>
<tr>
<td>010010</td>
<td>13 bit</td>
<td>13 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>010110</td>
<td>01010101010101</td>
<td>13 bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1101</td>
<td># samples - 8 bit</td>
<td>CRC -12 bit</td>
<td># frame - 8 bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1110</td>
<td>0101010101010101010101</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LiTE-DTU Verilog model**

Simulation example: 6-bit data format

- 5 MHz average data rate (exponential distr.)
- 64 cells FIFO - Post-synthesis verilog simulation
Model simulations

Noise levels from CATIA 1st prototype measurements (with APD and kapton cables)
Conclusions

- The CMS-ECAL upgrade foresee a redesign of the front-end electronics
  - Two custom development (CATIA and LiTE-DTU) + one common development (LpGBT+Versatile Link+)
  - CATIA main features
    - CMOS 130 nm technology
    - 1st prototype successfully tested in 2017 - 2nd prototype in 2018
  - LiTE-DTU main features:
    - dual 12 bits, 160 MS/s ADC - *IP developed by an external company*
    - data/gain selection, compression and serial transmission
    - radiation tolerant
    - CMOS 65 nm technology
    - 1st prototype in 2018
Backup slides
Scintillation vs spike signal

![Graph showing scintillation and spike signals over time](image-url)
LpGBTX block diagram

http://cern.ch/proj-gbt

2017/07/12 - Update 16
SAR and Time Interleaved ADCs

Differential, successive approximation architecture

Time-interleaved architecture
ADC metrics

- SNDR (or SINAD): Signal to Noise and Distorsion Ratio
- ENOB: Effective Number Of Bits
- SNR: Signal to Noise Ratio
- SFDR: Spurious Free Dynamic Range
- THD: Total Harmonic Distortion

\[
\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02}
\]

\[
\text{SNR} = \frac{\text{Digitized Signal Power}}{\text{Noise}}
\]

\[
\text{SINAD} = \frac{\text{Digitized Signal Power}}{\text{Noise + Harmonic Power}}
\]

\[
\text{THD} = \frac{\text{Digitized Signal Power}}{\text{Harmonic Power}}
\]

\[
\text{SINAD} = -20 \log \left( \frac{\sqrt{\frac{\text{BW}}{100}} \left(1 + \frac{\text{DNL}}{2^y}\right)}{2^y} + \left(\frac{2 \pi \frac{T_J}{10^2}}{2^y}\right)^2 + \left(\frac{2 \cdot \sqrt{2} \cdot \frac{V_n}{2^y}}{2^y}\right)^2 + \left(\frac{\text{THD}}{100}\right)^2 \right)
\]

Quantization noise, Clock Jitter noise, Analog noise, THD