The Phase-2 Electronics Upgrade of the ATLAS Liquid Argon Calorimeter System

Brigitte Vachon
McGill University
On behalf of the ATLAS Liquid Argon Calorimeter group

Calorimetry for the High Energy Frontier
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Challenging environment

- Instantaneous luminosity up to $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
  - Approximately 200 inelastic pp collisions per bunch crossing every 25 ns.
- Expected integrated luminosity of 4000 fb$^{-1}$ over a period of approximately 12 years.
- Major upgrades to the ATLAS detector required.
  - Presenting today the upgrade to the ATLAS LAr calorimeter readout electronics
ATLAS Liquid Argon Calorimeters

- Fine-grained sampling calorimeter
  - EM: LAr-lead
  - HEC: LAr-copper
  - FCal: LAr-copper and LAr-tungsten

- Granularity
  - $d\eta \times d\phi = 0.003 \times 0.1$ in EM first layer
  - $d\eta \times d\phi = 0.025 \times 0.025$ in EM second layer (shower max)

- 182,468 channels
Current readout electronics

Front-end electronics
On detector

Back-end electronics
Off detector
Upgrade of LAr readout

• LAr calorimeters expected to continue to operate reliably during HL-LHC data taking period.

• Upgrade of the electronics readout necessary to meet physics goals at HL-LHC.
  - Current LAr electronics readout incompatible with planned upgrade of the Trigger/DAQ system.
    ▪ Current system limited to 2.5 µs L1 trigger latency and 100 kHz readout.
    ▪ New system must be compatible with 10/35 µs latency for L0/L1 trigger at maximum readout rate of 4 MHz/0.8 MHz.

  - Expected luminosity at HL-LHC imposes radiation tolerance requirements on all front-end components beyond qualification for operation of the existing electronics.
    ▪ By 2026, ~20 years old electronics would not survive another ~10 years of HL-LHC operation.
    ▪ ASIC radiation tolerance requirements: TID = 1.24 kGy, NIEL = 3.4 x 10^{13} n_{eq}/cm^2, SEE = 4.6 x 10^{12} h/cm^2

  - Maintenance/replacement of electronic components > 20 years old would be difficult.

• Front-end on-detector as well as back-end off-detector electronics to be replaced.
Requirements

• Dynamic range: Driven by physics needs.
  - Low energy: Driven by calibration (MIP signals) and precision measurements needs.
  - High energy: Search for high mass particles.
  - Need ability to measure cell energy in the range ~ [50 MeV, 3 TeV].
    ▶ Requires ~ 16-bit dynamic range.
    ▶ Sets requirement on maximum input current pre-amplifiers need to cope with.

• Linearity: Energy scale set using Z or J/ψ events.
  - Need per-mille level for up to ~ 10% of dynamic range (up to ~ 300 GeV).
  - Linearity at few % level adequate at higher energies.

• Noise: Sum of electronics + pile-up noise.
  - Pile-up noise dominates at high luminosity;
  - However, aim to keep electronics noise smaller than MIP signal for calibration purposes and possible low μ physics.
  - Optimize analog shaper characteristics to minimize total noise after digital filtering.
    Baseline: Bipolar, CR-(RC)^2 shaping, 13 ns peaking time (programmable)
New readout architecture

**LAr Calorimeter Cells**

- **Phase-II Upgrade Front-End Board (FEB2)**
  - Preamp
  - Linear Mixer
  - ADC x2
  - Shaper
  - Clock & Control
  - Optical Links

- **Layer Sum Boards (LSB)**
- **CLK Fanout**

**LAr Signal Processor (LASP)**

- **FPGA**
  - MUX/Serializer
  - ORx Arrays
  - Energy sums & Data reduction
  - L0/L1 Accept Logic

- **Data Buffers**

**LAr Trigger Digitizer Board (LTDB)**

- **ADC x2**
- **MUX/Serializer**
- **CLK Fanout**
- **ORx**
- **Crate Monitoring**

**LAr Digital Processing System (LDPS)**

- **FPGA**
  - Optical Receiver Deserializer
  - TTC Control
  - L0/L1 Central Trigger Processor
  - Global Event Processor
  - Level-0,1 Calorimeter Trigger System

**FEX**

- **OTx Array**

**FELIX**

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New readout architecture

**FEB2**
- Provide input line termination, amplification, shaping, digitization and data transmission to back-end electronics.
- Design based on current FEB.
- Analog/digital separation.
- 1524 FEB2 boards, each handling 128 channels.
- Key ASICs:
  - Preamplifier + shaper
  - ADC
  - Serializer

**LAr Signal Processor**
- Processing of digitized waveform
  - Receive digitized waveform
  - Apply digital filter to calculate time and energy while suppressing noise.
  - Buffer data until trigger decision.
- Based on FPGA technology and modern communication architecture.
- Provide input to L0(L1) hardware trigger.

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Analog processing

• Integrate pre-amplifier and shaper into one ASIC.

• Two R&D projects ongoing.
  - 130 nm CMOS (TSMC)
    ‣ Line terminating preamp with dual range output and electronically cooled resistor.
    ‣ Test chip (pre-amp only) received in 2016 undergoing tests. Next submission will include shaper.
  - 65 nm CMOS (TSMC)
    ‣ Fully differential amplifier with passive feedback.
    ‣ Pre-prototype chip received in July includes preamp+shaper, programmable termination, 2 gains, programmable peaking time.

• Common test system has been designed and produced to evaluate both options.
  - Choose architecture and technology by end of 2017.
Preamp/shaper (130 nm)

- Linearity better than 0.5% up to 7 mA (25 Ω, low gain) [Current comparable to max expected from 5 TeV Z’ → ee]
- Input impedance of a few ohms can be tuned easily by C₂ capacitor.
- ENI measured to be about 300 nA.
  - A factor of two larger than expected. Larger noise due to additional resistance in input transistor. New transistor designed, tests in November
Preamp/shaper (65 nm)

- First tests encouraging.
- Linearity better than 0.2% up to ~9.7 mA (25 Ω, low gain)
- Gain increases when peaking time increases.
Digitization scheme

- Digitize waveform at 40 MHz.
- Baseline design is to use a 14-bit, radiation hard ADC.
- Cover full 16-bit dynamic range using two-gain system where each ADC digitizes only part of the range and both outputs are sent to the back-end electronics.
- Quantization noise must remain lower than intrinsic LAr resolution in order not to degrade the total resolution by more than 5%.
- Arrange gain switching such that photons from $H \rightarrow \gamma\gamma$ have their cell energy fall in the same gain as electrons from $Z$ decays, used to set energy scale.
ADC

• Requirements:
  - 14-bit dynamic range, rad hard, low power (< 100 mW / channel at 40 MSPS), INL/DNL < 1 LSB.

• Three options being explored:
  - Custom ADC design in 65 nm CMOS.
    ‣ Design that can be fully customized for LAr needs.
  - ADC design based on a commercial IP block.
    ‣ Intermediate approach: Use critical block with proven analog performance and customize digital interface as needed.
  - COTS ADC chip.
    ‣ Most expensive solution, and requires additional development to integrate into the FEB2 architecture.
    ‣ Market survey found a promising candidate: Texas Instruments ADS5294, octal 14-bit ADC, fabricated in 180 nm process, consuming 60 mW per channel at 40 MSPS
Custom ADC

- Dynamic Range Enhancer followed by 12-bit SAR.
  - DRE block similar to 4x amplifier. It determines most significant two bits of the 14-bit digital code.
  - Two-stage SAR architecture providing 12-bit.

- ADC test chips received in August and currently being tested.
Data transmission

• ADC data needs to be serialized and transmitted from on-detector front-end boards (FEB2) to off-detector back-end boards (LASP boards).

• 14-bit ADC output formatted into a 16-bit word and serialized at a bit rate of 640 Mbps.

• Total data rate per FEB2 of 163.84 Gbps.
  - 128 channels x 2 gains x 640 Mbps

• Use CERN-based IpGBT chips (8.96 Gbps user data bandwidth) and Versatile Link+ optical assemblies.
  - 65 nm CMOS (TSMC), lower power and higher bandwidth than GBT chip.
LAr Signal Processor system

- Full data stream of detector signals available in LASP modules.

- LASP module functionalities:
  - Receive digitized waveforms
  - Perform gain selection
  - Apply digital filtering and calculate energy/time of LAr signal pulses.
  - Buffer data until trigger decision
  - Transmit relevant data to trigger and DAQ systems.
LAr Signal Processor system

- Baseline hardware implementation is based on full-size ATCA format.
- LASP Processing Unit equipped with high-performance FPGA, electro-optical receiver/transceiver arrays operating at different link speed, and additional memory and clock distribution devices.
- Choice of FPGA premature, however some FPGA models on the market already fulfill LASP resource requirements.
- Each LASP Processing Unit will receive data from 2 to 4 FEB2 boards.
  - 1 LASP Processing Unit = 512 readout channels (4 FEB2)
Summary

- Readout electronics for ATLAS LAr calorimeter needs to be replaced for HL-LHC.
- New readout architecture based on free-running scheme where all data are sent off-detector to digital back-end system.
- Status and ongoing developments of critical components presented.
- The project is progressing well.
  - Technical design report submitted to LHCC at the end of September 2017.
New readout architecture

**LAr Calorimeter Cells**
- Preamp
- Linear Mixer
- Layer Sum Boards (LSB)
- CLK Fanout
- Optical Links

**Phase-II Upgrade Front-End Board (FEB2)**
- 2 gains
- Shaper
- ADC x2
- ADC x2
- ADC x2
- MUX/Serializer
- Clock & Control
- Optical Links
- Layer Sum Boards (LSB)
- CLK Fanout

**LAr Signal Processor (LASP)**
- FPGA
- ORx Arrays
- Energy sums & Data reduction
- data buffers
- L0/L1 Accept Logic
- TTC Control
- OTx Array

**LAr Digital Processing System (LDPS)**
- FPGA
- Optical Receiver Deserializer
- Optical Links
- ~250 Gbps/board
- 480 Gbps/module
- 1.92 Tbps/board
- MUX/Serializer
- CLK Fanout
- ORx
- Crate Monitoring
- SDRAM
- TTC Control Rx

**LAr Trigger Digitizer Board (LTDB)**
- ADC
- ADC
- ADC
- ADC
- MUX/Serializer
- Optical Links
- ~250 Gbps/board
- 480 Gbps/module
- 1.92 Tbps/board
- ORx
- Crate Monitoring
- SDRAm
- TTC Control Rx
Custom ADC

Small signal (0 - 0.5 V)

\[
\text{LSB} = \frac{V_{\text{fs}}}{2^N} = \frac{0.5}{2^{12}} = 0.12 \text{ mV} = \text{LSB}_{\text{ideal 14b}}
\]

Larger signal (0.5 - 2 V)

\[
\text{LSB} = \frac{V_{\text{fs}}}{2^N} = \frac{2.0}{2^{12}} = 0.49 \text{ mV} = \text{LSB}_{\text{ideal 12b}}
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