Contribution ID: **45** Type: **not specified**

The Phase-2 electronics upgrade of ATLAS LAr Calorimeter

Wednesday 4 October 2017 09:50 (20 minutes)

The LHC high-luminosity upgrade in 2024-2026 requires the associated detectors to operate at luminosities about 5-7 times larger than assumed in their original design. The pile-up is expected to increase to up to 200 events per proton bunch-crossing.
The current readout of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities to accommodate the hardware triggers requirements imposed by these harsh conditions. Furthermore, the expected total radiation doses are beyond the qualification range of the current front-end electronics. For these reasons an almost complete replacement of the LAr front-end and back-end readout system is foreseen for the 182,500 readout channels.

The system will follow a free-running architecture, where the calorimeter signals are amplified, shaped and digitized by on-detector electronics, then sent at 40MHz to the backend, which performs the energy and time reconstruction, send inputs to the trigger, and buffers the data until trigger signals are received.
The triangular calorimeter signals need to be amplified and shaped over a dynamic range of 16 bits, with low noise and excellent linearity. Developments of low-power preamplifiers and shapers to accommodate these requirements are ongoing in two technologies. In CMOS 65 nm, a fully differential design with a programmable termination, two gains and a shaper stage with programmable peaking time is being studied. A second design uses 130 nm CMOS, and features a new line termination preamplifier using an electronically cooled resistance.
In order to digitize the analogue signals on two gains after shaping, radiation-hard, low-power 40 MHz 14-bit ADCs are being developed using a SAR architecture in 65 nm CMOS technology. This architecture will lead to a total bandwidth of 275 Tbps to be sent off-detector. A newly designed VCSEL array driver shows that the required 10Gb/s transfer rate at 20-35mW per channel is achieved, suitable for integration into a low-power optical link package.

Results from the design studies on the performance of the components of the LAr readout system will be presented, as well as the results of the tests of the first prototypes.

Presenter: VACHON, Brigitte (McGill University, (CA))

Session Classification: Trigger, HV, electronics