ELECTRONICS AND TRIGGERING CHALLENGES FOR THE CMS HIGH GRANULARITY CALORIMETER

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on behalf of the CMS Collaboration
OUTLINE

- The CMS HGCAL Project
  - Electronics and Trigger Challenges
- Front-end Electronics
  - Readout ASIC
- Back-end Electronics
  - Trigger Primitive Generation
- Outlook & Summary
Major upgrade of the CMS Calorimeter Endcaps (CE) for the HL-LHC

- See JB Sauvan’s talk yesterday for a detailed overview

A high granularity and high luminosity is a big challenge for the detector design:

### THE CMS HIGH GRANULARITY CALORIMETER

<table>
<thead>
<tr>
<th>Endcap coverage: 1.5 &lt; $\eta$ &lt; 3.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CE-E</strong></td>
</tr>
<tr>
<td>Active: Silicon sensors</td>
</tr>
<tr>
<td>Absorber: Lead</td>
</tr>
<tr>
<td>Depth: $26 \times 0 / 1.7\lambda$</td>
</tr>
<tr>
<td>Weight: 23 t</td>
</tr>
<tr>
<td><strong>CE-H (Si)</strong></td>
</tr>
<tr>
<td>Active: Scintillator</td>
</tr>
<tr>
<td>Absorber: Stainless steel</td>
</tr>
<tr>
<td>Depth: $9\lambda$</td>
</tr>
<tr>
<td>Weight: 205 t</td>
</tr>
<tr>
<td><strong>CE-H (Sc)</strong></td>
</tr>
</tbody>
</table>

**CE-E** (Si)

**CE-H (Si)**

**CE-H (Sc)**
THE CMS HIGH GRANULARITY CALORIMETER

- Major upgrade of the CMS Calorimeter Endcaps (CE) for the HL-LHC
  - See JB Sauvan’s talk yesterday for a detailed overview
- A high granularity and high luminosity is a big challenge for the detector design:

<table>
<thead>
<tr>
<th>Total</th>
<th>Silicon sensors</th>
<th>Scintillator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>600 m²</td>
<td>500 m²</td>
</tr>
<tr>
<td>Number of modules</td>
<td>25 000</td>
<td>2 500</td>
</tr>
<tr>
<td>Channel size</td>
<td>0.5 — 1 cm²</td>
<td>4 — 30 cm²</td>
</tr>
<tr>
<td>N of channels</td>
<td>6 000 000</td>
<td>400 000</td>
</tr>
<tr>
<td>Power</td>
<td>Total at end of HL-LHC: ~180 kW @ -30°C</td>
<td></td>
</tr>
</tbody>
</table>
4.5 Services

The required cross-section of the service channels is mainly defined by the low-voltage, high-current bus that powers the electronics and the CO$_2$ cooling manifolding. The volume required for the low-voltage bus depends on a pending decision as to whether the DC-DC converters will be located inside the detector at the edges of the cassettes or in the RBX region, on the back of the calorimeter. There is approximately a factor of 5 difference in the current that the busses in the service channel must carry between these two cases, which has large impact on the services cross-section.

The cooling system manifolds must provide flow to 24 independent cooling loops in each endcap, as described in Section 4.4, each with its own control and shutoff valves. Preliminary layouts of the cooling piping show that these valves must be outside the main body of CMS, and hence 24 independent vacuum jacketed coaxial cooling lines must be provided to each endcap. The precise size of these lines has not been determined yet.

Within the CE, the services must be routed in the space between the calorimeter absorber outer boundary and the thermal screen. This volume in the cylindrical region of the CE-H, i.e., the back-most 8 layers, is illustrated in Fig. 4.9. In the current layout, the cross-sectional area available in this region is $\sim 7600 \text{ cm}^2$. Other critical areas are the routing of the services around the endcap mounting brackets, where a clear opening must be left for access to the ME1/1 chambers, and at the transition to the radial cable trays at the face of the YE/1 disk. This area is shown in Fig. 4.10.

Once the required area for the services has been determined, preliminary layouts will be made, from which mockups of the critical areas will be constructed, using the best available information about the available space, and the most realistic possible materials for mocking up the cooling lines, low-voltage bus, and other services (HV and optical cables).
The HGCAL electronics will have to cope with different detector sub-components:

- Silicon sensors (p-on-n or n-on-p):
  - 8” hexagonal wafers in three thicknesses:
    - 120 μm: 432 cells of 0.5 cm
    - 200 & 300 μm: 192 cells of 1 cm²
  - More in Elias Pree’s talk on sensors on Friday

- Scintillator part:
  - SiPM-on-tile for various tile sizes in η-φ
  - Based on CALICE’ AHCAL, see talk by F. Sefkow
  - More in Francesca Ricci-Tam’s talk on Friday

*Not to scale*
FRONT-END ELECTRONICS

Detector modules with 2 PCBs < 6mm thick:

1. PCB: “hexaboard”
   Wire-bonds to Si-sensor and very-FE ASICs

2. PCB: Motherboard for powering, data concentration, trigger generation and bi-directional communication

Trigger/data transfer:
low-power GBT links (lpGBT)

Hexaboard design for HGCROC

Hexaboard PCB for Test Beam

Wire-bonds from Silicon to 1. PCB
FRONT-END ELECTRONICS

- Detector modules with 2 PCBs < 6mm thick:
  1. PCB: “hexaboard” Wire-bonds to Si-sensor and very-FE ASICs
  2. PCB: Motherboard for powering, data concentration, trigger generation and bi-directional communication
- Trigger/data transfer: low-power GBT links (lpGBT)
At the heart of the detector electronics is the front-end readout ASIC. The design and environment of the HGCAL pose several requirements:

- System on chip: charge, time, digitization, data and trigger processing, ZS ...
- Low power: < 15 W/channel
- Low noise: < 2000 e^{-}
- High radiation: $10^{16}$ n$_{eq}$ (1MeV eq.)/cm$^2$
- High speed readout: > 1 Gb/s
- Same ROC for Si&SiPM

Signal: high dynamic range: 0–10 pC
- Charge: 0–100 fC [11 bits]
- Time over Threshold: 0.1–10 pC [12 bits]
- Timing information: Time of Arrival with 25 ps resolution > 50 fC [12 bits]
HGCAL ASIC EVOLUTION: FROM SKIROC TO HGCROC

- **SKIROC2 (CALICE)**
  - Dedicated 64 channel Si-detector readout ASIC, SiGe 350 nm

- **SKIROC2cms**
  - Submitted and received in 1Q of 2016
  - Modification for test beams with CMS-like running conditions
  - 40 MHz clock and sampling, Gain + ToA + ToT

- **Test Vehicle 1**: submitted in May 2016, received in August 2016
  - First HGCROC test vehicle in CMOS 130 nm architecture
  - Dedicated to preamplifier studies

- **Test Vehicle 2**: submitted in December 2016, received in May 2017
  - Dedicated to analog channel study for TDR

- **HGCROCv1**: submitted in July 2017, expected in October 2017
  - All analog and mixed blocks; many simplified digital blocks

*Final HGCROC submission by mid 2019!*
SKIROC2CMS: ASIC FOR BEAM TESTS

- Modified 64ch CALICE SKIROC2 specially for test beam use
- Dual polarity preamplifier (for p- or n-type Si)
- 40 MHz clock and 25 ns sampling
- ADC: low and high (x10) gain
  - Slow shaper with 40ns shaping time
  - 300ns in rolling analog memory
- Time-of-Arrival — *proof of principle!*
  - Fast shaper (5 ns)
- Time-over-Threshold — *proof of principle!*
  - For large signals directly from the preamplifier
- TDC (TAC) for TOA & TOT (~20 ps binning, ~50ps jitter)
Extensive tests of the SKIROC2cms ASIC have been performed

- Gain and TOT linearity, noise, pedestals
- TOA transfer characteristics, efficiency, time-walk, jitter
- Temperature stability

On single-ASIC test board and hexaboard

More details about the TB performance in tomorrow’s talk by Thorben Quast
SKIROC2CMS: ASIC FOR BEAM TESTS

- **ADC and TOT linearity:**
  - HG/LG linear until 500 fC
  - TOT linear for 500fC — 10pC
- **Noise for gain:** ~ 3500 e-

- **TOA performance:**
  - Off-line correction for time-walk possible
  - Constant term: 50 ps
  - Noise term: 10ns/Q(fC) [expected ~4ns/Q]

*Jagged shape is due to imperfect interpolation between characterisation measurements.*
TEST VEHICLES FOR HGCROC

- TSMC 130 nm: rad hard technology
- 6 positive + 6 negative input preamplifiers
- 1 baseline channel
- 4 discriminators for TOT
- CR-RC shapers: HG and LG
- Digital part for noise coupling tests

- Groups 8 channels with variants of ADC and shapers
- Positive preamps
- Global 10b-DAC
- 11 bits SAR-ADC, 32x512 RAM

Building blocks successfully tested
Noise in TV2 as in specification

Noise in TV2 as in specification
- 32 channels for development/cost
- Dual polarity (for p- or n-type silicon)
- TOA, TOT with 2 variants: low power or DLL
- 11-bit SAR ADC @ 40MHz
- Simplified Trigger path: no ZS, only 4 sums
- Data readout @ 320MHz
- Slow Control with triple voting (shift register like SK2-CMS)
- Digital blocks with simplified architecture
- Services: bandgap, PLL, 10b DAC

*Not yet included*
Resolution and granularity reduction, formation of trigger cells (TC)

Selects fraction of trigger cells (threshold or fixed number of highest energy TC)

Dynamical 2D clustering of trigger cells per layer

Formation of 3D clusters — trigger primitives (TP)

L1 trigger correlator with input from track trigger

Central CMS L1 trigger
2.1. Silicon sensors

2.1.2 Sensor properties and layout

The silicon sensors for the CE-E and the inner parts of the CE-H will be planar DC-coupled hexagonal silicon sensors cut out of 8 inch (8") wafers. The hexagonal shape of the sensors makes more efficient use of the available area of the circular wafers, as compared to square or rectangular sensors, while minimising the ratio of periphery to active surface. The vertices of the hexagonal sensors are truncated, allowing clearance for the mounting/fixation system, and further increasing the use of the wafer surface. Designs based on both hexagonal as well as square sensors were studied, and the system level implications of the different geometries were considered and compared. These studies confirmed that, due to more complete use of the silicon wafers, deploying hexagonal sensors would result in a substantial cost reduction.

As discussed above, sensors will have three different active thicknesses (300, 200 and 120 µm) in order to optimize the charge collection and operation conditions over the full lifetime of the HGCAL. The baseline substrate material is physically thinned p-type FZ silicon wafers for the 300 and 200 µm thick sensors, and p-type epitaxial on a handle wafer for the 120 µm thick sensors. P-type sensors are preferred, as these have been shown to be more robust against non-Gaussian noise due to radiation induced surface charge effects [ref Tracker R&D, calculations]. In addition, the better characteristics and radiation tolerance expected for the NMOS input transistors of the front-end amplifier lead to a better expected S/N performance for p-type sensors as compared to n-type sensors. The possible use of n-type 300 µm sensors in the lower fluence part of the HGCAL remains an option under study, contingent on demonstrating a design which remains unaffected by non-Gaussian noise up to a fluence of $10^{15}$ n$_{eq}$/cm$^2$, as this may result in significant cost savings compared to the baseline p-type sensors.

Different sensor cell geometry and tiling options have been examined, and their system level implications have been considered. The “three-fold diamond” configuration, shown schematically in Fig. 2.3, was chosen as it allows convenient definition of symmetric sets of 2x2 and/or 3x3 neighbouring cells to form trigger primitives, and the subdivision of the module into symmetric domains for the readout chips, simplifying the layout of the module readout printed circuit board (PCB). Figure 2.4 shows the silicon wafer layouts using the three-fold diamond configuration.

**TRIGGER: HGCROCv1**

- **Reduced energy resolution:**
  - ADC/TOT linearization: automatic switching
  - Digitized charge data:
    - Gain: 11-bit ADC $\rightarrow$ LSB @ 0.1 fC
    - TOT: 12-bit TDC $\rightarrow$ LSB @ 2.5 fC
  - Compensate LSB ratio (~25) $\rightarrow$ 17 bits

- **Reduced granularity:**
  - 4 (9) cells per Trigger Cell (48 per wafer)
  - Sum of 4 channels $\rightarrow$ 17+2 bits

- **Compression:**
  - 4+4 encoding $\rightarrow$ 8 bits
Stage 1:
- Dynamical clustering based on the Nearest Neighbour TCs generates **2D clusters** in each trigger layer.

Stage 2:
- Creation of **3D-clusters** exploiting the longitudinal development of the shower using the projected position of each 2D cluster to identify its direction.

The Stage 1 -> Stage 2 data transmission is **x24 time-multiplexed** in order for all data from one endcap to be processed by one single FPGA.
BACK-END: TPG HARDWARE

- Both DAQ and TPG require boards with high I/O and significant processing power
- Aim to use generic boards developed for the whole CMS trigger and DAQ systems, not only HGCAL
  - ATCA format
  - ~100 I/O links up to 16 or 25 Gbit/s in and out
  - Ultrascale(+) FPGA(s) for processing

- Firmware simulations of the stage 1 algorithms show perfect agreement with software
OUTLOOK FOR HGCAL ELECTRONICS

Front-end electronics

- Readout ASIC:
  - HGCROCV1 tests in 2017-2018
  - HGCROC submission by 2019

- Concentrator ASIC:
  - Development in parallel to HGCROC
  - First version 2018, final by 2019

- Full system tests in 2018
- Production to start in 2020

Back-end / Trigger

- Main R&D areas for the TPG will be:
  - Development of TPG and central L1T correlator algorithms
  - Evaluation of their firmware resource requirements

- Trigger/DAQ TDR scheduled for 2020
- Production scheduled for 2021
4.5 Services

The required cross-section of the service channels is mainly defined by the low-voltage, high-current bus that powers the electronics and the CO$_2$ cooling manifolding. The volume required for the low-voltage bus depends on a pending decision as to whether the DC-DC converters will be located inside the detector at the edges of the cassettes or in the RBX region, on the back of the calorimeter. There is approximately a factor of 5 difference in the current that the busses in the service channel must carry between these two cases, which has large impact on the services cross-section.

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### HGCal Si-Sensor and Wafers

- **Hexagonal geometry** as largest tile-able polygon
  - 6” and 8” sensors considered
  - Cell sizes of ~0.5 cm² and ~1 cm²
  - Cell capacitance of ~50 pF
  - Will most likely need n-on-p for inner layers

- Some design goals
  - **1kV sustainability** to mitigate radiation damage
  - **Four quadrants** to study inter-cell gap distance and its influence on $V_{bd}$, $C_{int}$ and CCE

- A few more details about those sensors
  - Active thickness by **deep diffusion or thinning**
  - Inner **guard ring is grounded**, outer guard ring is floating
  - Truncated tips, so called **mouse bites**, for module mounting
  - **Calibration cells** of smaller size for single MIP sensitivity at end of life
A charge injection circuit with a large dynamic range will be used for covering both the ADC and TOT ranges.
Measurements from the SKIROC2_CMS currently used for HGCAL testbeams

- Highlights the increasing difficulty of achieving good noise performance at short shaping time

![Graph of RMS Noise vs Shaping Time](image1)

![Graph of ADC/TOT Code vs Input Charge](image2)
3-coefficient analog or digital finite impulse response (FIR) filters can help managing the high occupancy

Simulated for $e_n = 0.5 \text{nV/} \sqrt{\text{Hz}}$, $C_d = 80 \text{ pF}$, 10-bit signal to noise ratio after the preamplifier, with and without 1 fC (6250 e-) pileup noise in preceding samples
CONCENTRATOR ASIC

- Basic task: receive, select and transmit trigger and data
  - In two separate chains
- HGCROC trigger output: 4 e-links @ 1.28 Gb/s
- HGCROC data output: 1 e-link @ 1.28 Gb/s
- Trigger logic:
  - Reducing event size
  - Threshold or fixed number of highest trigger cells selection
  - Transmiting selected trigger cells and global sums
- Design and production to be in sync with VFE ASIC