Performance study of SKIROC2/A ASIC for ILD Si-W ECAL

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with support of Omega, LLR, ILD SiW-ECAL groups
ILD: one of two ILC detector concepts
ILD ECAL: 20-30 layers of sandwich calorimeter with tungsten absorber and 5x5 mm - segmented silicon diodes (~ $10^8$ channels in total)
PCB with ASICs embedded
Detector module of ILD SiW-ECAL

- Coper sheet for cooling
- Cover (EMI shielding)
- Power pulsing circuitry (400 mF)
- Detector Interface (DIF)
- Front-end, DAQ, TFC Not shown
- FCC Interconnects
- Single layer, ‘U’ stiffener
- Stiffener, Absorber Carbon fiber + W
- A “short SLAB”
- HV kapton
- Si PIN diodes
- PCB 1024 chn. 16x SKIROC2
- Kyushu University
Slab in bench and testbeam
Issues in slabs of test beam

Pedestal shift at some condition occurred

Some fixed channel (37?) is always noisy

Investigation of dedicated setup may help
skiroc2 (analog part)

feedback capacitance

15 cells analog memories

64 channels

Analog signal

preamp

PAC

Rf

cf

in_PA

Gain10

Fast shaper

5p, 10p, 15p or 20pF

300k

6k

Vth_trigger

4-bit DAC adjustment

10-bit DAC

12-bit TDC ramp

time tagging

Signal

Test pulse

fine tuning individual trigger threshold adjustment

12-bit ADC ramp

sel_ADC_test?

slow control

out_adc

MUX

MUX

MUX

Gain selection

Vth_gs

TDC_on?

slow control

auto gain?

forced gain?

slow control

Sel_FlagTDCb_ext?

forced FlagTDCb?

slow control

8-bit delay box:

100ns to 300ns

10-bit DAC

(From digital ASIC)

10-bit DAC

out_adc

out_tdc

out_ssh_G1

out_ssh_G10

Sel_ADC_test?

slow control

4-bit DAC adjustment

out_trigger
SKIROC2 (Analog part)

SKIROC2 features

- AMS 0.35μm SiGe process
- 7.1 x 8.5 mm die size
- 64 ch / chip
- 15 analog memories / ch
- 12 bit BX counting
- Two 12 bit ADC (G1 and G10)
- Internal trigger with DAC threshold adjust
- Power pulsing

Modification on SKIROC2A

- Threshold adjustment on individual channels
- TDC
- Empty events
- Retriggering
- Auto gain selection
- External trigger etc.
SKIROC2/2A testboard

- With soldered SKIROC2A (Thanks to OMEGA)
- Analog probe
- Slow clock in
- Connector for detector connection
- BGA400 socket SKIROC2/2A
- Test pulse in
- DIF interface
- Control PP/TDC etc.
- USB readout
Readout and DAQ

OMEGA Labview software (ported to Linux)
- Initialization
- Slow control
- Analog probe

C++ DAQ (original)
- Reimplementation of Labview DAQ
- Automatic DAQ for taking data (no configuration)
- Output compatible to ILD SiW-ECAL DAQ (Analysis codes can be shared)
Power pulsing

Cut current of each stage to minimize power consumption
Analog part (PWR_A) is examined
Power pulsing in testboard

One of power lines can be controlled from outside (this time Analog is tested)

PWR_A controls the power on the analog line

Val_evt controls the trigger veto - 10 ms delay from PWR_A due to limit of testboard

Removing capacitors can shorten the delay (ongoing)
Data sample (10 ms delay, 2 MIP)

Injection (ch. 10) memory = 0

- Entries: 1679
- Mean: 460.1
- RMS: 4.587

Pedestal (ch.10 with ch.19 injection) memory = 0

- Entries: 1704
- Mean: 239.4
- RMS: 3.585

Double pedestal seen?

Pedestal varied by memory cells

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Performance studies

- Dynamic range of threshold adjustment
- Trigger (fast shaper)
  - Gain and S/N ratio
- ADC (slow shaper: G=10)
  - Gain and S/N ratio
- TDC
  - Timing resolution and dynamic range

All studies are done with test pulse, no detector connection
Power pulsing on analog part enabled
Trigger threshold control

4-bit DAC is implemented for ch-by-ch adjustment of trigger threshold (to cope with noisy channels). We checked the threshold by S-curve measurement.

~7 DAC channel variation

Dynamic range of threshold adjustment is improved in SKIROC2A:
<1 DAC in SKIROC2 $\rightarrow$ 12.75 DAC in SKIROC2A
($\sim 0.13$ MIP with 1.2 pF $C_F$) $\rightarrow$ still not enough?
Trigger (fast shaper) performance

S-curve

50% efficiency

1 MIP

Gain : DAC count of 1-2 MIP (50% point)

Gain and S/N with average of 3 channels

<table>
<thead>
<tr>
<th></th>
<th>SKIROC2 @socket</th>
<th>SKIROC2A @socket</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (DAC/MIP)</td>
<td>108.7</td>
<td>111.8</td>
</tr>
<tr>
<td>Width (DAC) @1MIP</td>
<td>8.52</td>
<td>8.71</td>
</tr>
<tr>
<td>S/N ratio @1MIP</td>
<td>12.8</td>
<td>12.8</td>
</tr>
</tbody>
</table>
ADC (slow shaper: G=10)

### Gain (ADC / MIP)
- **Blue: SKIROC2**
- **Red: SKIROC2A**

<table>
<thead>
<tr>
<th>Channel Index</th>
<th>Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>41.9</td>
</tr>
<tr>
<td></td>
<td>46.0</td>
</tr>
</tbody>
</table>

### Pedestal width
- Channel index: 3.06
- Channel index: 4.01

### S/N ratio
- Channel index: 13.8
- Channel index: 11.8

<table>
<thead>
<tr>
<th>SKIROC2@socket (average of 64ch)</th>
<th>SKIROC2A@socket (average of 5ch)</th>
<th>SKIROC2A @soldered*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (ADC / MIP)</td>
<td>41.9</td>
<td>46.0</td>
</tr>
<tr>
<td>pedestal width</td>
<td>3.06</td>
<td>4.01</td>
</tr>
<tr>
<td>S/N</td>
<td>13.8</td>
<td>11.8</td>
</tr>
</tbody>
</table>

*different configuration (to be updated)
Bunch clock (5 MHz)

TDC Ramp Voltage

TDC Value

Test pulse

Behavior of even and odd BX seems different → should be investigated

1MIP

$\sigma_t \sim 5 \text{ ns} \ ?$

TDC Value

slope (2): $-11.1 \pm 0.03 / \text{ ns}$

slope (1): $29.6 \pm 0.13 / \text{ ns}$

TDC mean

bunch clock delay [ns]

TDC mean

bunch clock delay [ns]

TDC width

width (2): $\sim 55$

bunch clock delay [ns]

TDC width

width (1): $< 40$

width (2): $13.1 \pm 0.04 \text{ TDC}$

5MIP

$\sigma_t \sim 1 \text{ ns}$

TDC Value

slope (2): $-10.1 \pm 0.001 / \text{ ns}$

slope (1): $44.3 \pm 0.04 / \text{ ns}$

TDC mean

bunch clock delay [ns]

TDC width

bunch clock delay [ns]

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Summary and plans

• SKIROC2 is an ASIC for SiW-ECAL in ILD, successfully tested at several test beams.
• SKIROC2A is a modified version to improve issues found at prototypes.
• We confirmed similar performance on analog performance (gain, S/N) and several improved features (eg. threshold adjustment, TDC).
• We continue to identify issues in the prototype by
  - Removing capacitances from testboard to test similar condition to prototypes
  - Statistical tests with ~10 ASICs and comparison to test beam results
Plans (cont.)

• Develop a QA system for chips
  - Establish automatic testing procedure to test many chips (before assembling to the detector)

• Develop a platform for sensor studies
  - Noiseless connection to sensors necessary
  - Various type (pad, strip, PSD, LGAD, …)

• Develop a slab production system
  - Duplication from French system (for mass production) with some optimization / improvements
  - In light of ILC “official proposal” expected soon
SKIROC2 overview

- **Silikon**
- **Kalorimeter**
- **Integrated**
- **Read**
- **Out**
- **Chip**

- **64 Channels**
  - Difficult layout: 1Mip=4fC, digital activity

- **250 pads**
  - 17 for test purpose only

- **AMS 0.35 µm SiGe**
- **Die size = 65 mm²**
  - 7.5 mm x 8.7 mm
SKIROC2 analogue features

- Very low noise ($0.4 \text{ fC} = 2500 \text{ e}^-$) and very large dynamic range ($2\text{fC} \left[ \frac{1}{2} \text{ MIP} \right]$ up to $10\text{ pC} \left[ 2500 \text{ MIP} \right]$) charge preamplifier
  - With $C_{\text{detector}} = 20\text{pF}$
  - PIN diode leakage current swallow capability (up to $10\text{nA}$)

- 180ns shaping time Slow Shapers for charge measurement
  - Optimized S/N
  - Antisaturation system in Gain 10 Slow Shaper

- 2-bit shaping time adjustable Fast Shaper (30 to 120ns)
  - Antisaturation system in Fast Shaper

- Discriminator for autotrigger on $\frac{1}{2} \text{ MIP}$ (with Mask on each channel)
  - 8-bit adjustable delay to position the Hold signal

- Analogue Memory depth: up to 15 events can be stored

- 12-bit Wilkinson ADC
SKIROC2 digital features

- Full Power Pulsing

- Common features with Hardroc & Spiroc (compatibility with any CALICE DAQ system)
  - Open Collector token-ring ReadOut
  - Redundancy on Data Out & Transmit On signal lines
  - 2 switchable StartReadOut Inputs & EndReadOut Outputs:
    - to prevent chip failure

- Slow Control (versatility) + Probe System (debug)
  - Multiplexed Slow Control & Probe

- Very Complex Digital Part (~10% of the Die)
  - Manage Acquisition, Conversion, 15 SCA control, RAM, I/Os...
  - Digital part will increase in 3rd generation (~40% of the Die !)
POWER PULSING in SK2

- **Requirement:**
  - 25 µW/ch with 0.5% duty cycle
  - 500 µA for the entire chip

- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - Shut down bias currents with vdd always ON

- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => 0.6 mW/ch

- **4 Power pulsing lines:** analog, conversion, dac, digital
- Each chip can be forced on/off by slow control

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**Measurements**

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Current, Power</th>
<th>Duty Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acquisition</td>
<td>88 mA, 290 mW</td>
<td>0.5%, 1.45 mW</td>
</tr>
<tr>
<td>Conversion</td>
<td>27.3 mA, 90 mW</td>
<td>0.25%, 0.225 mW</td>
</tr>
<tr>
<td>Readout</td>
<td>8.0 mA, 26.4 mW</td>
<td>0.25%, 0.066 mW</td>
</tr>
</tbody>
</table>

**Skiroc2 power consumption with Power pulsing:** 1.7 mW ie 27 µW/ch
SKIROC2A Modifications

• **BUG CORRECTIONS**
  - Some « Zero events » during digitization: **OK** (added delays, cf. SP2C)
  - Substrate Shielding, Inputs Shielding: **IMPROVED** (added connections)
  - Test mode for naked dies (voltage drop off & missing pads): **CORRECTED** (but not tested, N/A in BGA package)
  - Trig Ext path no more thru delay cells to store the analog data: **OK**

• **IMPROVEMENTS**
  - 4-bit DAC for trigger level adjustment: **OPTIMIZED to 1 DAC unit**
  - Bandgap: **CHANGED** (from HR3)
  - Delay Cell: Slightly **IMPROVED**
  - AutoGain Selection: **CHANGED**

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**256 P-I-N diodes**
0.25 cm² each
18 x 18 cm² total area