



The NA62 Calorimetric Level-0 trigger and readout electronics

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$K^+ \rightarrow \pi^+ \nu \overline{\nu}$ Branching ratio measurement with $\mathcal{O}(10\%)$ precision

SM prediction [Buras et al. JHEP 1511 (2015) 33]

Experimental status (E787, E949)

[Phys. Rev. D 77, 052003 (2008), Phys. Rev. D 79, 092004 (2009)]

 $BR(K^+ \to \pi^+ \nu \bar{\nu}) = (8.4 \pm 1.0) \cdot 10^{-11}$ $BR(K^+ \to \pi^+ \nu \bar{\nu}) = (17.3^{+11.5}_{-10.5}) \times 10^{-11}$



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$K^+ \longrightarrow \pi^+ \pi^0$	0.20
$K^+ \longrightarrow \mu^+ \nu$	0.64
$K^+ \longrightarrow \pi^+ \pi^+ \pi^-$	0.06

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O(100 ps)Timing between sub-detectorsO(104)Background suppression from kinematics> 107Muon suppression> 107 π^0 (from K⁺ $\rightarrow \pi^+ \pi^0$) suppression

BR(K⁺ → $\pi^+ \nu \overline{\nu}$) = (8.4 ± 1.0) · 10⁻¹¹ BR(K⁺ → $\pi^+ \nu \overline{\nu}$) = (17.3^{+11.5}_{-10.5}) × 10⁻¹¹









THE NA48/62 LKr CALORIMETER





The detector

- 10 m³ liquid Krypton calorimeter, 1.25 m deep (27 X_0)
- 13284 2x2 cm² cells, projecting geometry
- Preamplifiers inside the LKr tank
- Calibration system mounted on the LKr tank

Use

- Veto in the forward direction
- High-precision measurement of the electromagnetic energy deposit



NA62 The Trigger and DAQ System



Trigger levels:

LO: Hardware synchronous level. 10 MHz to 1 MHz. Max latency: 1 ms.

L1/L2: Software level. 1 MHz to O(kHz).

12 sub-detectors. ~ 80 000 channels. 25 GB/s raw data.







6U VME board developed by CAEN upon CERN specifications.





16 CREAMs per crate.28 CREAM crates in 8 racks.TTC-LKr board handles Timing, Trigger and Control.





TEL62: the NA62 TDAQ motherboard





TEL62/L0Calo: I/O Mezzanines



TELDES 16 ch (16 bit @ 40 MHz) LVDS over Ethernet



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NA62 The NA62 Calorimeter L0 trigger



<u>3D trigger information</u>: time, position, energy of reconstructed clusters. <u>Independent</u> from CREAMs readout.

Inst. hit rate: 30 MHz Time resolution: 2.5 ns Latency ~ 20 us

Calorimeter L0 trigger implementation



- 37 9U TEL62 electronics modules
- 111 dedicated mezzanines
- 884+20 input channels, 16 bit @ 40 MHz over Ethernet LVDS
- 1 trigger output channel (Gbit Ethernet) to the L0 Trigger Processor



Peak reconstruction (parallel on all channels)







NA62 Liquid Kripton Calorimeter



- 1 D + 1 D pixel based algorithm: LKr divided in slices parallel to the y axis.
- Front-End boards (28): peaks in space and time **indipendently** searched in ٠ each vertical slice: digital constand fraction discriminator + linear interpolator for fine timing.
- Merger boards (7): peaks close in space and time merged and assigned to the • same electromagnetic cluster. **Overlap resolution** to avoid double counting: only clusters with maximum along x axis in the yellow area are reconstructed.



NA62 Calorimetric trigger performances





Conclusions

The NA62 calorimetric trigger and readout are performing as by specifications and taking data.

2016: Commissioning + Physics run (SM sensitivity) 2017-2018: Physics runs

Radiation induced effects on the electronics are being observed and managed.





Thanks!



The NA62 detector



NA62 The NA62 experiment at CERN SPS





NA62 The NA62 experiment at CERN SPS





 $d[0] < d[1] \le d[2] \ge d[3]$ d[2] > threshold

NA62 The NA48 Liquid Krypton electromagnetic calorimeter



$K^+ \rightarrow \pi^+ \pi^0$ VETO

For $K^+ \rightarrow \pi^+ \pi^0$ decays in the decay fiducial region and for $E_{\pi} < 35$ GeV 80% of the photons are in the Lkr acceptance



NA62 The NA48 Liquid Krypton electromagnetic calorimeter



13248 channels
27 X₀

$$\frac{\sigma_E}{E} = \frac{0.032}{\sqrt{E}} + \frac{0.09}{E} + 0.0042$$

$$\sigma_{X,Y} = \frac{0.42}{\sqrt{E}} + 0.06$$

$$\sigma_t = \frac{2.5}{\sqrt{E}}$$
(GeV, cm and ns)

Photon veto in the angular decay region 1-8.5 mrad

For $K^+ \rightarrow \pi^+ \pi^0$ decays in the decay fiducial region and for $E_{\pi} < 35$ GeV 80% of the photons are in the Lkr acceptance Inefficiency < 10⁻⁵ for $E_{\pi} > 10$ GeV



• INPUT SIGNAL SHAPING: the 2.7

μs long triangular signal from LKr channels is shaped into a 70 ns
FWHM pseudo-Gaussian signal
DIGITISATION: shaped signals are digitised @ 40 MHz by octal 14 bit ADCs and copied in a circular buffer
FIRST TRIGGER LEVEL (L0T):

upon reception of the LOT signal through the custom P0 VME backplane, data is moved from the circular buffer to the L0 buffer

• SECOND TRIGGER LEVEL (L1T):

when a L1T signal is received through a Multiple request UDP packet (MRP) data is sent to the PC farm

• **TRIGGER SUM LINKS**: the sums of the digitised samples from two groups of 16 channels each are serialized inside the FPGA and sent to the LKr L0 processor











- 2015: Commissioning run
- 2016: Commissioning + Physics Run (40% nominal intensity)
- 2017: Physics Run (55-60% nominal intensity)
- 2018: Physics Run
- SM Sensitivity with 2016 data