BI seminar agenda

- ***"Project context and Introduction to the collaboration with the HES-SO",*** 10 min, Jonathan Emery, CERN

- ***"A Generic and Modular Protocol Scheme for Inter-FPGA Communication using Serial Links",*** 45 min, Cedric Vulliez, CERN Technical student, Master thesis with the Reconfigurable & Embedded Digital Systems institute (REDS), HEIG-VD.

Project context and Introduction to the collaboration with the HES-SO

BI seminar

12 April 2017

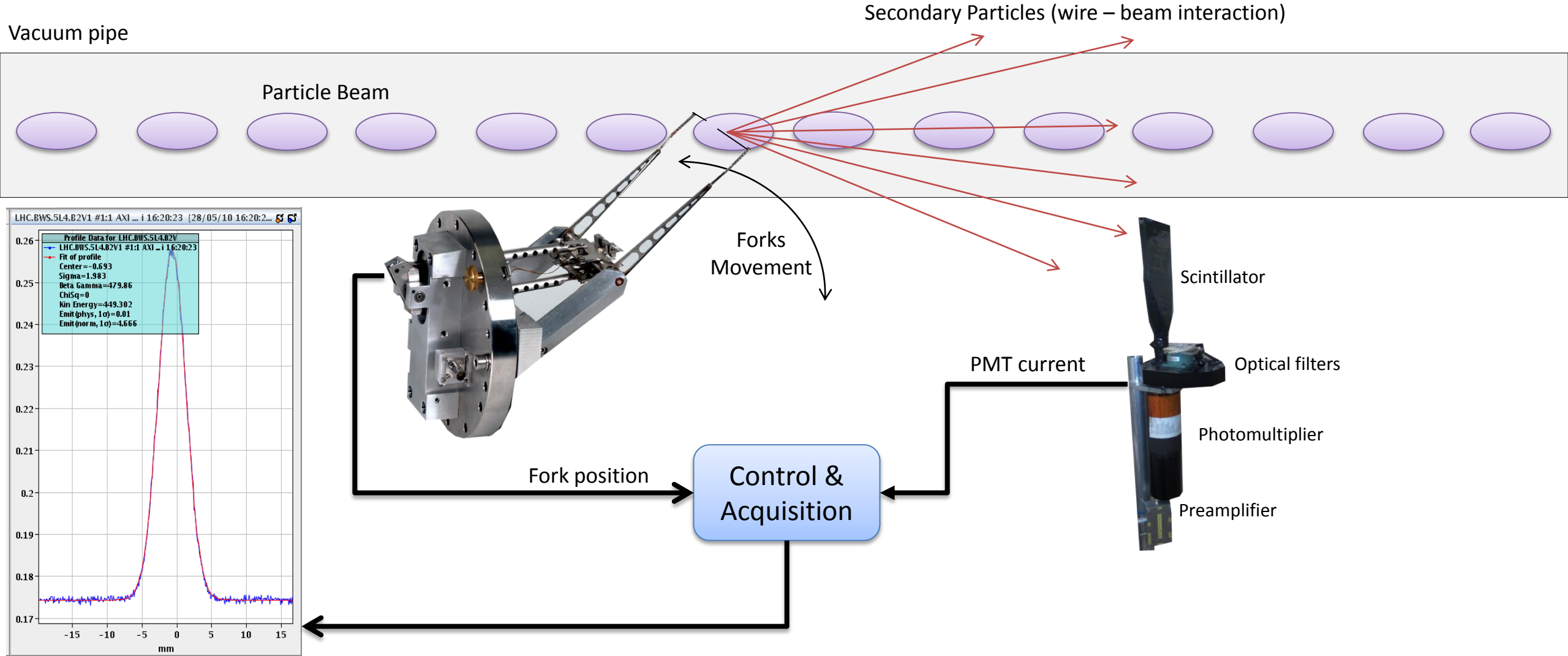J. Emery for the Wire-Scanner Electronics Project

Contents

- Beam wire-scanner principle & architecture

- Presentation of the HES-SO and HEIG-VD structure

- List of their contribution to the wire-scanner system

Project context: beam wire scanner instrument

Secondary Particles (wire – beam interaction)

Vacuum pipe

Particle Beam

Forks Movement

Scintillator

Optical filters

Photomultiplier

Preamplifier

PMT current

Fork position

Control & Acquisition

LHC.BWS.5L4.B2V1 #1:1 AXI … i 16:20:23 [28/05/10 16:20:2…

Profile Data for LHC.BWS.5L4.B2V

- LHC.BWS.5L4.B2V1 #1:1 AXI … i 16:20:23
- Fit of profile
  Center =-0.693
  Sigma=1.983
  Beta Gamma=479.86
  ChiSq=0
  Kin Energy=449.302
  Emit (phys, 1σ)=0.01
  Emit(norm, 1σ)=4.666

mm

Beam Transversal Profile
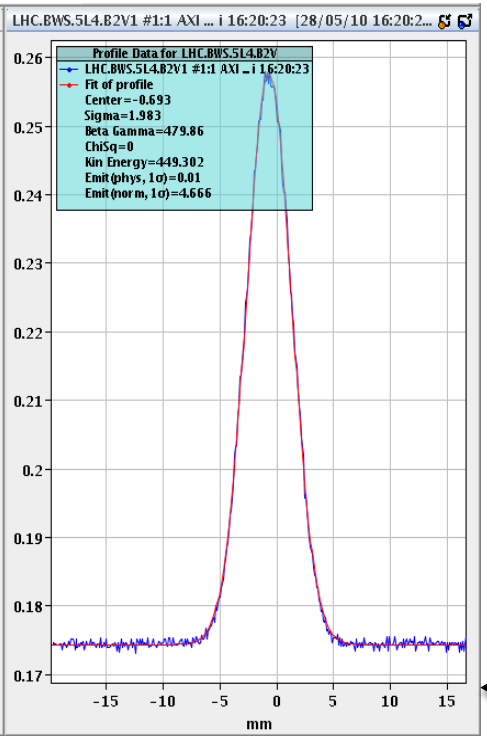
Project context: system architecture

Initial project of inter-FPGA communication

ACQUISITION AND SUPERVISION

- CPU
- MACHINE SYNCHRO
- FPGA VFC
- FPGA VFC

INTELLIGENT DRIVE

- Ethernet
- FPGA VFC
- SFP link
- Optical encoder interface
- Resolver and Serial number
- 3-phases powering
- Motor temperature
- Wire resistivity
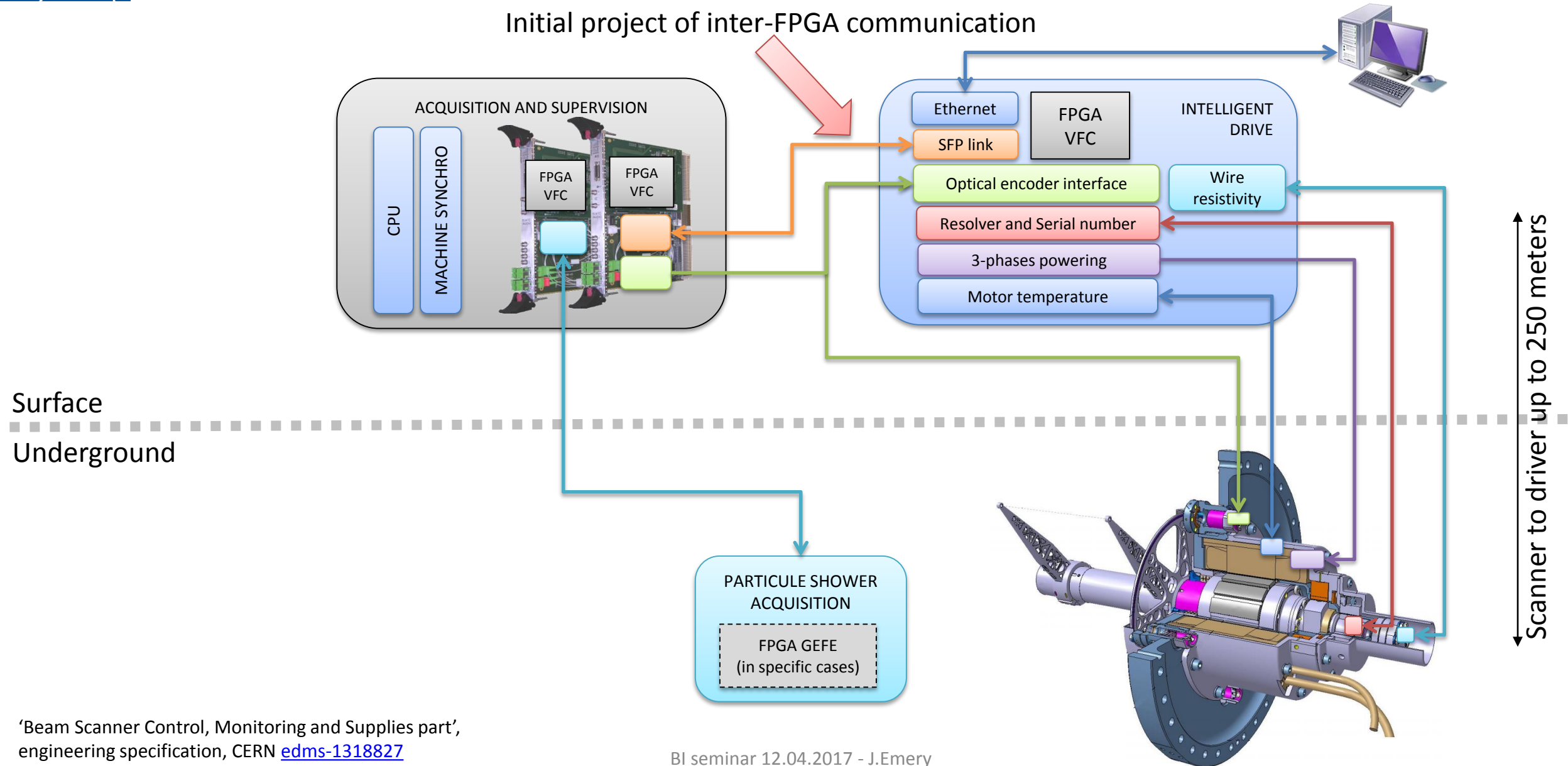
Surface

Underground

Scanner to driver up to 250 meters

PARTICULE SHOWER ACQUISITION

FPGA GEFE
(in specific cases)

'Beam Scanner Control, Monitoring and Supplies part',
engineering specification, CERN edms-1318827

BI seminar 12.04.2017 - J.Emery

Inter-FPGA connectivity meeting for BE-BI
29 Jun 2016
https://indico.cern.ch/event/542750/

- Presentations of inter-FPGA communication requirement for multiple project

- Solutions with the GBT link for FPGA to GBTX/FPGA preferred

- No common approach foreseen for higher protocol layer:
  GBT <- > to application specific logic

- Proposal of a generic and modular (versatile) concept to ease designers work

- Solve classic challenges when using serial links

- Technical specification available: https://edms.cern.ch/document/1701798/

Inter-FPGA connectivity

- Project funded for 8 month tech. student
- Cedric Vulliez join BE-BI-PM in September 2016
- Master thesis with the HES-SO, core presentation of this seminar

- At the end of this project,
  we believe we solve common complexity of such links:
1) Ports arbitration (with various services)
2) Transparent FPGA bus interconnect (virtual memory mapping)
3) Streaming interfaces with predefined bandwidth
4) Time critical signal transport with low jitter (< 100ns)
5) Extra data integrity layer by retransmission mechanism

Introduction to the collaboration with the HES-SO

28 'Hautes Ecoles' from Western Switzerland
21'000 students 2016-2017
1900 Master level students
http://www.hes-so.ch/

University of Applied Sciences (Vaud)
1600 students (2013)
http://www.heig-vd.ch/
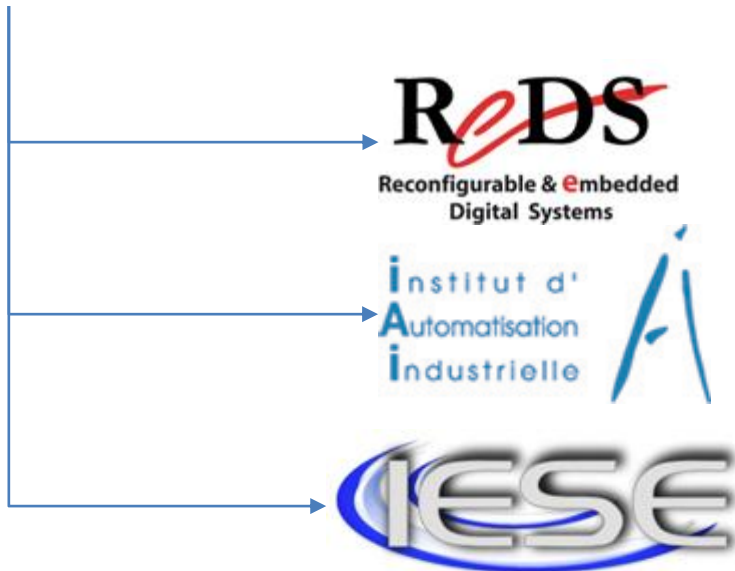
Reconfigurable & Embedded Digital Systems
https://reds.heig-vd.ch/

2 Master thesis
2 Bachelor thesis

Industrial automation
https://reds.heig-vd.ch/

1 Mandate
1 PA

Energy & Electrical Systems
https://reds.heig-vd.ch/

1 Bachelor thesis

Introduction to the collaboration with the HES-SO

- First contacts in September 2011
- Since then, 7 projects done.

- High technical competencies required during designs phases
- Large variety of subjects requiring experts of various domains
- High knowledge return by close collaboration (kickoff meetings, follow-up students progress, detailed written information)

- It results a in-depth system knowledge of our system, and higher specialisation/performance compared industrial solution

Motor and Break Design (2014)

- Initial motor performances not compatible with final design

- Outcome:
  - Complete design & simulation of an optimised motor
  - Extensive list of available motor type close to our needs
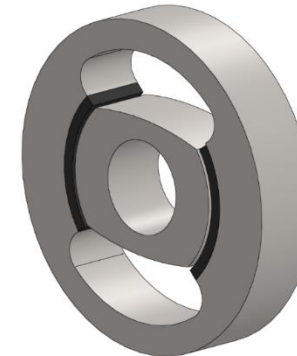 - Break design installed on SPS and PSB prototypes

SPS prototype motor

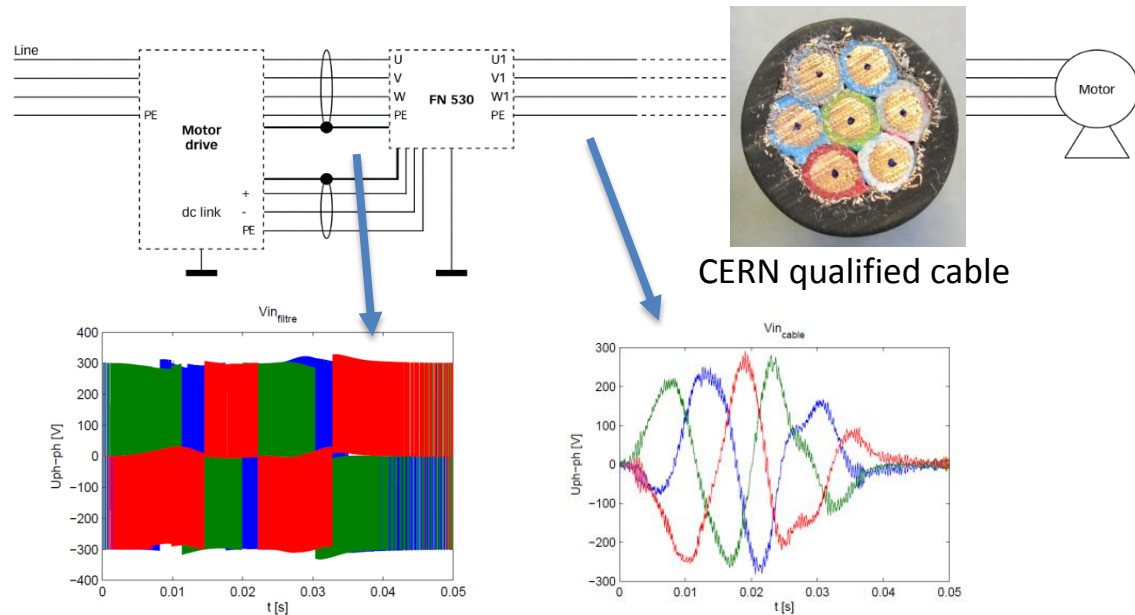New motor field lines simulation
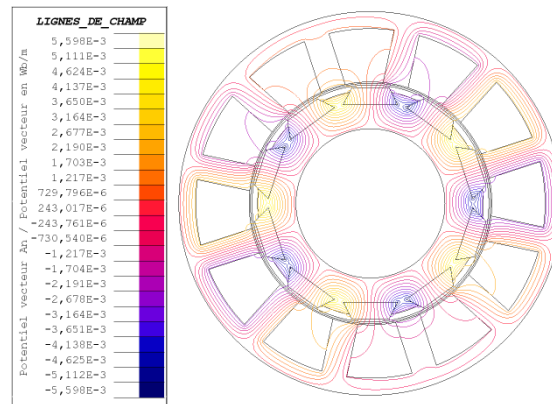
Break

See C. Grosjean presentation: BI seminar 26.09.2014

EDMS report https://edms.cern.ch/document/1416824/

Automation and powering (2012 and 2016)

Mandate on the power stage (2012-2013)
- Validate the use of switch mode drive for the BWS
- Simulate and measure EMI in the lab and in BA5

CERN qualified cable

System identification (2016)
- Experimental technics to measure system response
- Use this response to calculate feedback parameters

Outcome:
- Simulink power stage and cables modelling
- Motor control improvement (feedforward action added)
- Design recommendation for EMI minimisation to nearby cables
- Report with recommendations edms_1416465
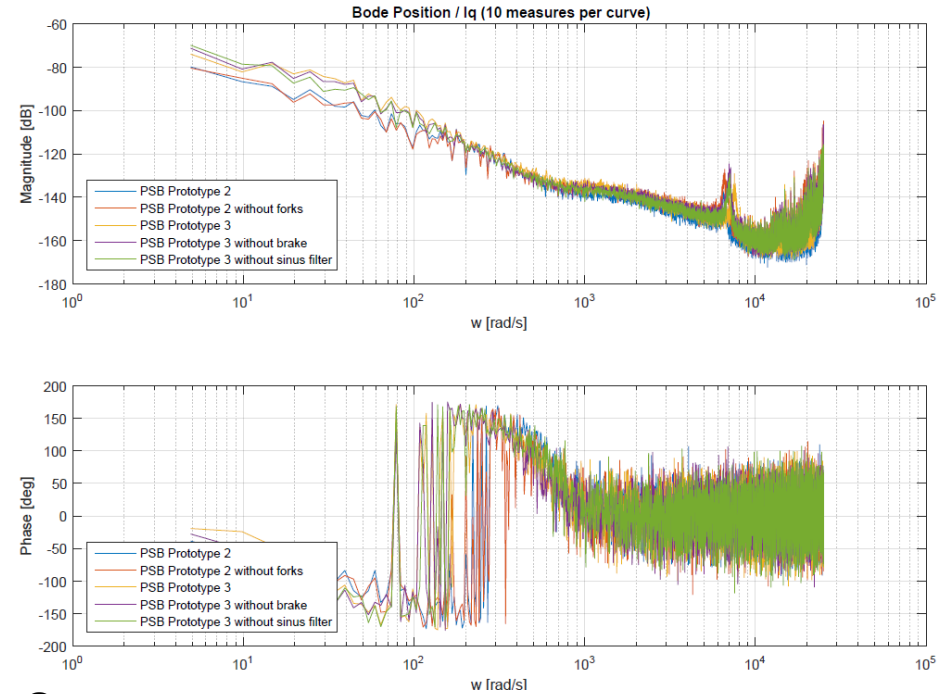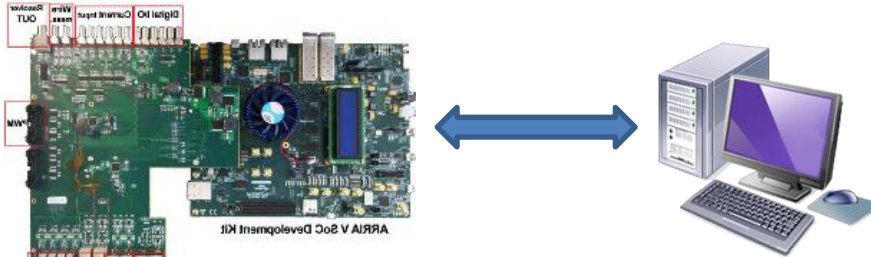
Outcome:
- New technics/tools to measure electrical and mechanical response
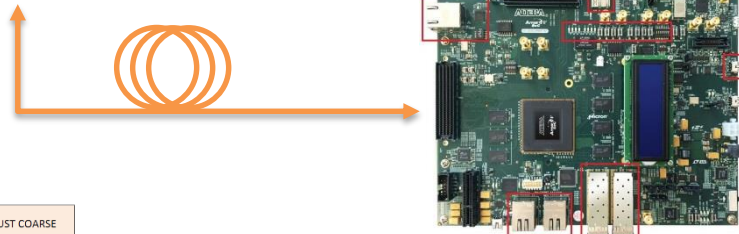- Identification of a mechanical limitation later fixed
- Report edms_1772036

FPGA based processing (2013-2017)
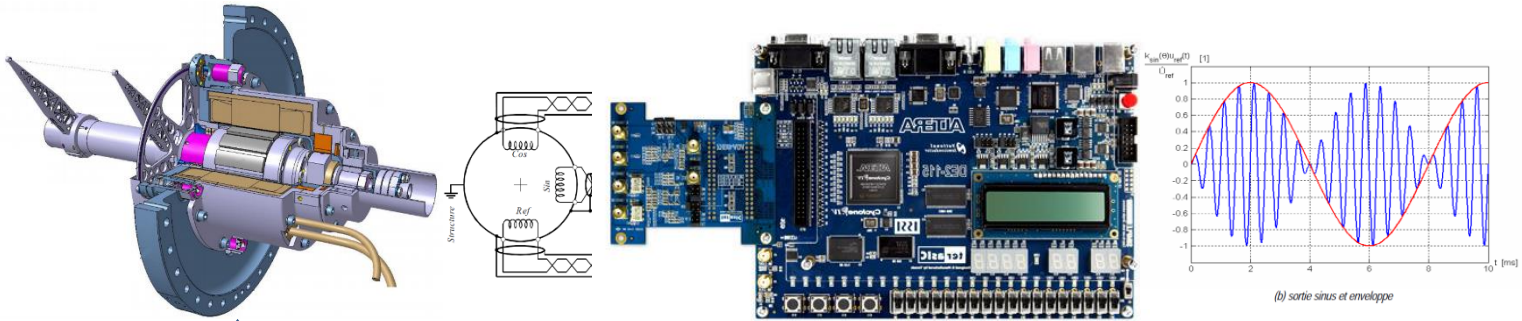
1. FPGA based position recovery from resolver signals:
Bachelor thesis by Kevin Henzer, 2013, edms_1416781

2. Ethernet interface with a System On Chip based FPGA:
Bachelor thesis by Kamil Florek, 2014, edms_1416786

3. Inter-FPGA versatile and generic protocol over serial link:
Master thesis by Cedric Vulliez, 2017, to be published in CDS
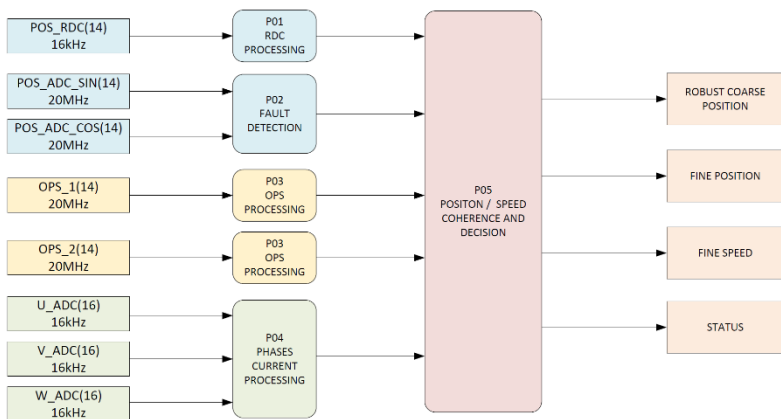
4. Real-time FPGA based processing for the wire-scanner sensors:
Master thesis on-going

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