Debug and development of the ATLAS Tile Calorimeter (TileCal) read-out link and control board (Daughterboard) for the Demonstrator Project.

(1) Introduction

The ATLAS Hadronic Tile Calorimeter Demonstrator project aims to develop and test new front-end electronics for the HL-LHC Phase-II upgrade [1].

For Phase-II, 1024 read-out modules (minidrawers) (Figure 1) each handling up to 12 photomultipliers (PMTs), will serve 256 calorimeter modules. In addition to calibration tasks, the front-end electronics condition, shape and digitize the PMT signals before they are transmitted to a Daughterboard (DB) (Figure 2) through a dense high speed FMC connector. The DB communicates with the Tile Pre-processor (TilePPr) at the off-detector systems through multi-Gb/s optical links, providing timing, configuration and control to the front-end, and continuous readout of all the MB channels to the back-end.

Clocking scheme studies for the transceivers and front-end timing were made with two different candidates: the CERN GBTx [3] and the TI CDCE ASICs. Development of alternatives for remote reconfiguration capabilities of the FPGAs are being implemented.

This work outlines some of the progress made on the development of DBs from revisions 3 and 4, and towards the upcoming DB revision 5.

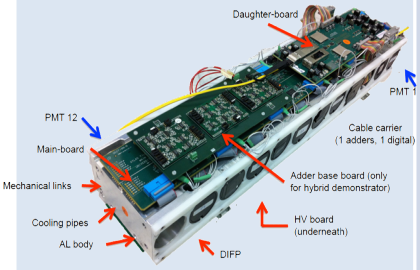

Figure 1: Demonstrator Minidrawer

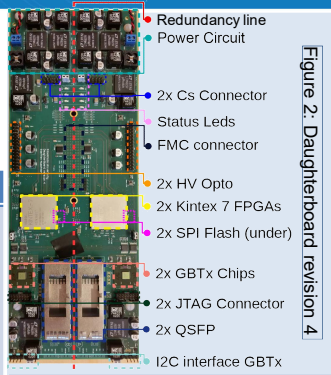

Figure 2: Daughterboard revision 4

(2) Daughterboard timing.

- The DB needs to receive ~ *5 Gbps* GBT downlink for clock recovery, control and configuration signals, and transmits readout data off of the detector via redundant ~ *10 Gbps* uplinks.
- The GBTx version 1 and CDCE performance were tested and compared resulting in a recovered *160 MHz* clock with $Tj = 94.78\ ps$ for the CDCE and $Tj = 58.25\ ps$ for the GBTx (Figure 4).
- Additional measurements were made on the GBTx version 2, resulting in $Tj = 55\ ps$ and $|\Delta Tj| > 5\ ps$ for working temperatures from 20^oC to 100^oC.
- We chose GBTx over CDCE, because it is radiation tolerant, in addition to having better jitter performance and good stability in a broad temperature range.

- GBTx-Kintex 7 solution in DB version 4 was problematic because of:
  - Compatibility with GBTx required a *4.8 Gbps* downlink and consequently a *9.6 Gbps* uplink.
  - A configuration with *9.6 Gbps* uplink is out of the Kintex7 GTX specifications, leading to a complex and non-recommended timing scheme (Figure 3).
- DB revision 5 is being designed based on a GBTx-Kintex Ultrascale+ solution, powered with GTY transceivers that remove the GBTx incompatibility.

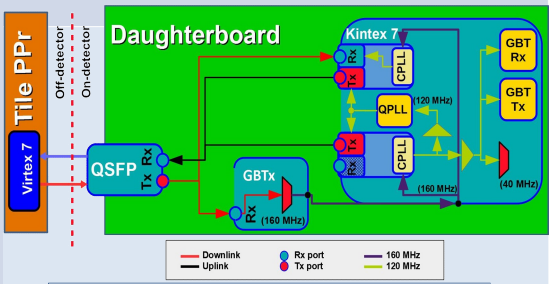

Figure 3: Daughterboard revision 4 clocking scheme

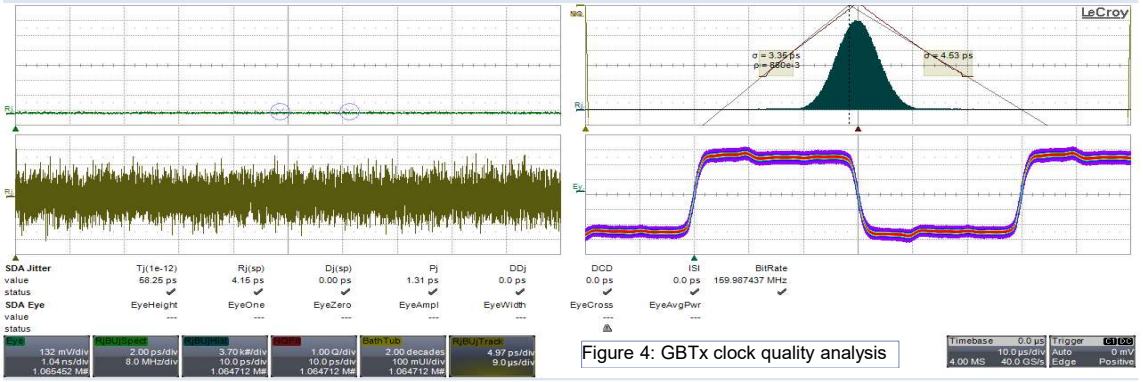

Figure 4: GBTx clock quality analysis

(3) Remote Reconfiguration.

- The FPGAs have a *128 Mbit* NAND flash each. Both FPGA and flash are reconfigured using JTAG protocol.
- For remote access to the JTAG chain, the TDI, TCK and TMS signals are received from the GBTx eports and a TDO returning signal is transmitted from the opposite FPGA uplink.
- Remote reconfiguration with JTAG commercial programmers and compatible Xilinx software has been achieved with *750 kHz - 1 MHz* maximum speed given the latency of the TDO returning signal in *90 m* optic fibers.
- Further options via networking through IPBUS are being implemented and studied, which include the use of SVF vector files and "blind programming" with no TDO signal verification. This will boost the remote reconfiguration scheme up to *20 MHz* and achieve better integration with the Phase-II system.

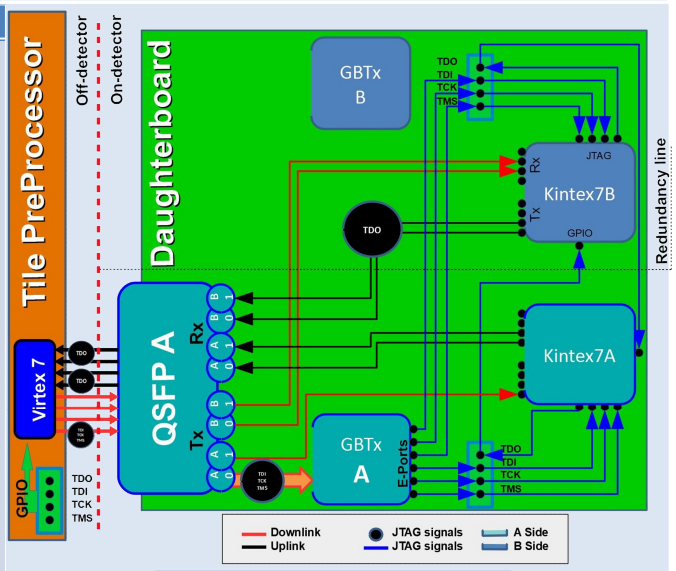

Figure 5: Remote reconfiguration scheme

(4) Outlook.

Based on the gathered experience and debugging from revisions 3 and 4, we are designing a new DB revision. The integration of GBTx and its incompatibility with the GTX transceivers motivates migrating to a new compatible transceiver architecture. Additionally it is encouraged to extend the GBTx capabilities, hence it is desirable to migrate to a FPGA fully compatible with sub-LVDS standard. The remote reconfiguration capabilities will be improved and fully integrated with the Phase-II system.

(5) References.

[1] G. Drake. **The new front-end elect-ronics for the ATLAS tile calorimeter phase 2 upgrade.** ATL-TILECAL-PROC-2015-023, 2015.

[2] S. Muschter *et al.* **Readout link and control board for the ATLAS Tile Calorimeter upgrade.** *DiVA: 805818*, 2015.

[3] **GBTX Manual**, https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf, 2016.

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