Test Status of VMM3

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Acknowledgment

Nachman Lupu, Alex Vdovin (Technion, Israel) - Brigitte Vachon, Benoit Lefebvre (MgGill, Canada)
Lorne Levinson, George Mikenberg, Ilia Ravinovich, Vladimir Smakhtin (Weizmann, Israel)

CERN - April 27, 2017

Questions

b. VMM readout start-up sequence

So far a **start-up** sequence (CKBC & TKI low before one CKTP before being enabled again) is necessary to get data from the VMM3. The VMM designers must confirm whether such a start-up sequence is necessary in the expected running mode on the NSW, fully document it and verify by simulation that it works under all conditions. It would be very good to have a test done with the ROC FPGA emulator.

c. SFM issue

It seems that this issue can be reliably solved by adding a bias resistor at the VMM input. However, it would be good to understand how the **resistor** is to be selected for instance by showing the charge and rate limits for a given resistor value. Gianluigi shall define how this can be quantified (e.g. looking at the deadtime introduced as a function of charge and rate) and make the related simulations.

d. SREC issue

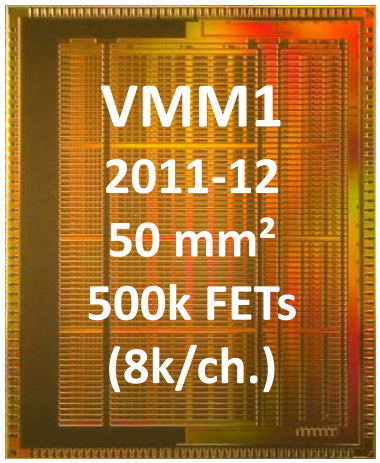
The possibility of running safely the sTGC with the **SREC** disabled is still to be proven. A plot of dead-time versus charge when the SREC is not enabled must be presented. In case the SREC is enabled, a **pi-network** is recommended at the input of the VMM and preliminary measurements with an sTGC indicate it is efficient but may not be necessary for the strips and the pads (a single resistor might work). As for the SFM, simulations should be done showing which are the charge and rate limits for a given network. Additional tests with the small sTGC must be presented. If possible, tests with the large chamber should also be presented (this might be difficult as the chamber is expected mid-April).

g. Other issues

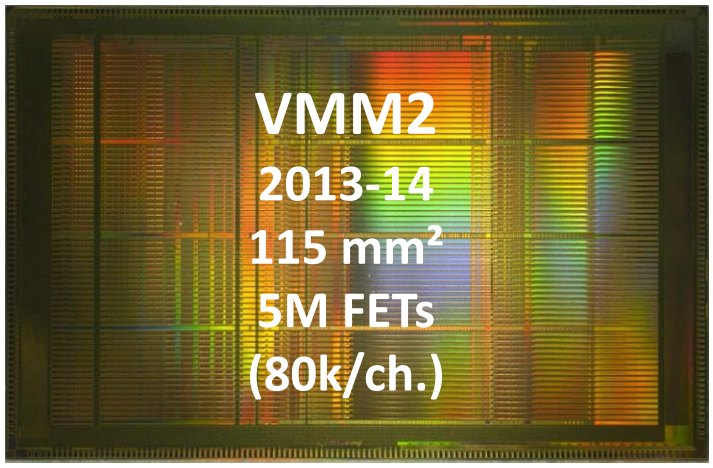
It has been shown that one can leave with the degraded performances of the **ADCs (yield*)**, the acquisition reset issue and the locking in ToT mode ... **baseline (yield*)** issue.

***new**

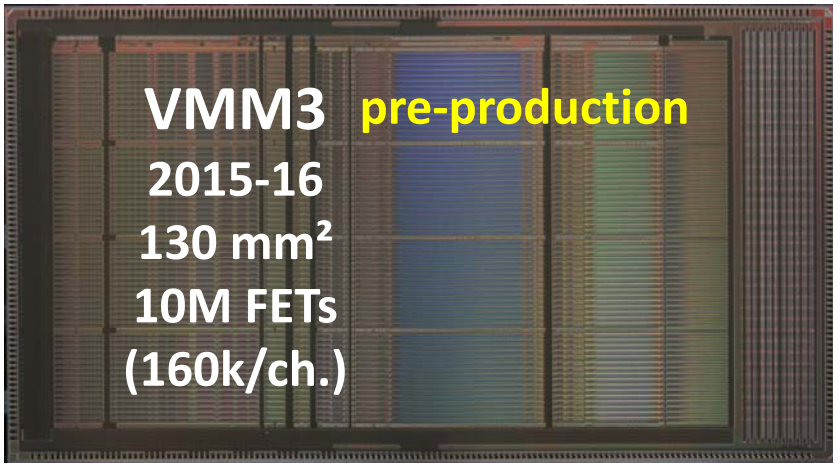
VMM Development Progress



- mixed-signal
- 2-phase readout
- peak and timing
- neighboring
- sub-hysteresis
- few timing outputs



- mixed signal
- continuous fully-digital readout
- current-output peak detector
- increased range of gains
- three clock-less ADCs per channel
- FIFOs, serialized data with DDR
- serialized ART with DDR
- additional timing modes
- 64 timing outputs
- ITAR
- additional functions and fixes



- **mixed signal + digital**
- **continuous simultaneous readout**
- **SEU-tolerant logic**
- **deeply revised front-end for TGC**
  (2nF, 50pC, fast recovery, …)
- **L0 handling digital core**
- **SLVS and new config. interface**
- **new reset control and fast reset**
- **timing at threshold**
- **timing ramp optimization**
- **pulser range extension**
- **ART synchronization**
- **32-channel skip**
- **additional functions and fixes**

VMM3 is “de facto” a first prototype

VMM3 Issues

Issue	Circuit	Notes
Need start-up sequence	channel logic	**workaround**
Handle sTGC charge & rate	analog front-end	**workaround**
Locking in ToT	channel logic	**workaround**
ENA acquisition reset	control logic	**workaround**
Trimming range extension	channel trimmer amplifier	**3/4 of targeted**
High baseline	shaper	**workaround - yield 25ns***
ADC accumulation	ADCs	**improvements - yield MSB***

***new**

Summary of Startup Sequence Issue

- **Issue** - Specific one-time sequence of control signals is required at power-on

- **Origin** - Register in the acquisition logic of the channel doesn't get reset at power-on

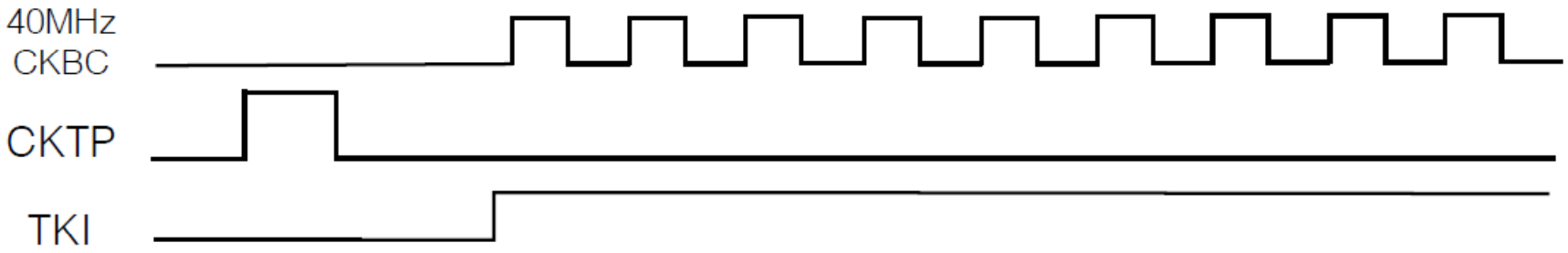
- **Workaround** - Enable-disable auto-reset function (bit STCR)

- **Fix** - Add reset logic to register

Startup Sequence Issue

VMM Readout

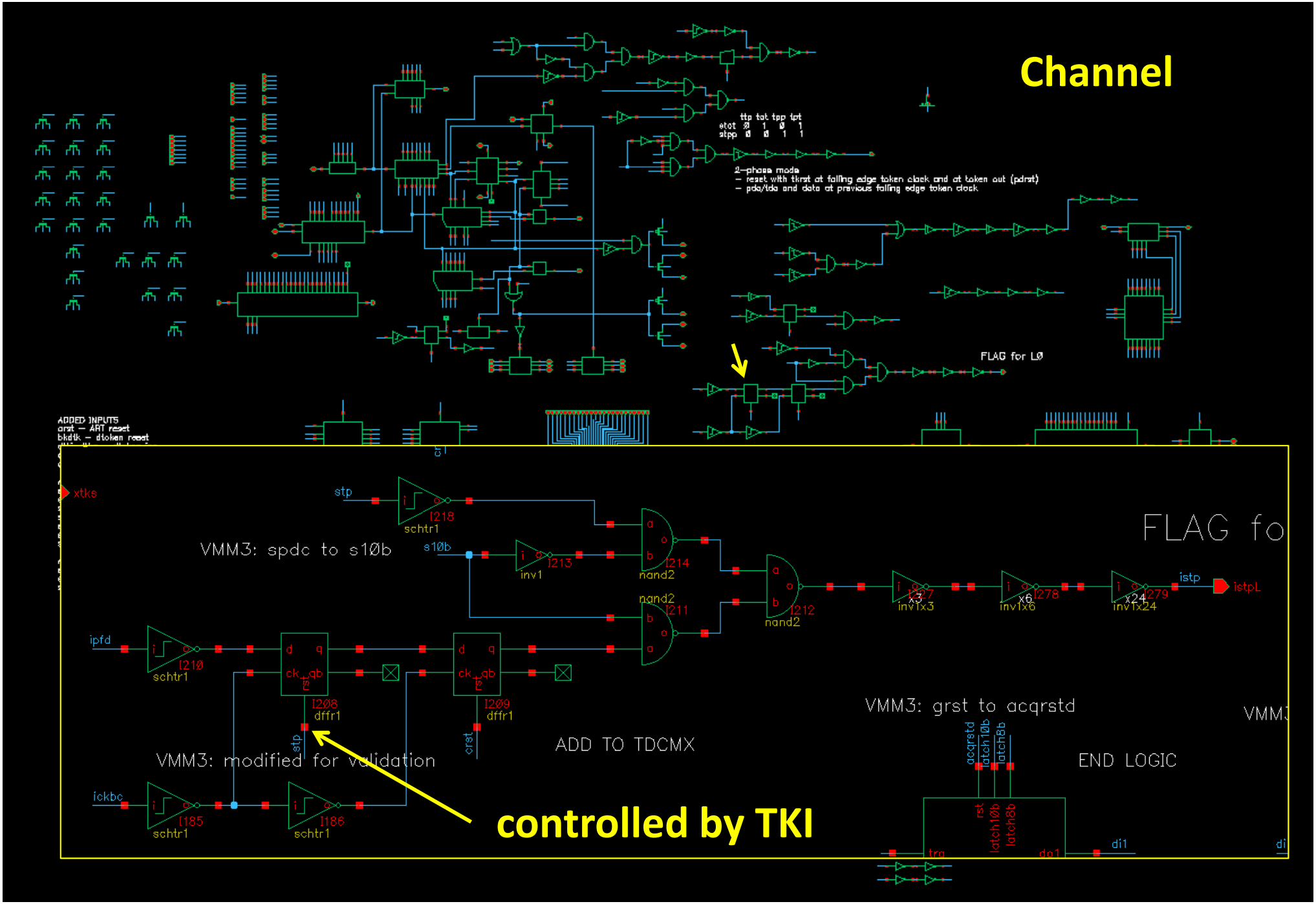
- As of today I am not aware of anybody who have readout the VMM3 without a startup sequence we found initially.
- CKBC, TKI should be low, one CKTP and afterwards we enable them again



- If the above is not followed no data are seen in the data0/1 lines
- Possible functionality comes from the reset of two monostables relevant to the global reset from the CKTP.
- If we keep the VMM3 this functionality should be foreseen in the readout/configuration logic.
- L0 readout functionality should be checked if shows the same behaviour.

This is an ongoing investigation and should be understood if it is compatible with the NSW readout.

Startup Sequence Issue



Summary of SFM Issue - Part 1

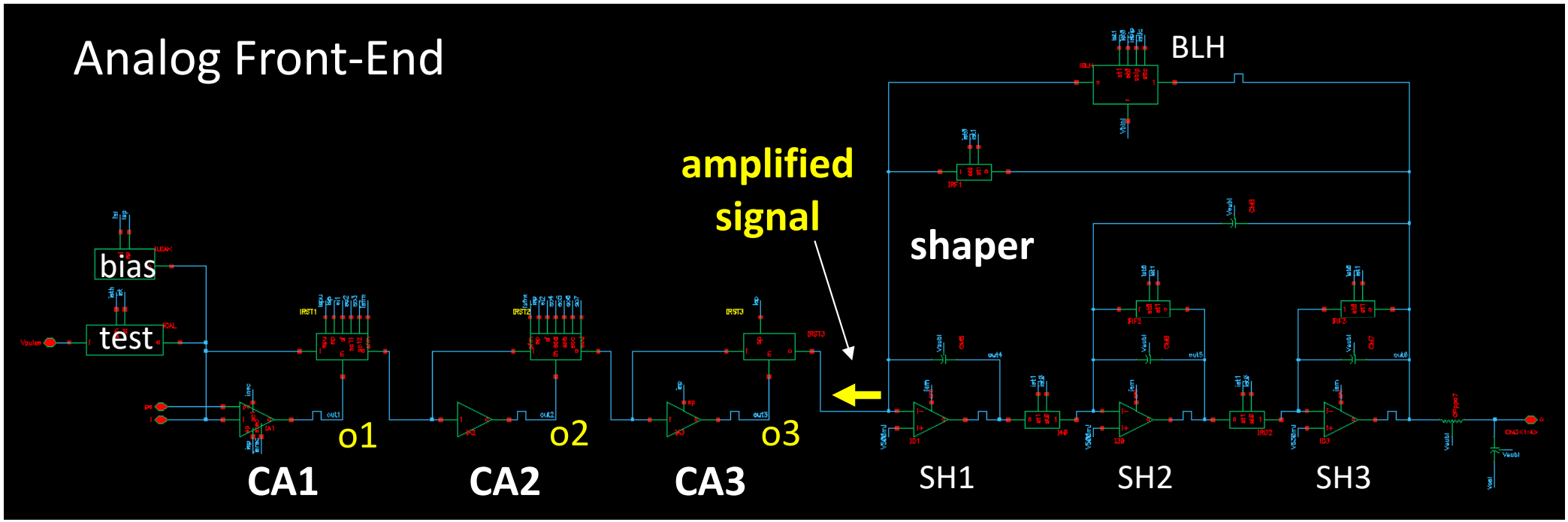
- **Issue** - In SFM mode, internal operating points can become undefined

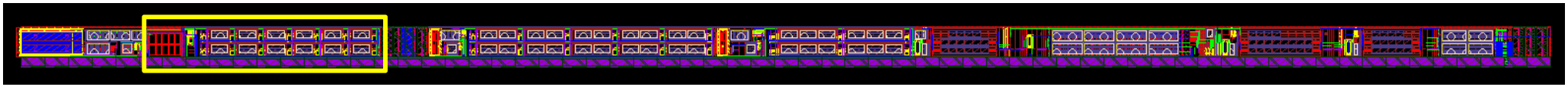
- **Origin** - In charge amplification chain, mismatch between SFM currents affects bias current of next stage

- **Workaround** - External bias resistor

- **Fix** - Increase value of bias current in SFM mode

Charge Amplification in VMM3

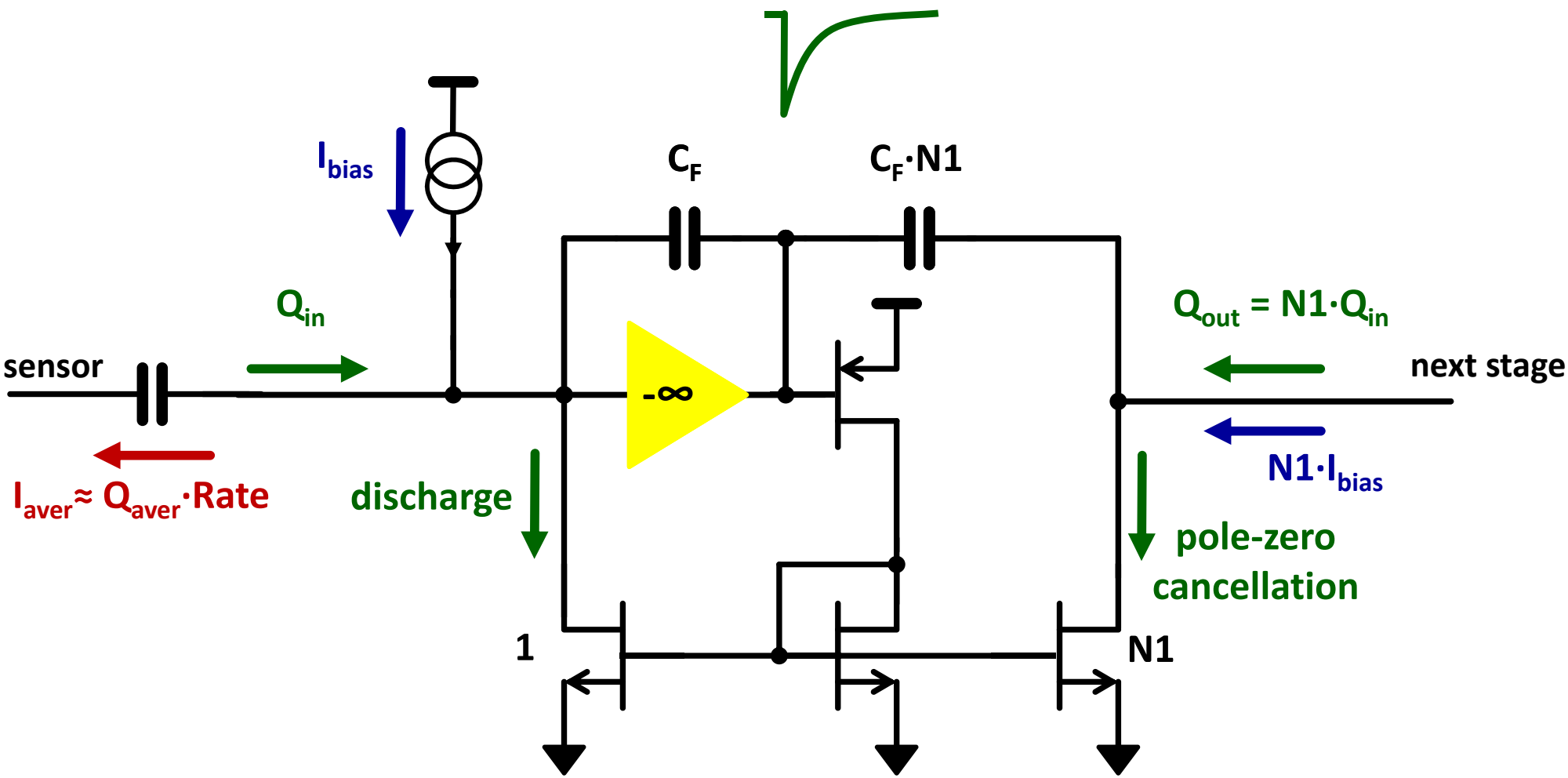




~ 4mm

- **CA1** and **CA2** are charge amplification stages with programmable gain
- **CA3** is a charge inversion stage (enabled for positive charge, bypassed for negative charge) to keep same signal polarity at input of shaper

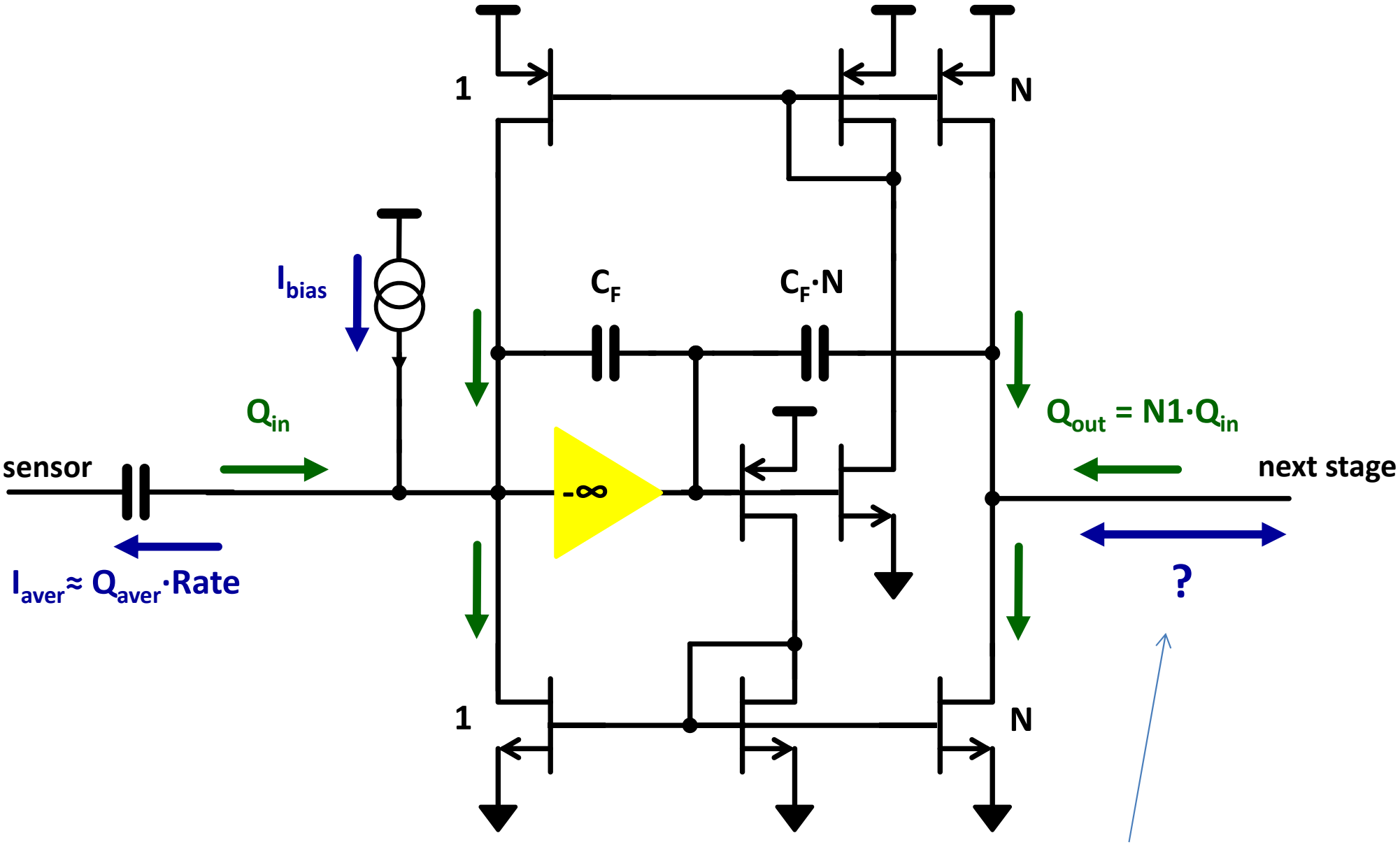
AC Coupling



$I_{aver} > I_{bias}$ → amplifier shuts down → dead time

Full-Mirror Circuit* (SFM)

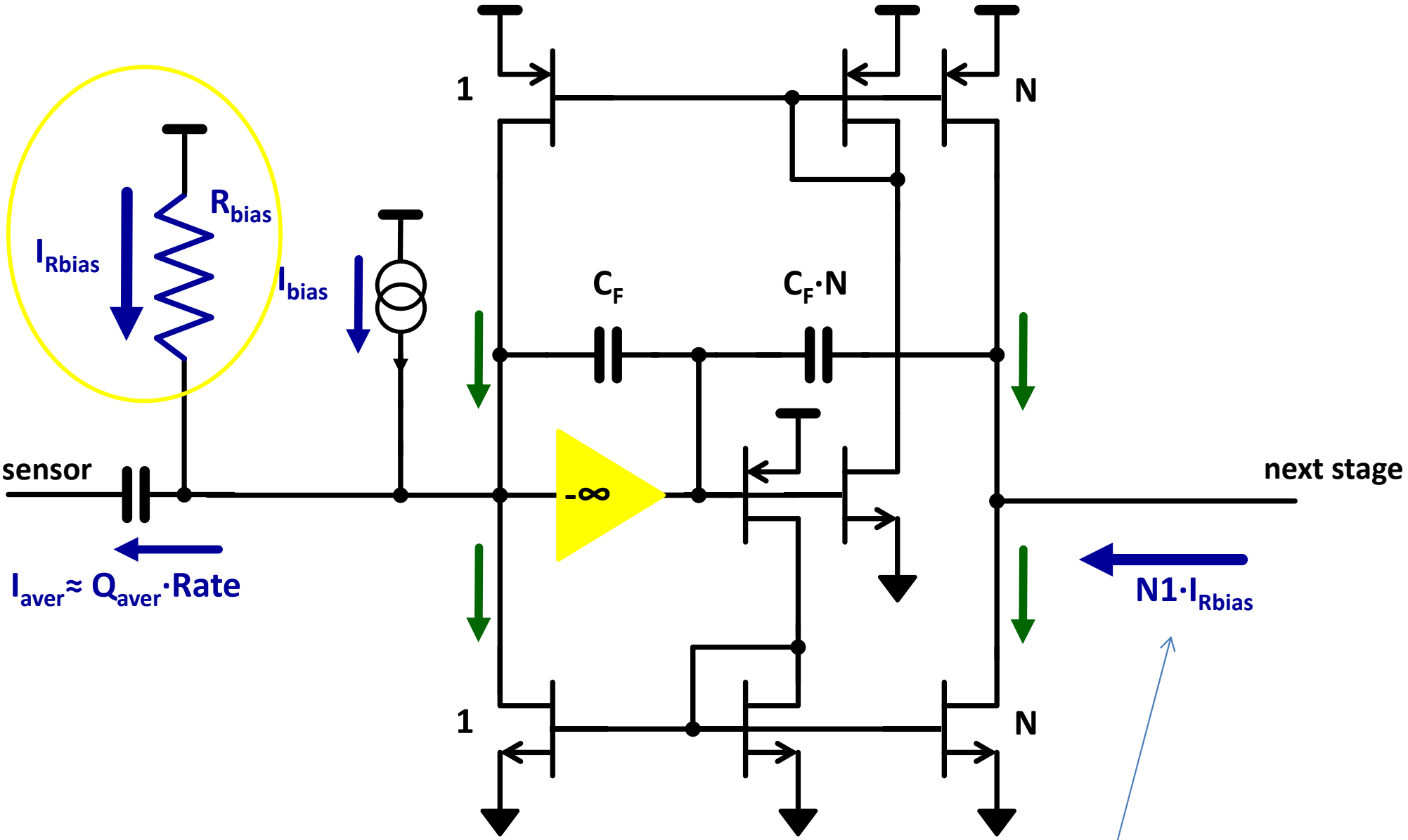
* previously called Dynamic Discharge



mismatch → uncontrolled bias current to next stage

→ ~40% of the channels shut down

Workaround for SFM Issue



external bias current (few nA) → correct polarity is re-established

Summary of SFM Issue - Part 2

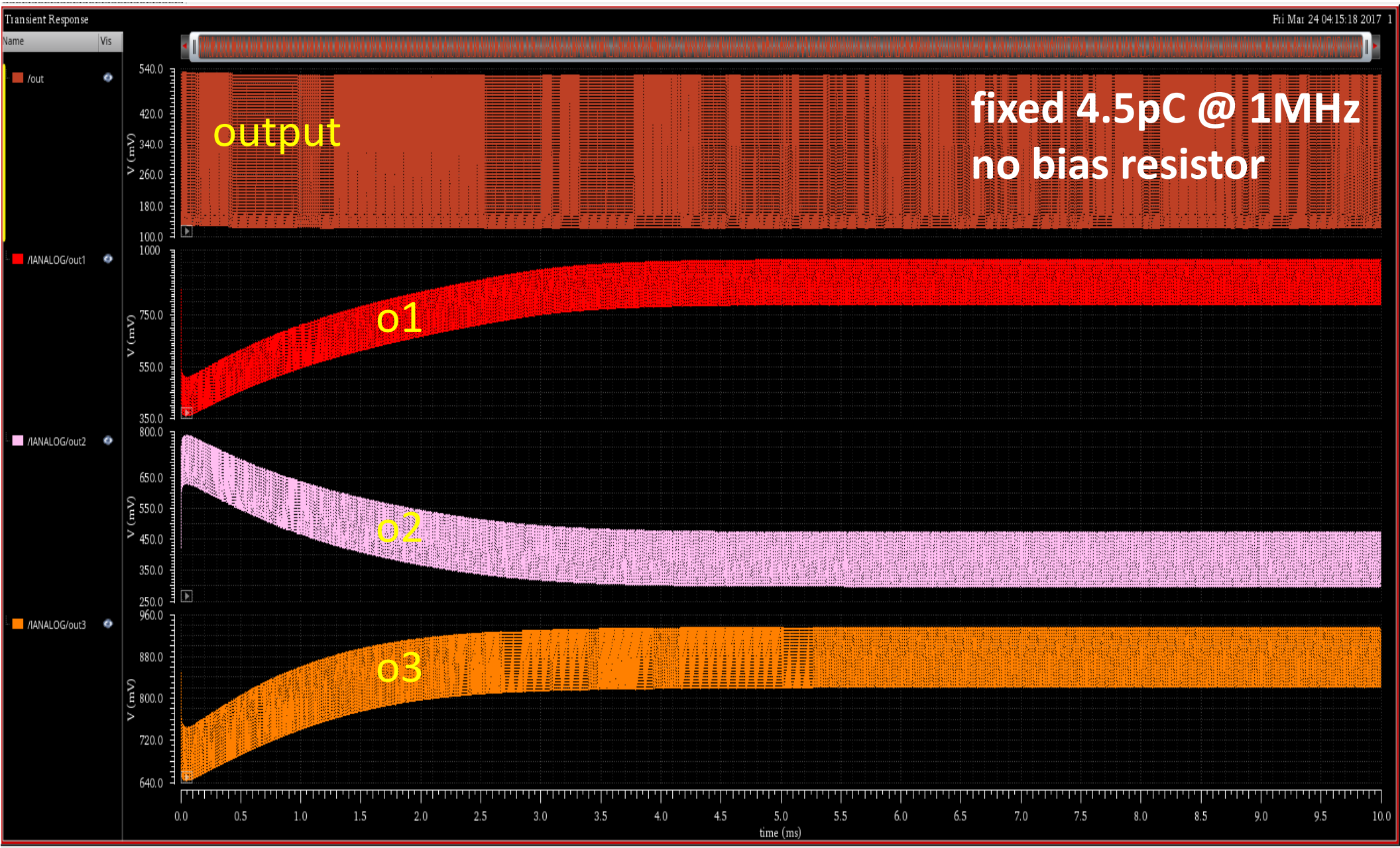
- **Issue** - Given a "good" (in SFM mode) channel, dead time occurs with actual charge distribution

- **Origin** - Non-linearity of active reset combined with charge distribution

- **Workaround** - External bias resistor (same as before)

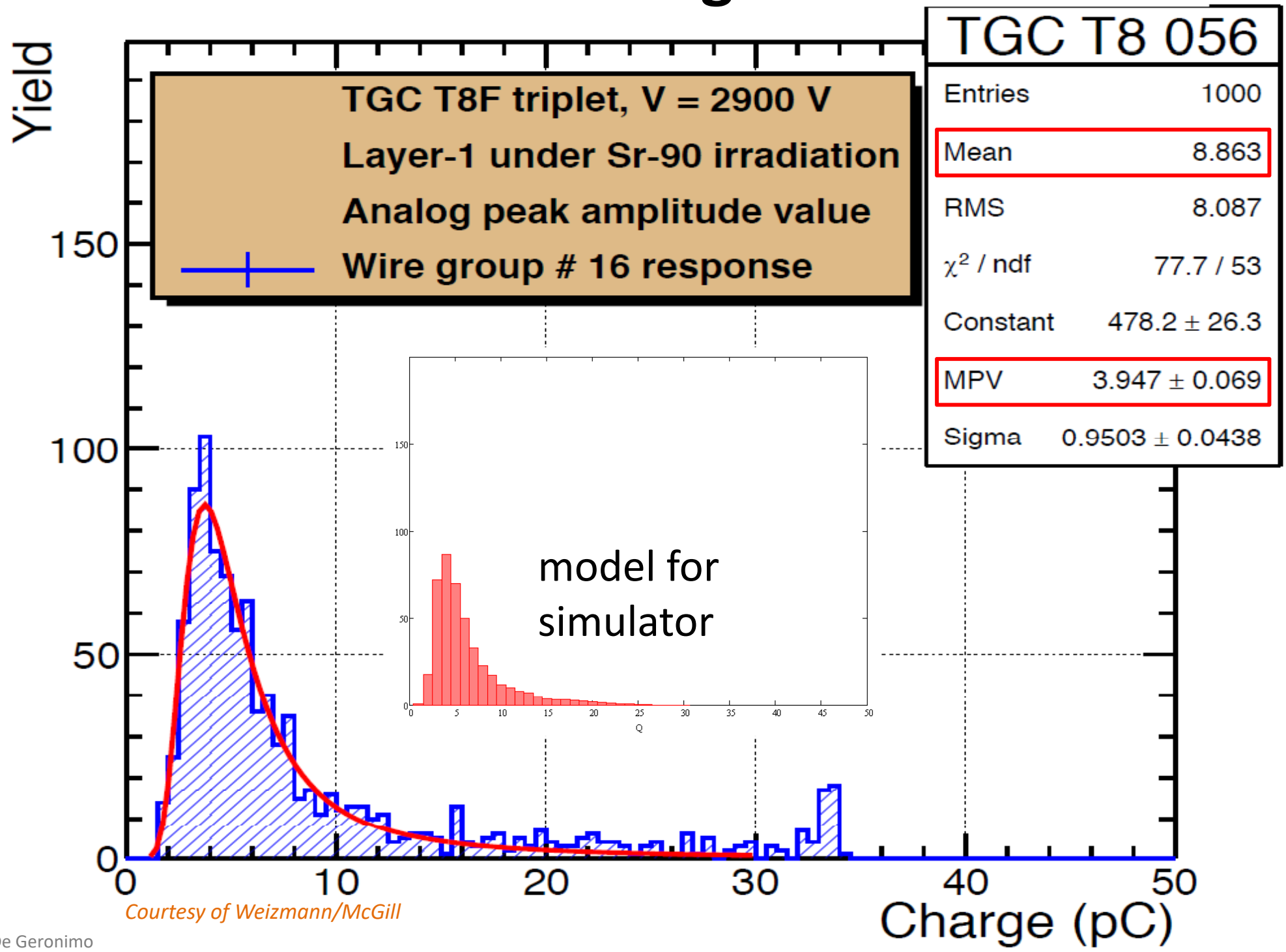
- **Fix** - Increase value of bias current in SFM mode (same as before)

Pad Simulation 4.5pC @ 1MHz - No Resistor



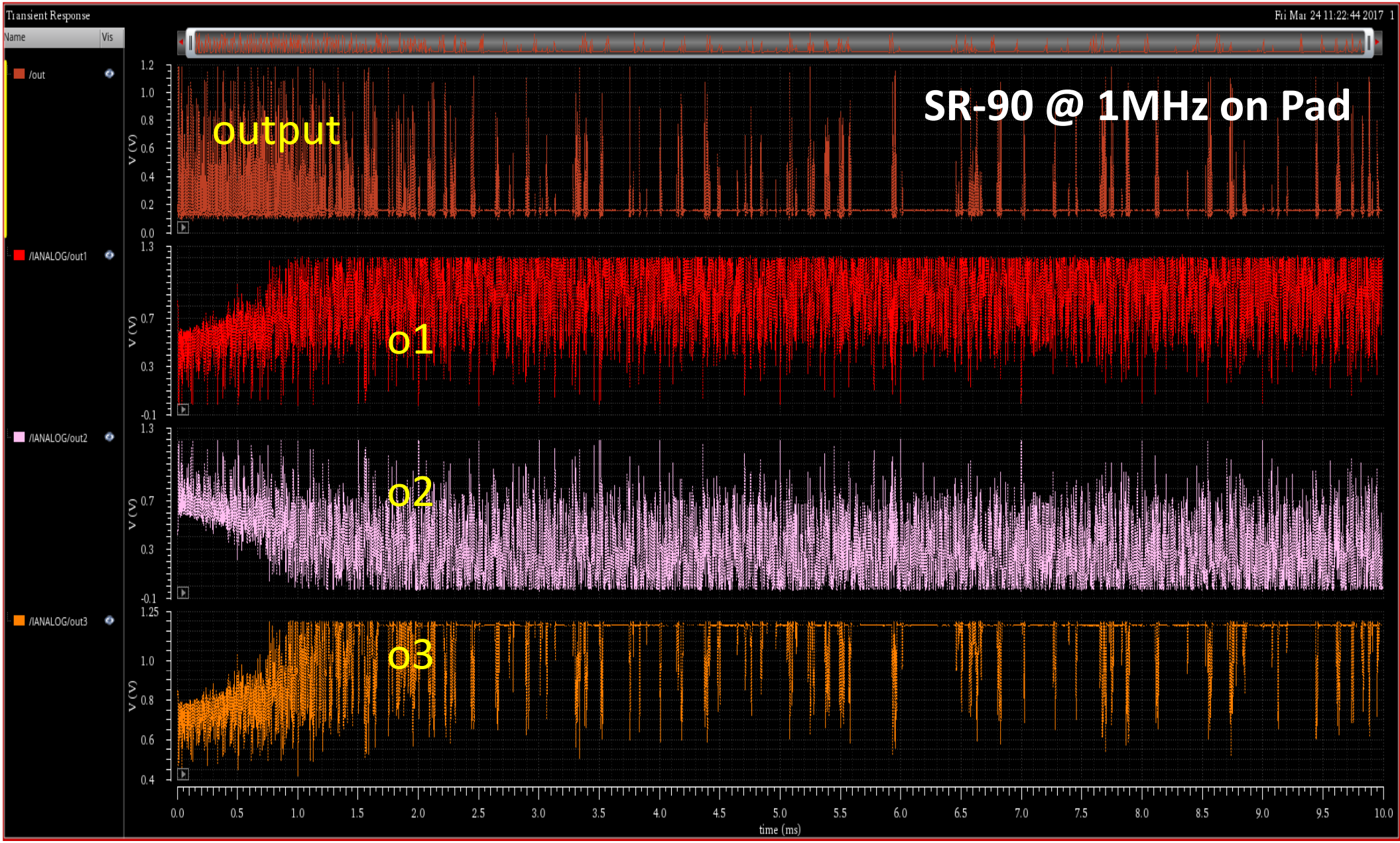
3pC were specified

Strontium-90 Charge Distribution



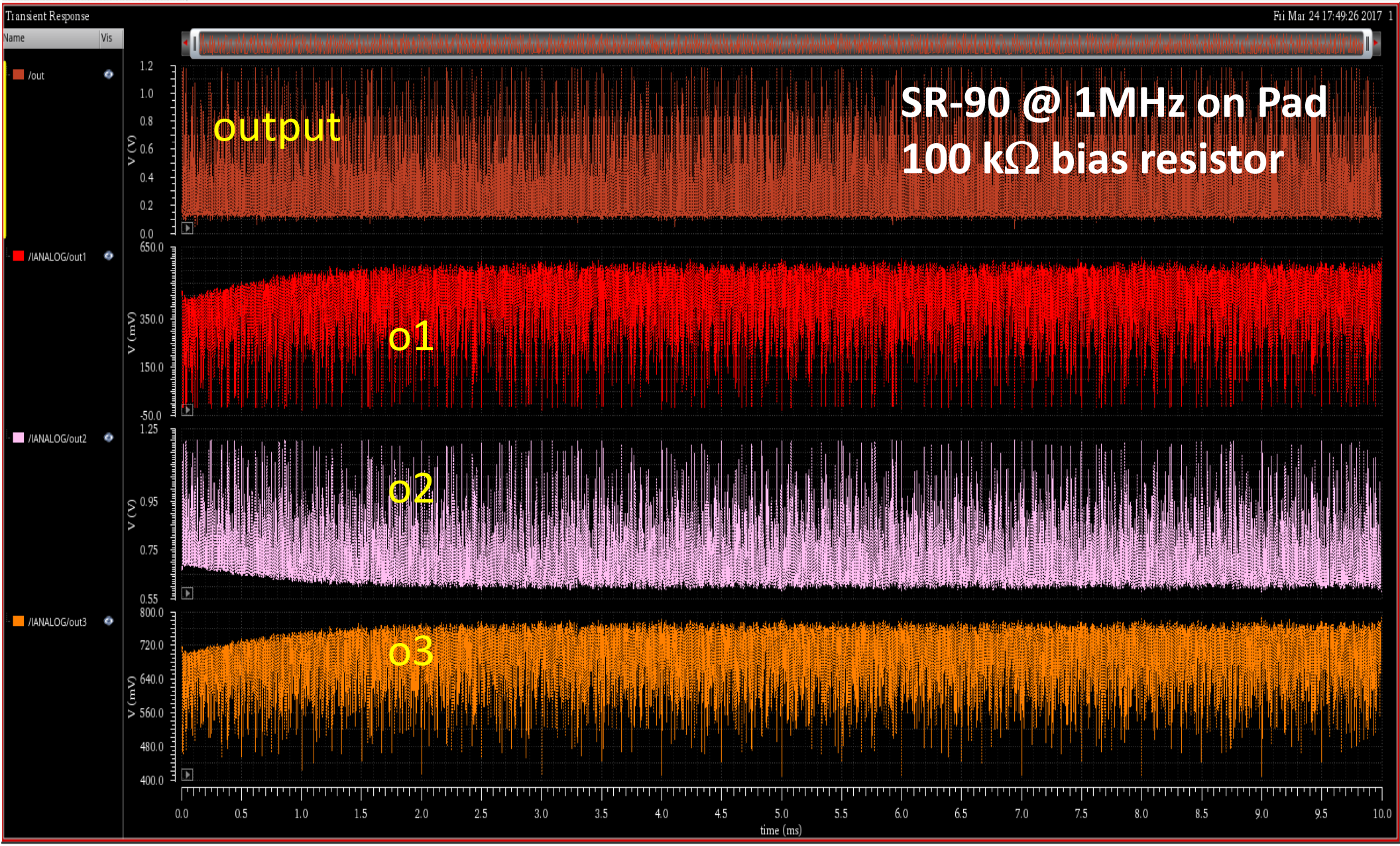
Courtesy of Weizmann/McGill

Pad Simulation SR-90 @ 1MHz



Stage 3 fails due to non-linearity of active reset (no SFM)

Pad Simulation SR-90 @ 1MHz - 100kΩ Resistor



$R_{bias} \approx 100k\Omega$ adjusts operating points and compensates for I_{aver}

Choice Criteria for Bias Resistor

- When in SFM mode, VMM3 is able to sink or source DC currents up to 10 µA, but conservatively 5 µA must be assumed
- As a rule of thumb, the current provided by the bias resistor must have same polarity of the charge with values on the order of the worst-case <Q>×Rate product, and not exceed 5 µA
- Worst-case <Q>×Rate products higher than 5 µA must be handled with the attenuation network (π-network) as discussed later, to limit the effective average current within 5 µA
- Note1: the DC voltage of the VMM3 inputs is on the order of 300mV. In positive mode, the resistor should be placed between VDDP and input. In negative mode between input and AGND. Both VDDP and AGND nodes are available at the protection diodes.
- Note 2: 100 kΩ noise contribution ≈ 880 e^- rms (≈ 0.13 fC)

Summary of SREC Issue

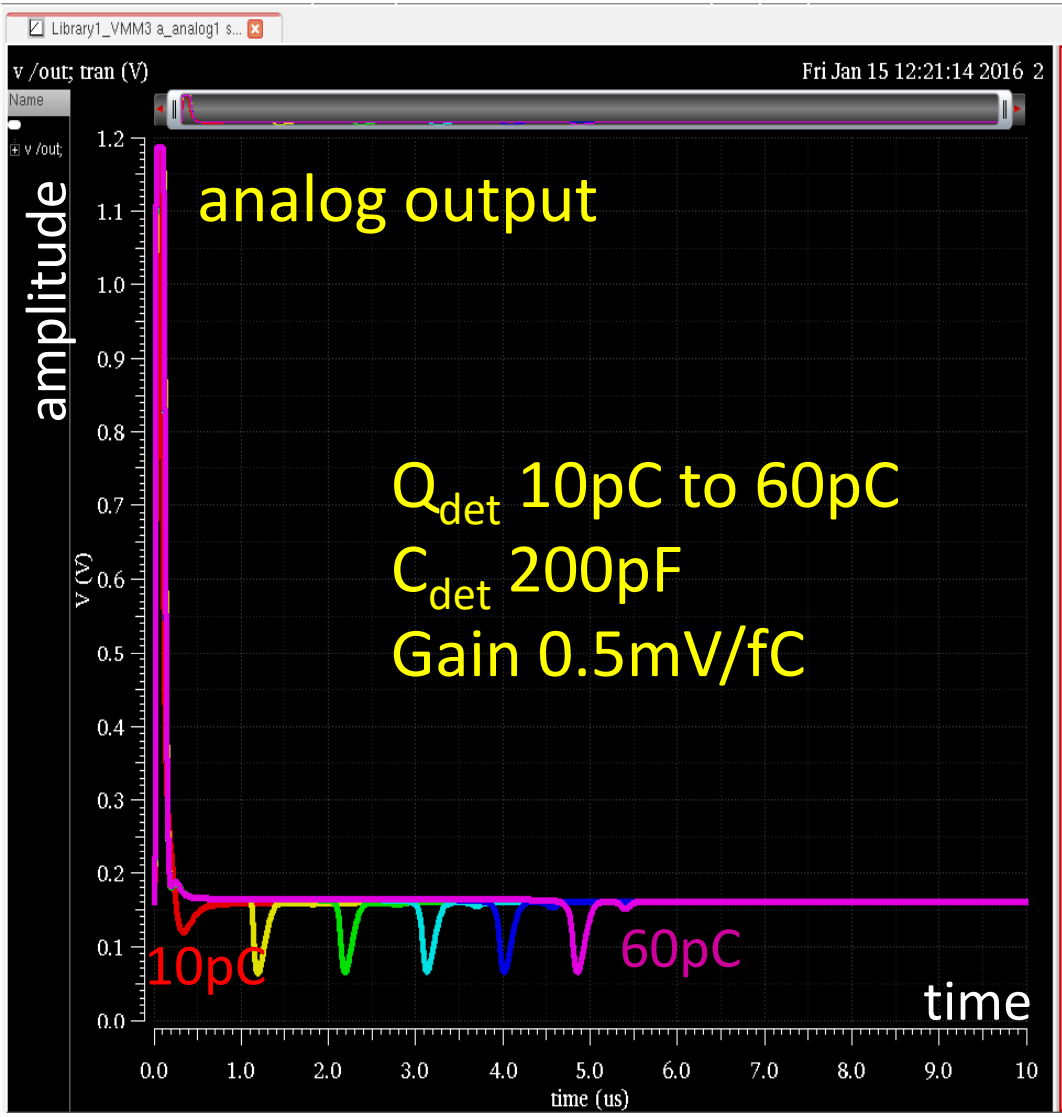
- **Issue** - The fast-recovery circuit, engaged at very-high-charge, may cause multiple threshold crossings

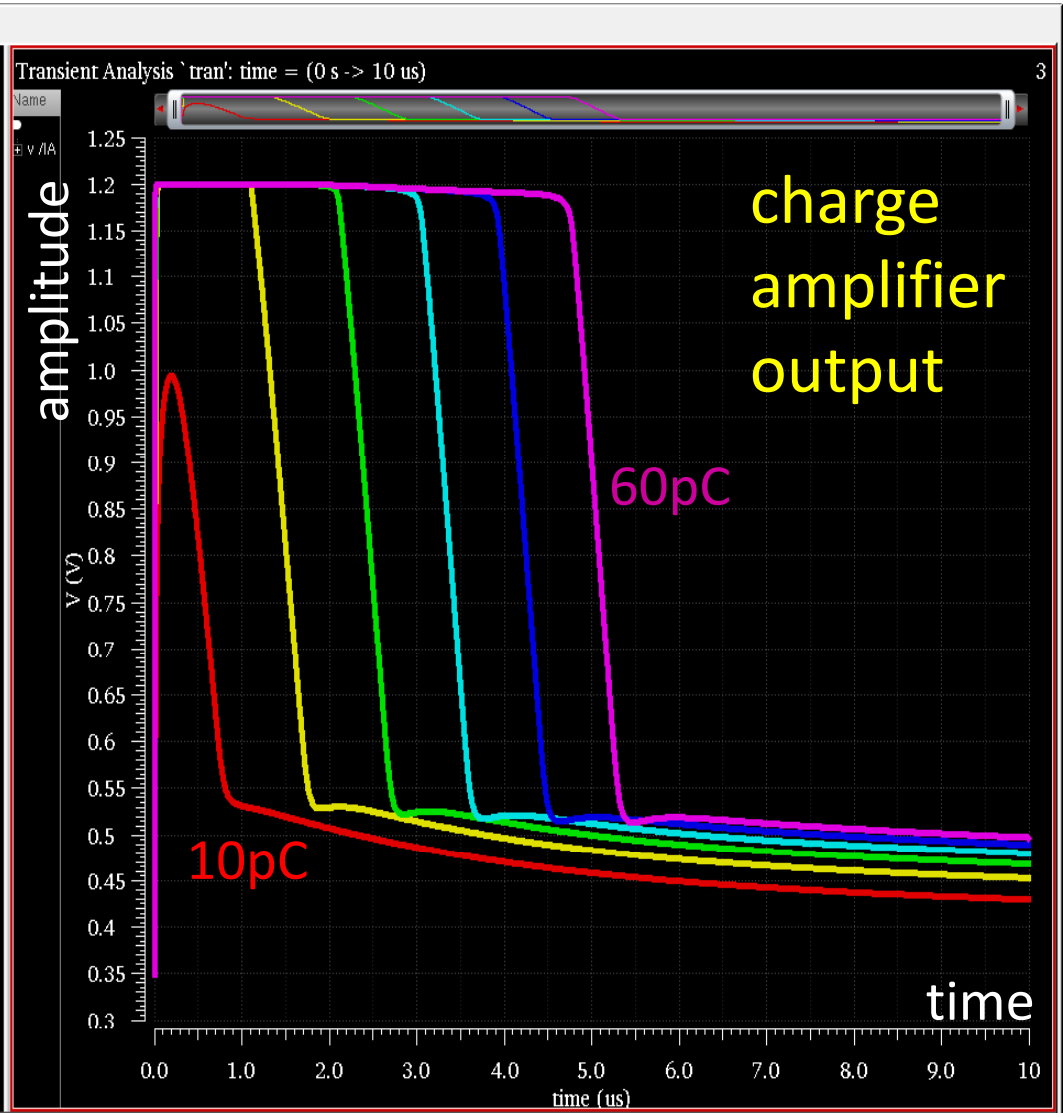
- **Origin** - Parasitics

- **Workaround** - Disable SREC or reduce number of very-high-charge events

- **Fix** - To be investigated (ASIC, package, PCB)

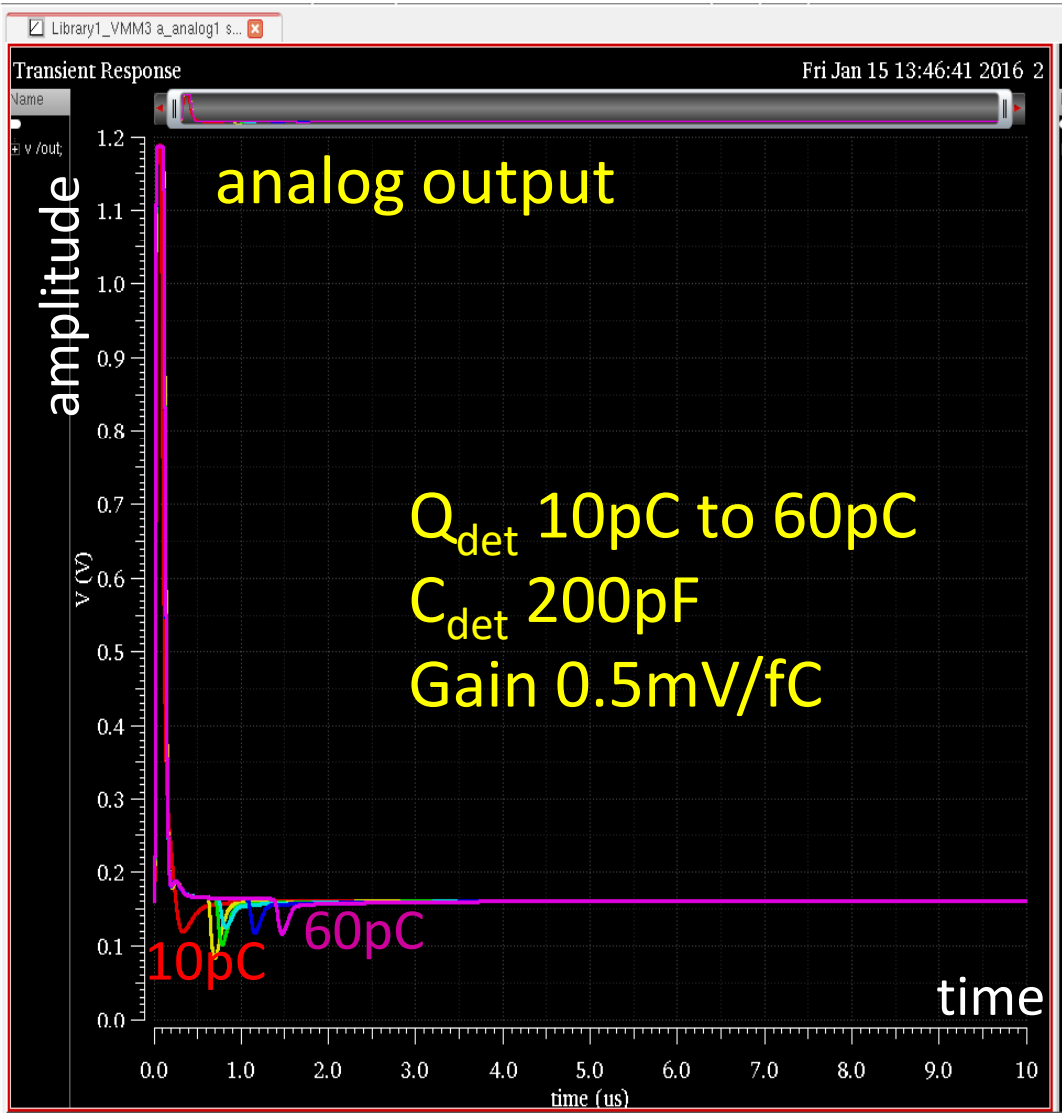
Response Without SREC

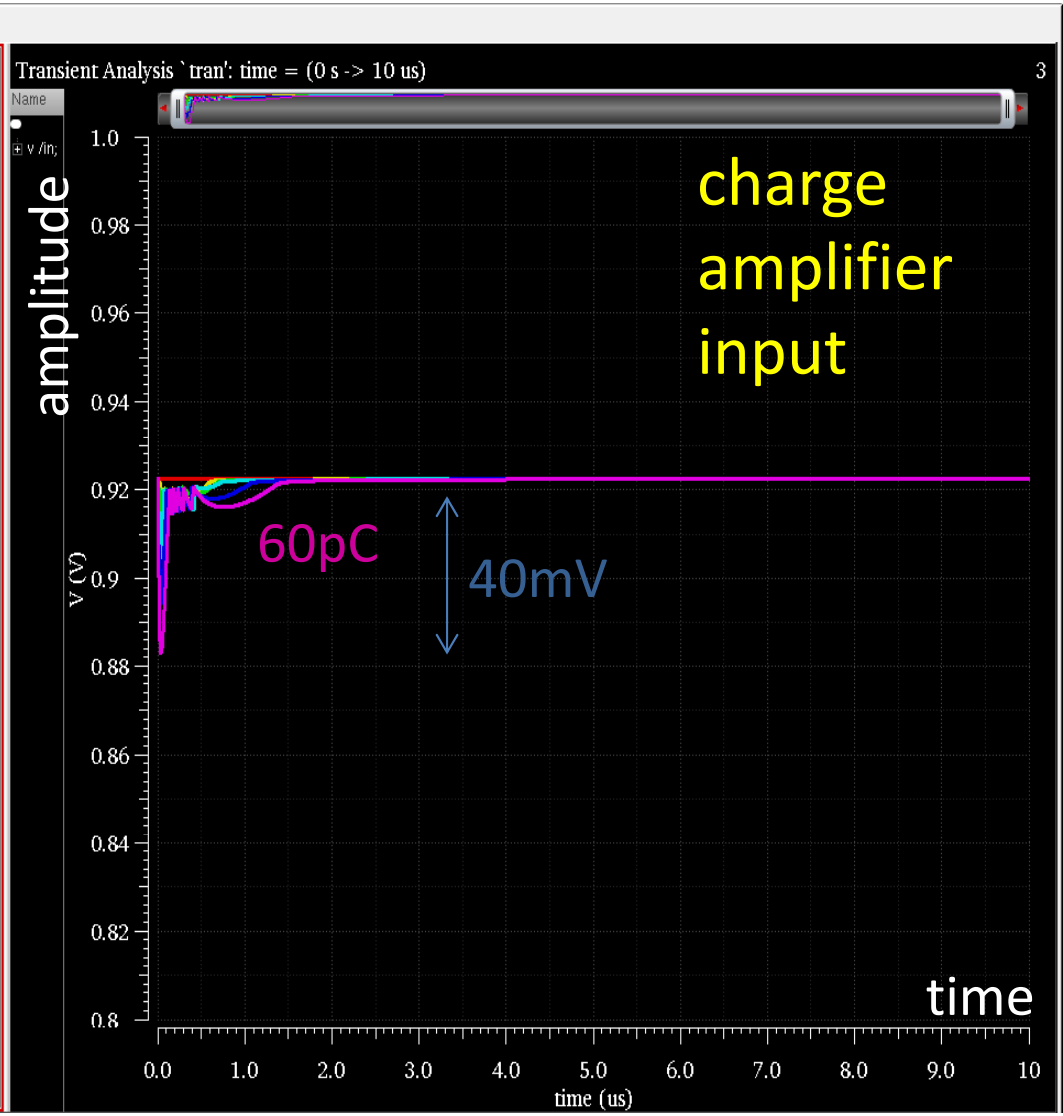




- **Saturation of the charge amplifier extends to 2µs at 20pC and 6µs at 60pC**
- **Similar behavior is obtained for positive charges**

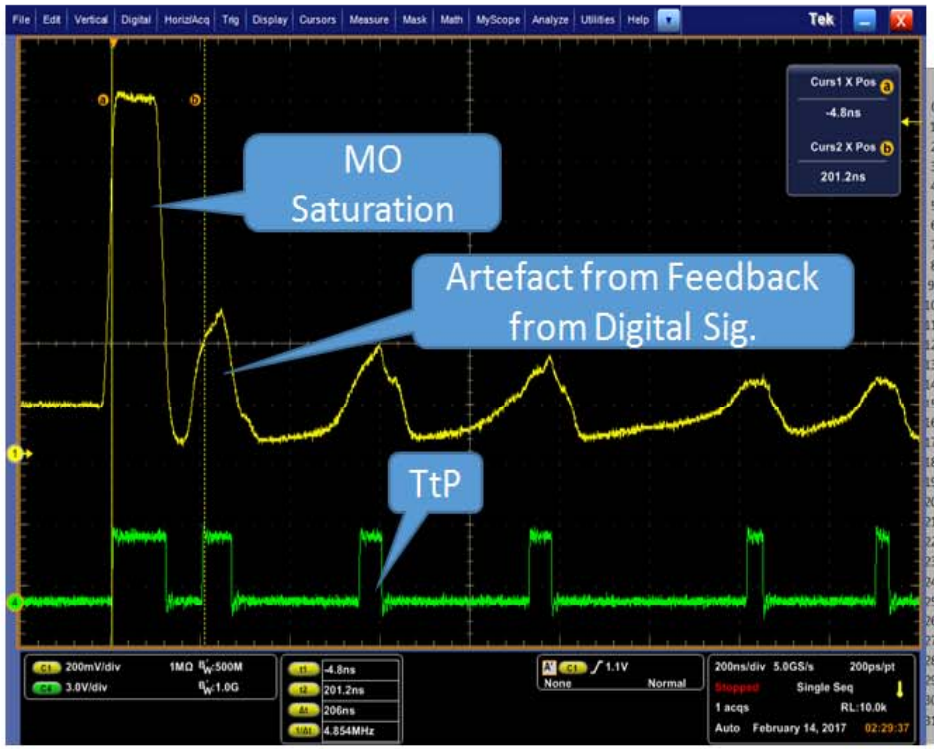
Response with SREC

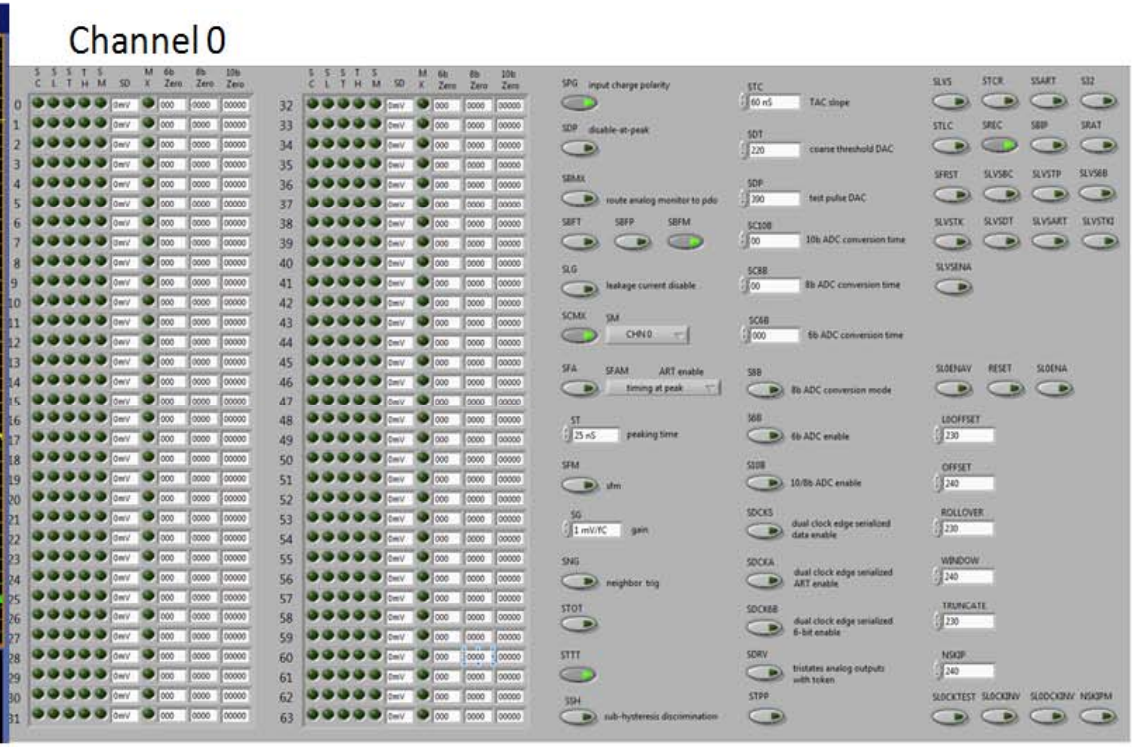




- **With the fast recovery circuit enabled, the saturation of the charge amplifier is reduced to 1.2µs at 20pC and 2µs at 60pC**
- **Similar behavior is obtained for positive charges**

Measurement with SREC





Recovery from Saturation Response 205 ns.

Low Discrimination Level 220 .

Courtesy of Technion (N.Lupu)

- **Effect first reported by Technion (pulser), much smaller at Weizmann**
- **Due to external parasitics, needs investigation (PCB), risk of cross-talk**

This may require disabling SREC and/or attenuating

Original Specs

3 Wire Signals

1. The VMM should recover from wire signals of $\langle Q_w \rangle = 6$ pC within 200 ns.
2. The linearity is not a critical factor here; however it is desirable for the linearity up to 2 pC to be known in order to apply offline corrections.

4 Pad Signals

1. In ADC mode, the VMM should recover from pad signals of $\langle Q_p \rangle = \langle Q_w \rangle / 2 = 3$ pC within 250 ns.
2. The linearity is not a critical factor here; however it is desirable for the linearity up to 2 pC to be known in order to apply offline corrections.
3. In direct-timing-only mode (Time-over-Threshold and 6-bit ADC):
    a. if the pulse charge is less than 6pC, the dead time shall be 60 ns after the trailing edge of the ToT pulse or 60ns after the readout of the last bit.
    b. if the pulse charge is more than 6pC, the dead time shall not exceed ~1 µs from the peak.

5 Strip Signals

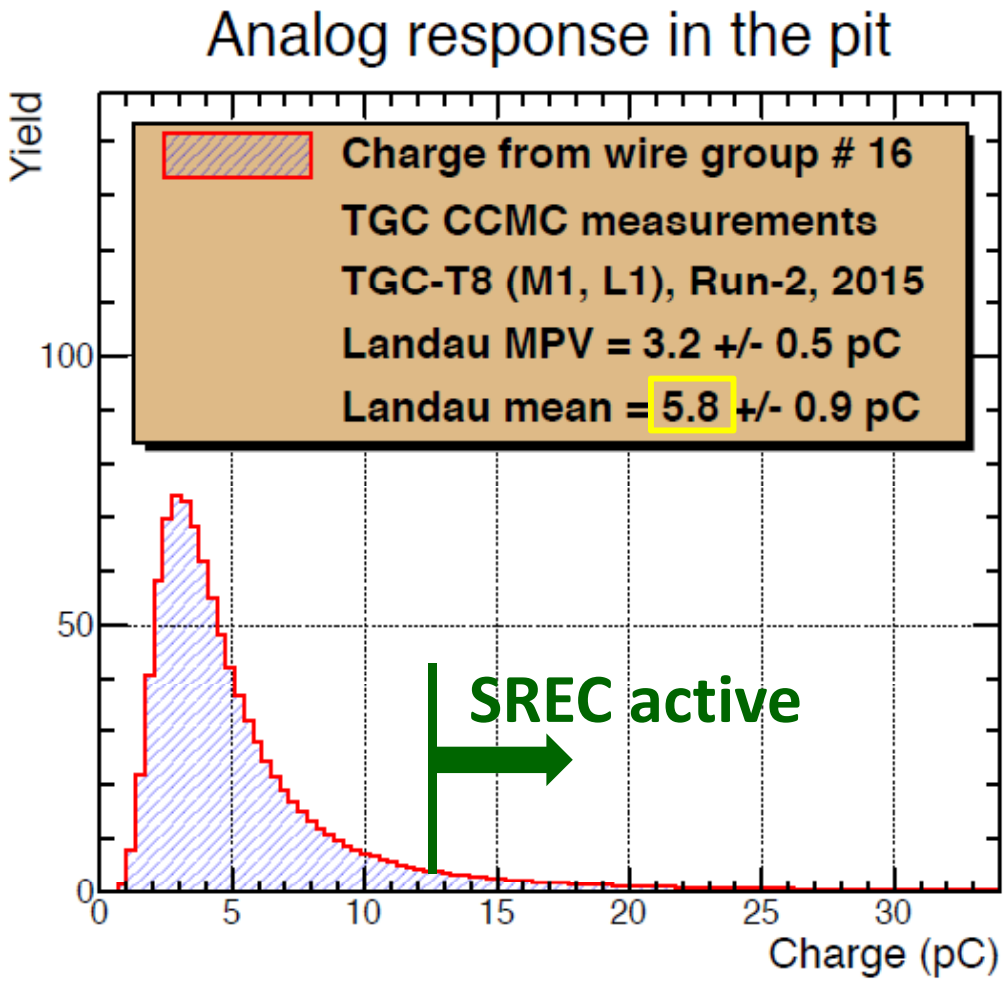
1. The VMM should recover from strip signals of $\langle Q_s \rangle = \langle Q_w \rangle / 6 = 1$ pC within 200 ns. The factor of 6 comes from the assumption that the signal will be distributed over three strips on average.
2. Linearity within ± 2% up to 2 pC is required.

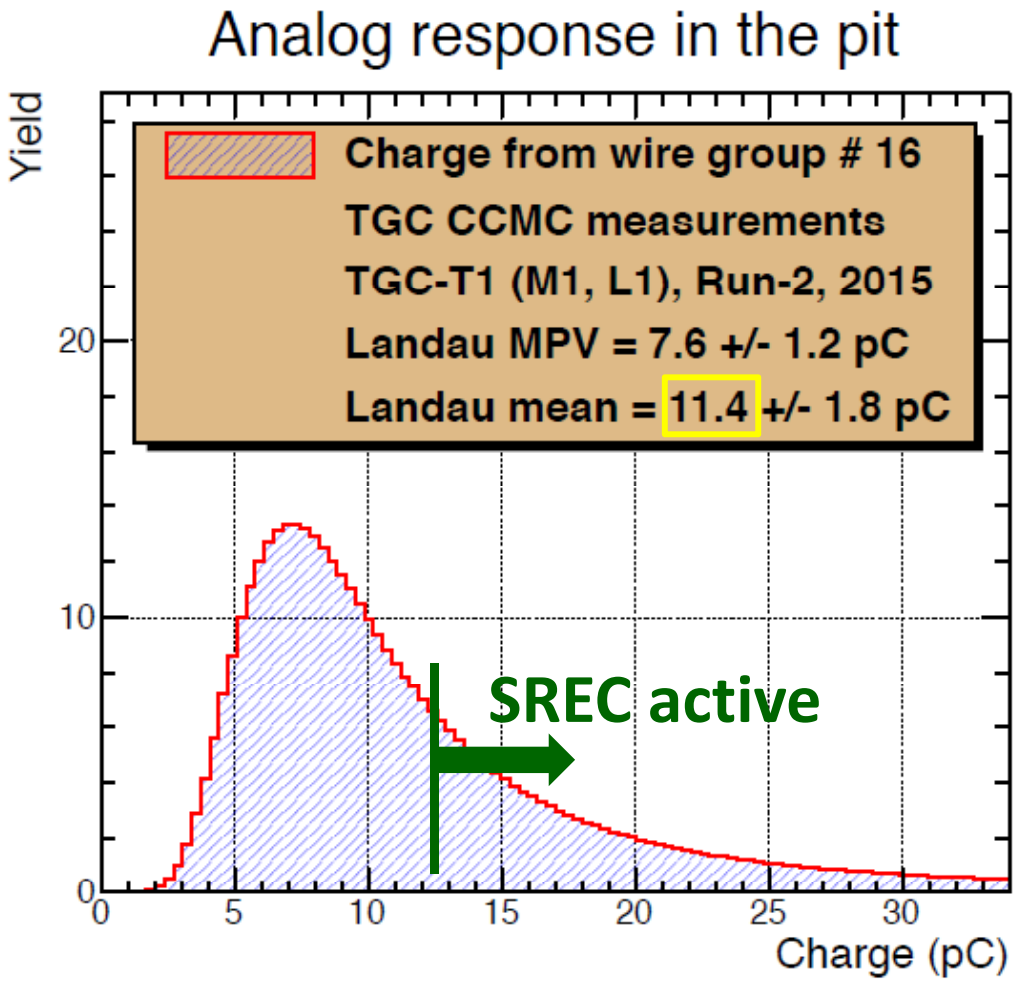
7 Rate per VMM

1. The expected/estimated maximum rate at luminosity of 7×10^{34} is 0.8 MHz per VMM channel for pads and 0.9 MHz per VMM channel for strips. An average strip multiplicity of 4.7 is assumed in this, including from neighbour-on mode. A value of 4.7 is on the considered to be on the high side, compared to data from the FNAL 2014 test beam which indicate an average of 4.2. The difference between the 2 numbers is kept as safety margin.

Example of simulation from Weizmann

- preliminary -

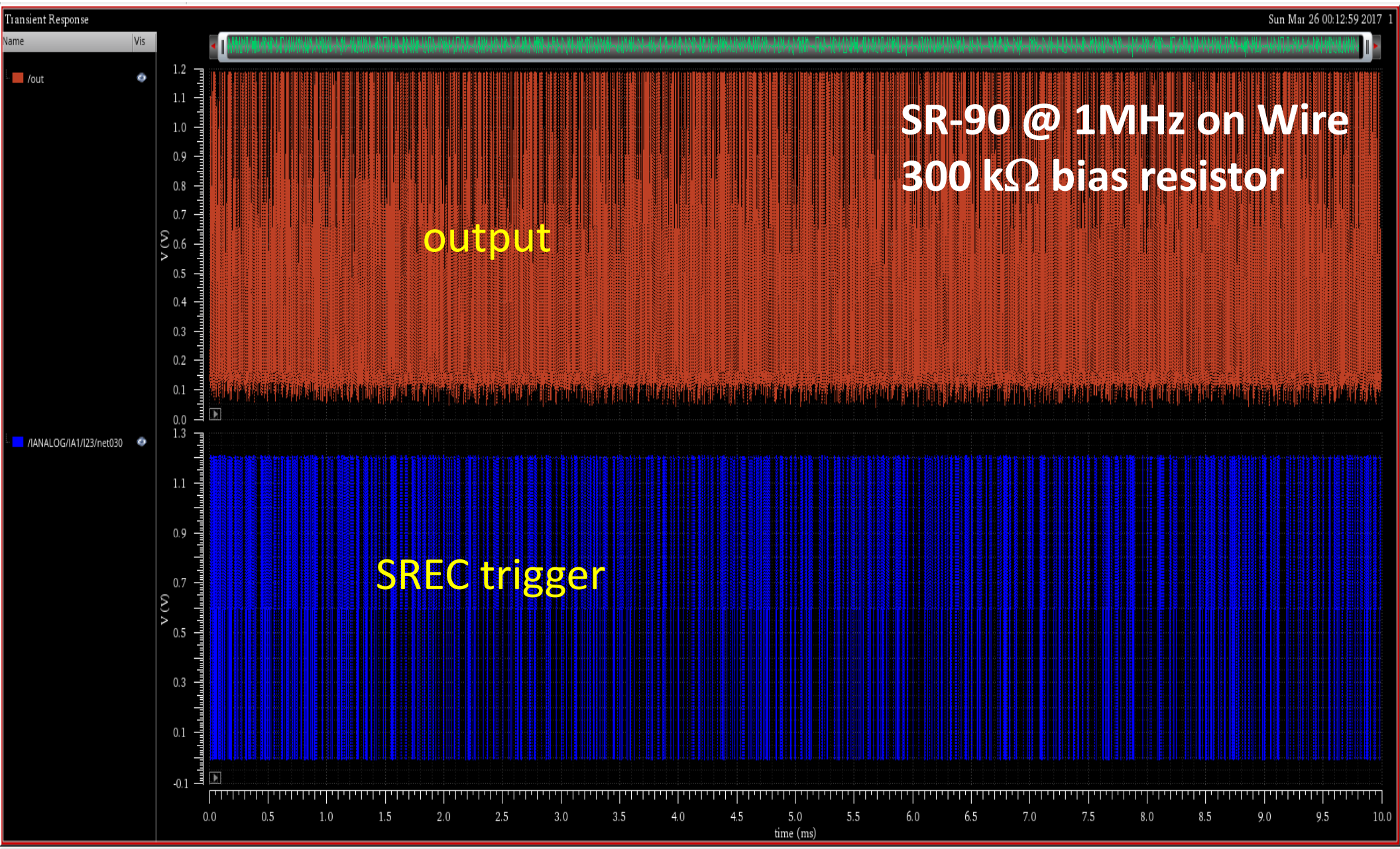




Courtesy of Weizmann

Charges up to ~12 pC, Rates up to ~1.5 MHz (~18 µA)

Wire Simulation SR-90 @ 1MHz - 300kΩ Resistor



Are Bias Resistors Enough?

• Input **bias currents (resistors) can reduce the dead time to very few % at most**, verified with average rates in excess of 1 MHz and average charges in excess of 15 pC.

• However, **the VMM3 internal nodes are still subject to excessive excursions**. Additionally, parasitic effects associated with high charge and fast-recovery circuit can cause **multiple triggers and cross-talk**, and it should be kept to a minimum.

• Critical: **Wires may exceed 10µA and can't afford frequent loss of virtual ground**.

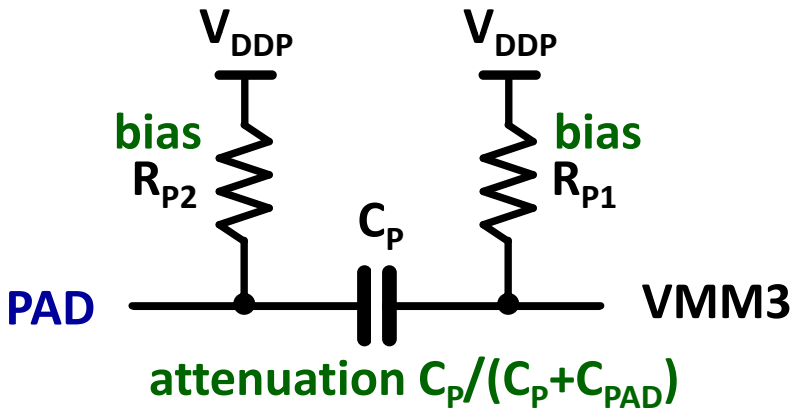
↓

Capacitive Attenuation Networks (π-Networks)

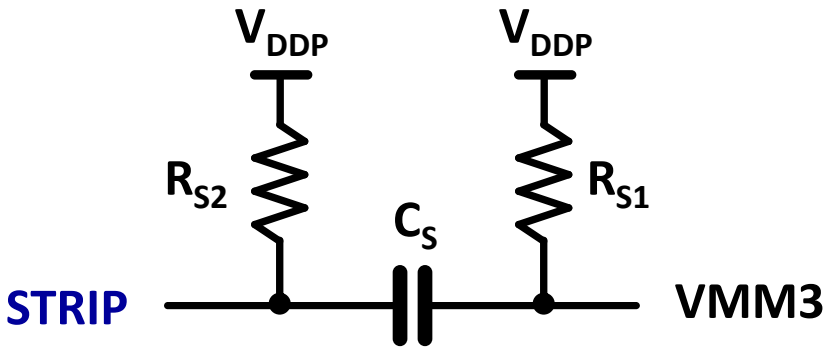
The **π-networks** are designed to keep **VMM3 in a safe linear region** for most of the measurement, and to **minimize the engagement of the fast recovery circuit**.

- **Minimum size for integration in FEB** near the ESD protection circuit.
- **Increased protection** and **lifetime** of the front-end.
- **Very modest impact on S/N ratio**, increase in ENC **within 1fC**.
- **VMM gain can be increased** as needed.
- **Attenuation values** will come from **simulations and measurements** done in close collaboration with Weizmann and Technion.

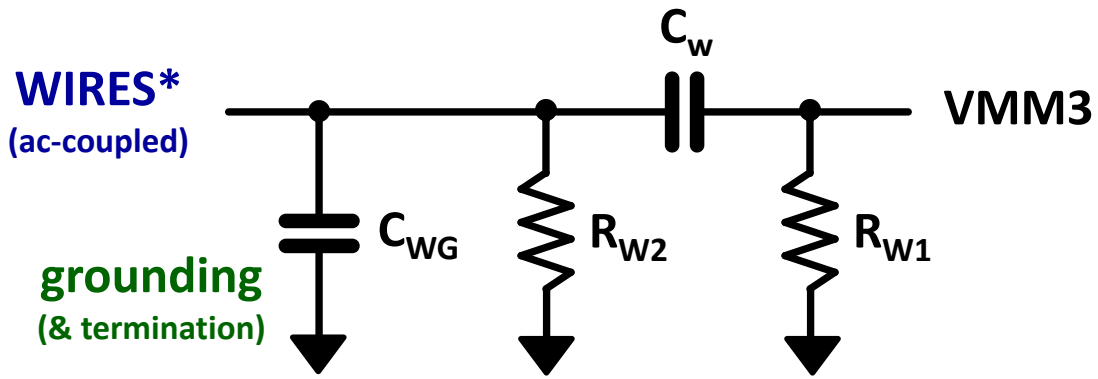
Attenuation Networks (π-Networks)



$R_{P1} \approx 300\ k\Omega$, $R_{P2} \approx 300\ k\Omega$
$C_P \approx C_{PAD}/2$ or **100pF** 10V
Attenuation 1/3, can be adjusted
No attenuation → only R_{P1}=100kΩ



$R_{S1} \approx 300\ k\Omega$, $R_{S2} \approx 300\ k\Omega$
$C_S >$ **100pF** 10V
Small attenuation, or none
Beware of inter-strip coupling
No attenuation → only R_{S1}=100kΩ



$R_{W1} \approx 1\ M\Omega$, $R_{W2} \approx 300\ k\Omega$
$C_{WG} \approx$ **1nF** 10V, $C_W \approx$ **200pF** 10V
Attenuation 1/6, can be adjusted
C_{WG} keeps wire impedance low
Controlled termination possible
No attenuation → only R_{W1}=300kΩ

* Alternative CR from Nachman (no C_{WG}) being investigated

Summary of ADC Accumulation Issue 2 (yield)

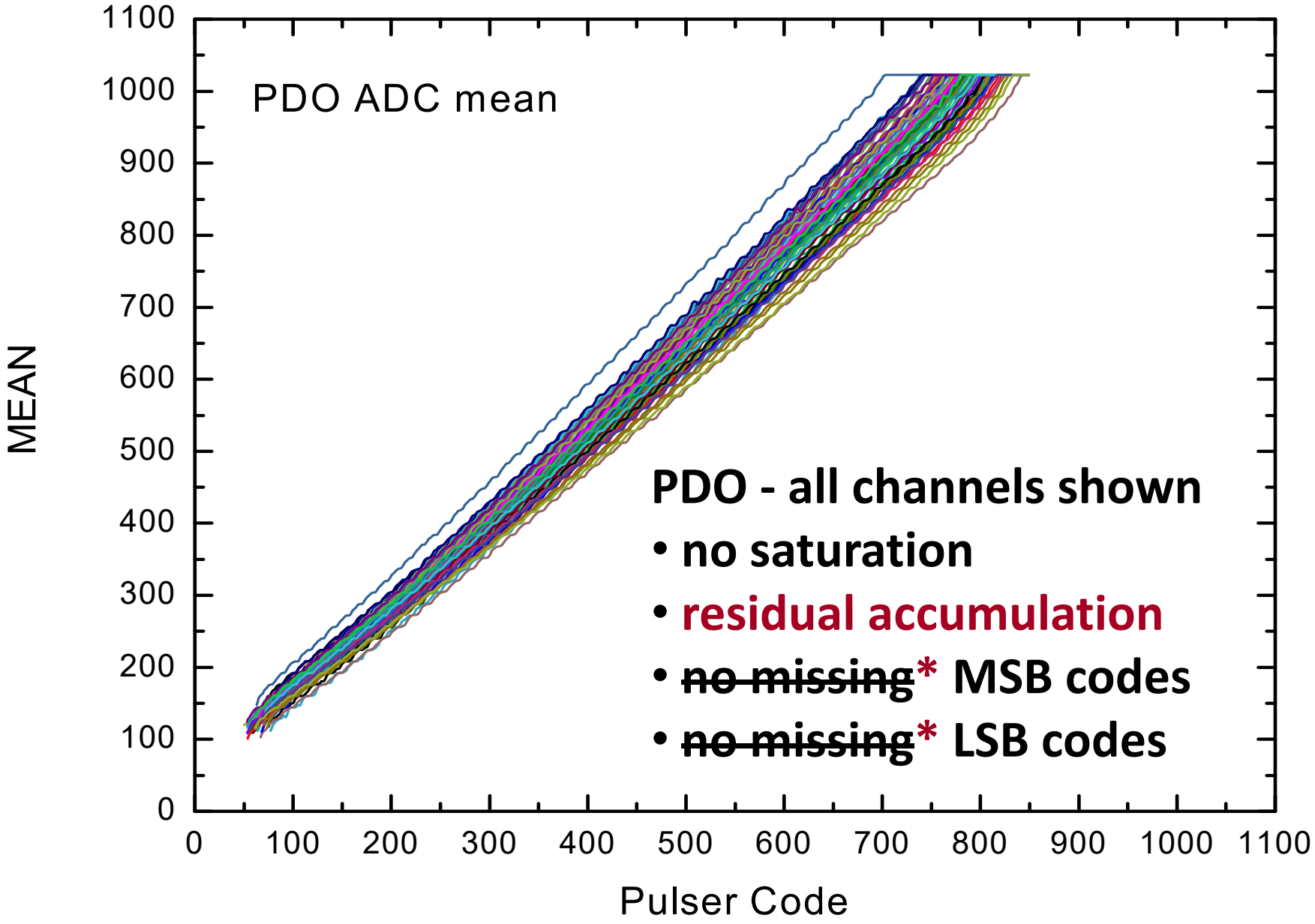
- **Issue** - Both 10-bit ADC (charge) and 8-bit ADC (timing) still present occasional (preliminary ~5%) missing MSB and LSB codes

- **Origin** - Residual mismatch between MSB decision p-MOSFETs

- **Workaround** - None

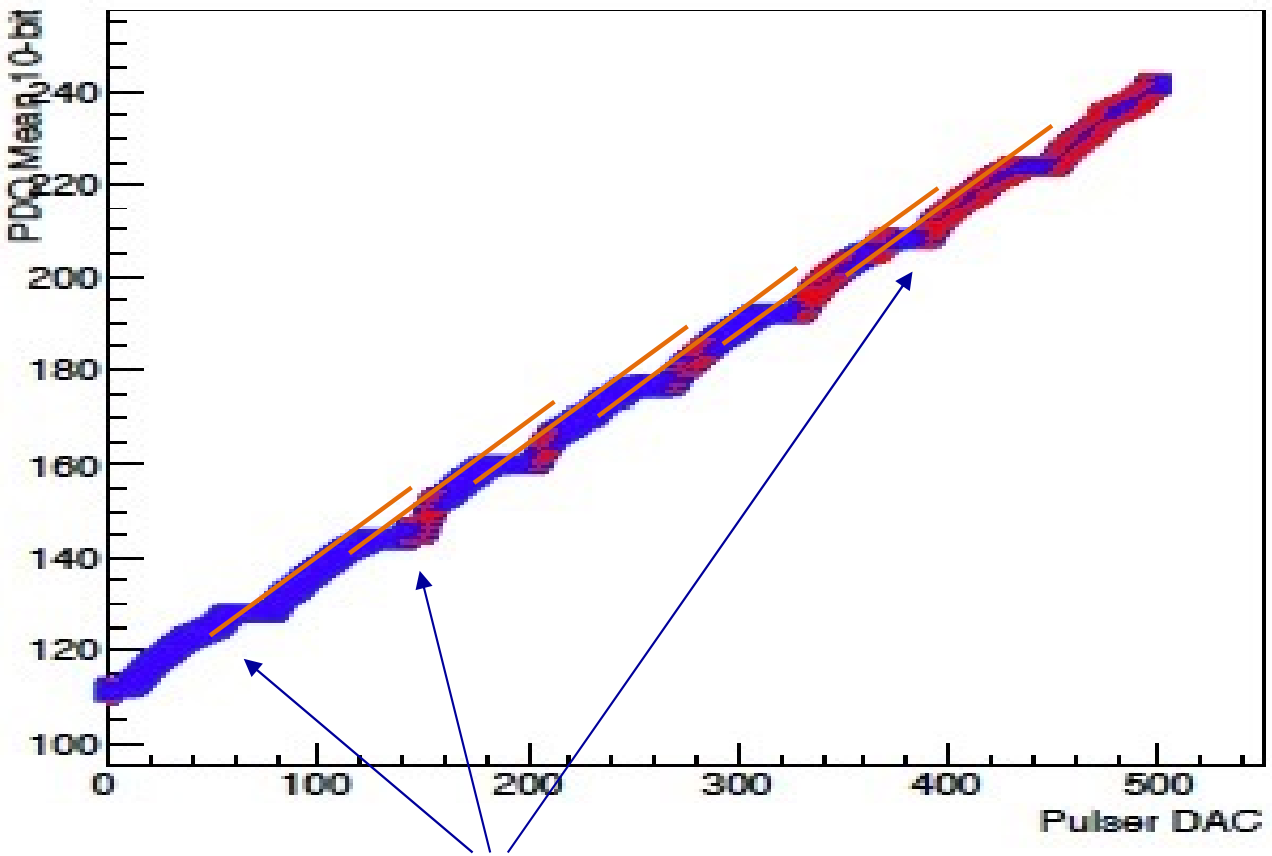
- **Fix** - TBD, simulations queued

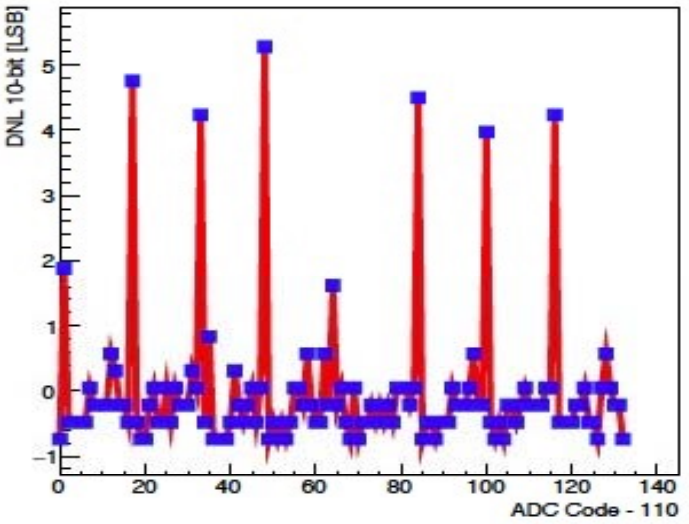
ADC Results in VMM3



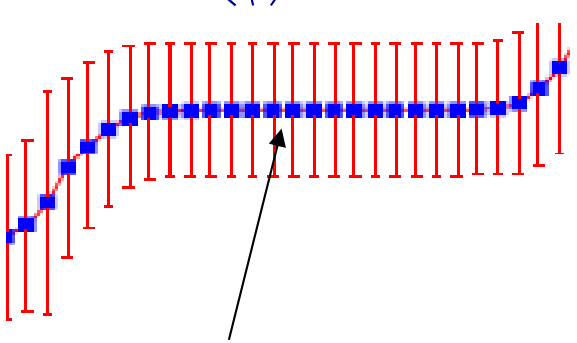
*** occasional missing of MSB and LSB codes still present**

Detail of Residual Accumulation





V. Polychronakos

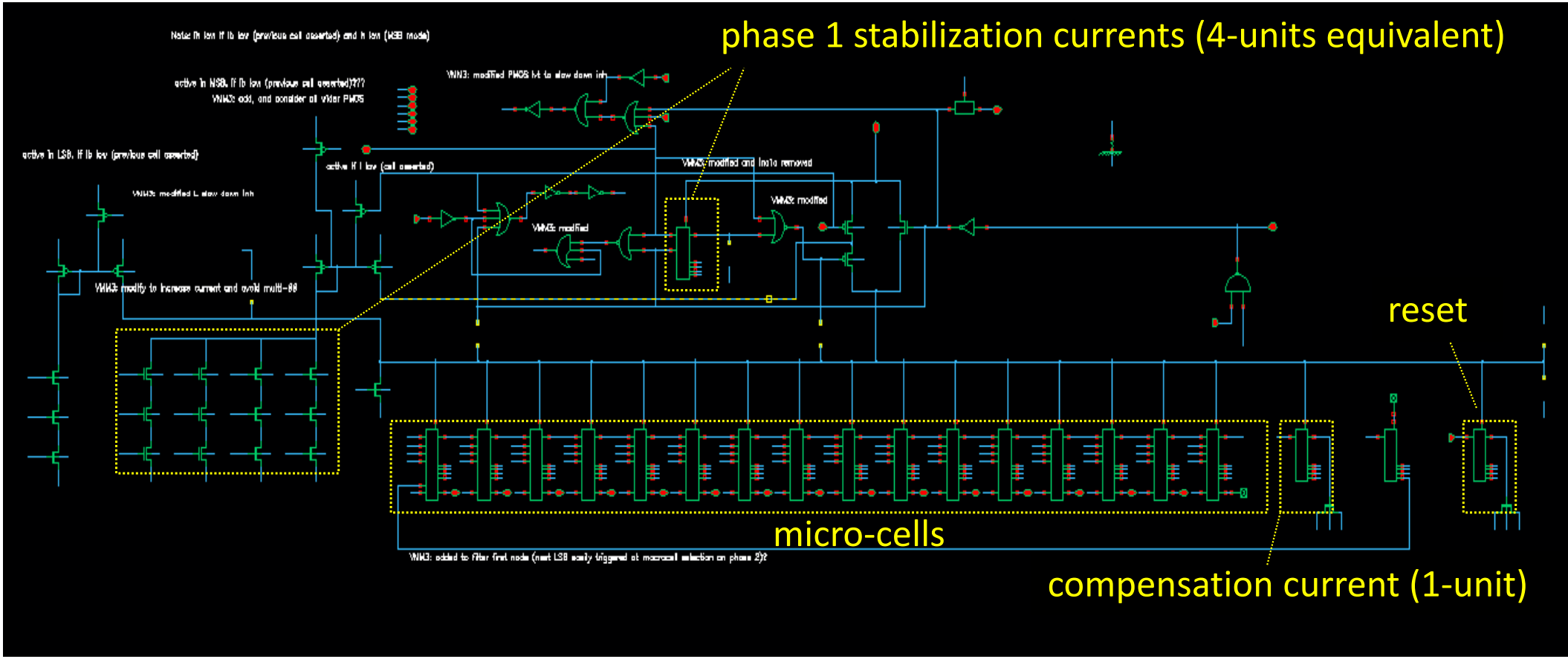


code xxxxxx0000

In phase 2: added parasitic current of ~4 micro-cells → bin ~5 times larger → larger xxxxxx0000 code

Probable Origin of Residual Accumulation

Macro-Cell Schematic

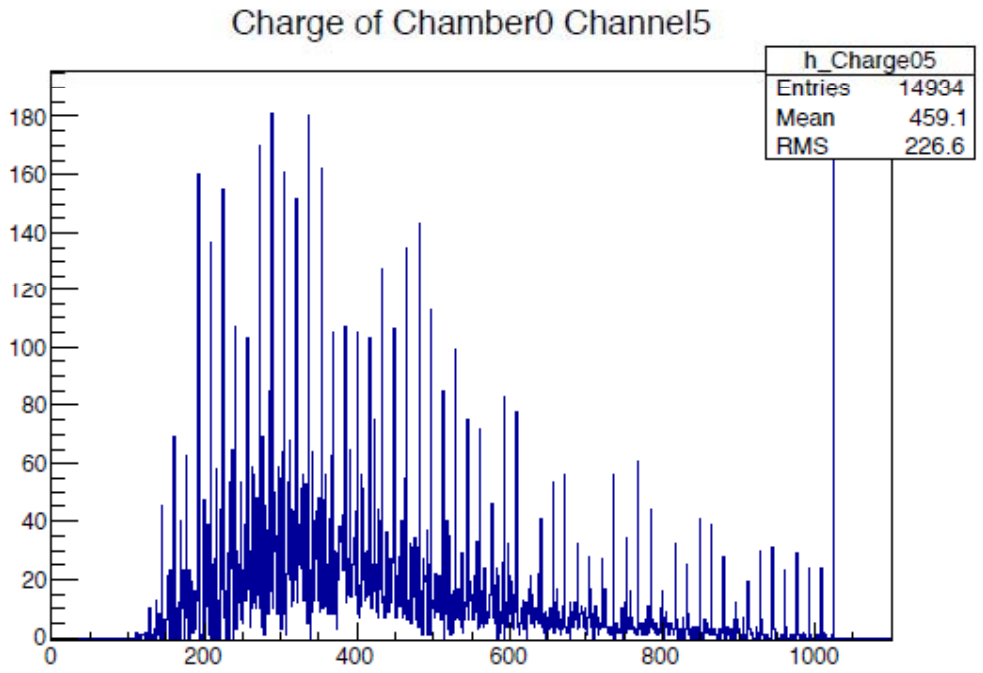


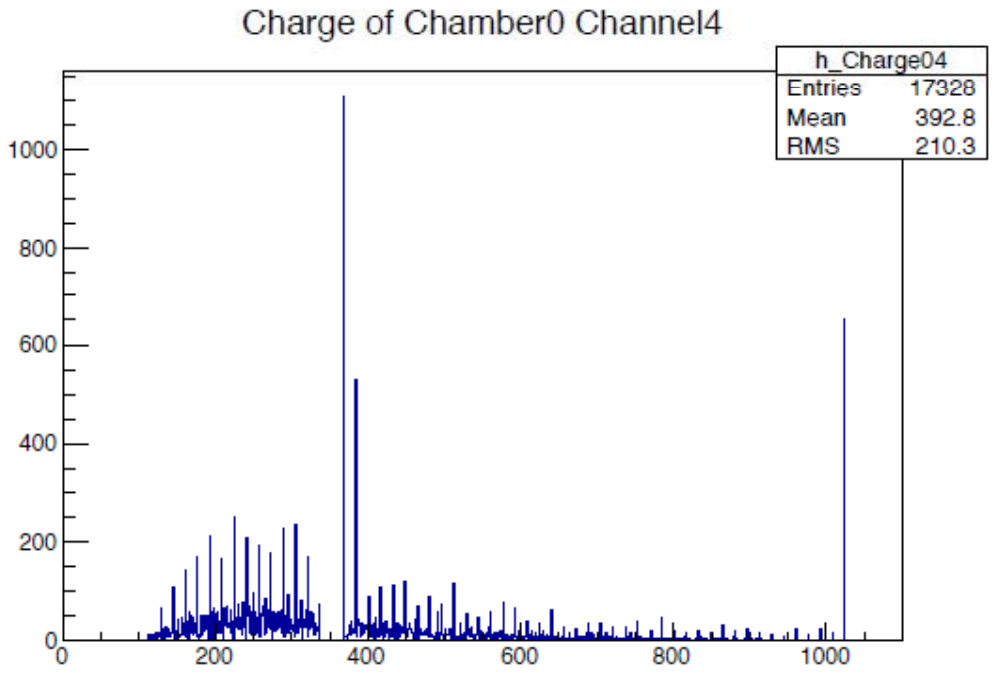
One of the phase 1 stabilization currents remains enabled during phase 2, resulting in the larger code xxxxxx0000

Missing MSB Yield Issue

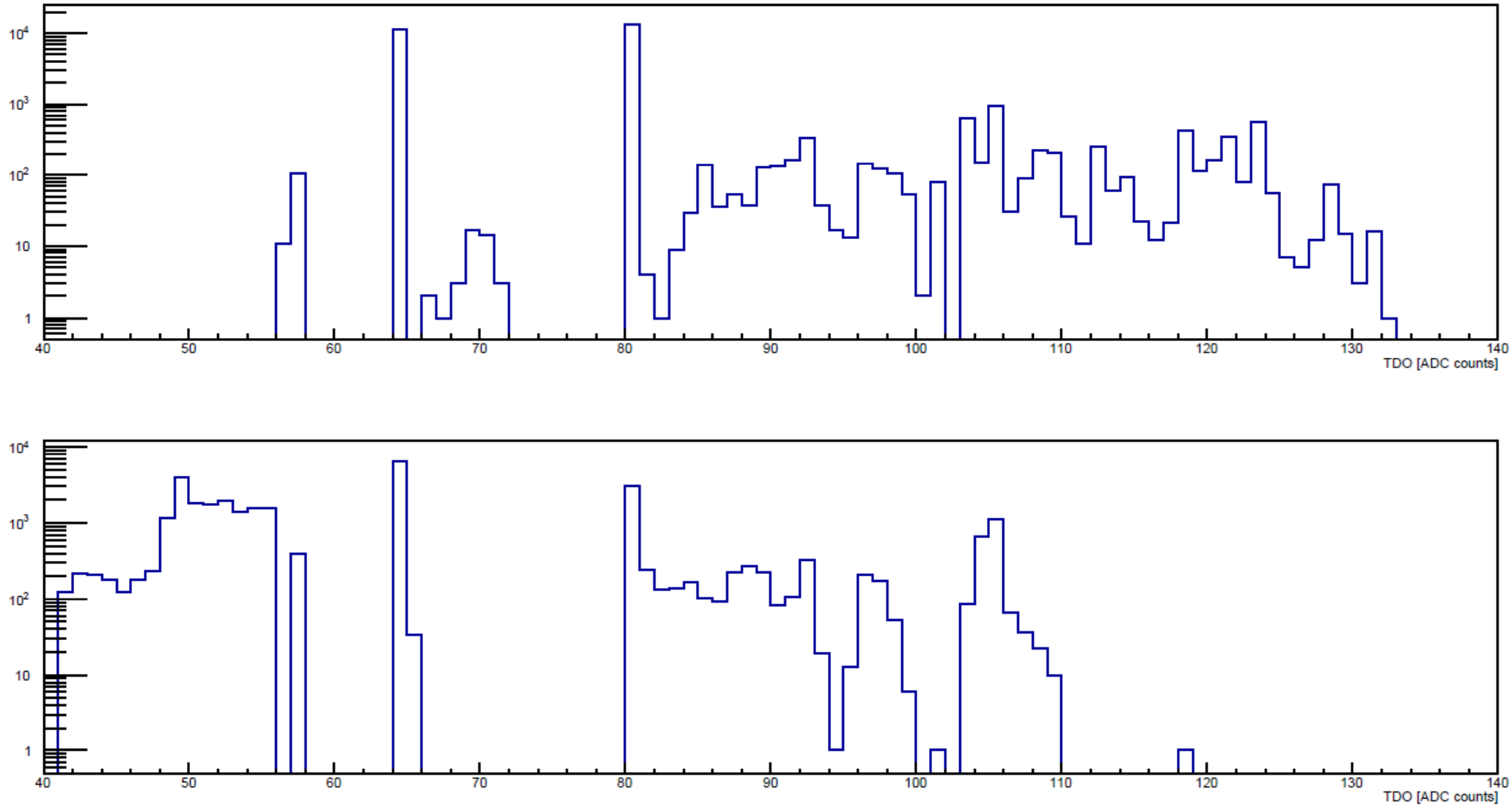
- Data taken with an MDT chamber shows that for some channels there is accumulation different than what was observed before.
- Gap in the distribution shows some macrocells-microcells completely missing while other channels show continuous spectrum.

~ 5% of the channels (preliminary)





Missing MSB Yield Issue

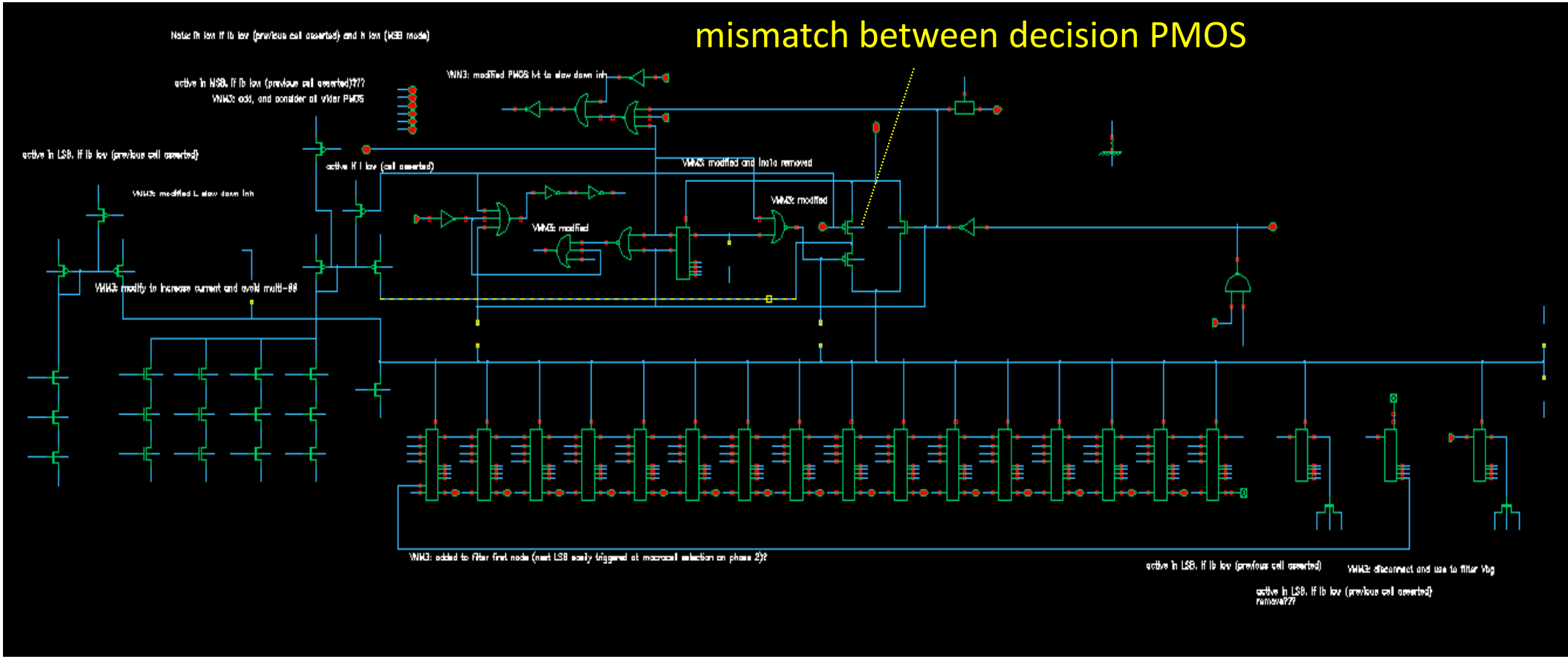


ADC offset does not shift position of missing MSB

→ Mismatch between MSB decision PMOS

Probable Origin of Missing MSB

Macro-Cell Schematic



The decision PMOS is engaged only during the MSB phase. Excessive mismatch can cause selection of more than one Macro-Cell ahead.

Summary of High Baseline Issue 2 (yield)

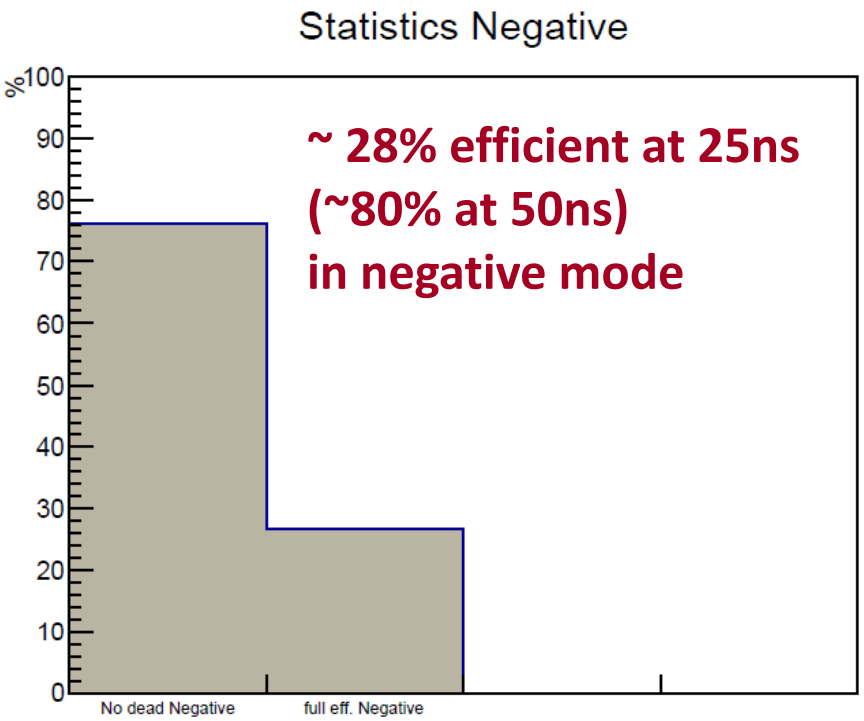
- **Yield Issue** - A large amount of samples exhibit small response and high analog baseline (>200mV, compared to the nominal ~160mV) in the central channels and no response when operating at the minimum peaking time 25ns

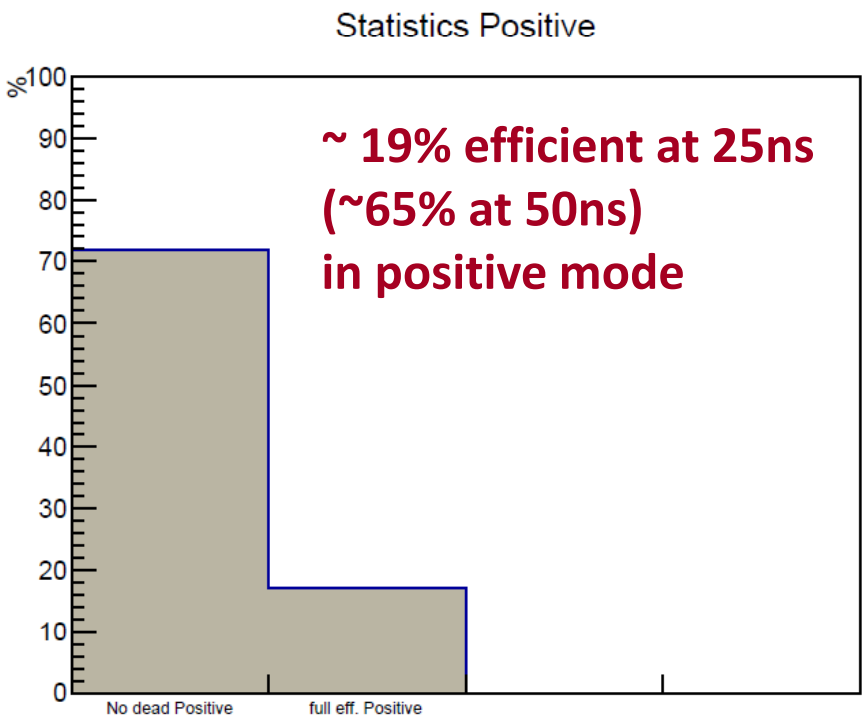
- **Origin** - Limited drive capability in second stage of shaper, combined with ground voltage drop

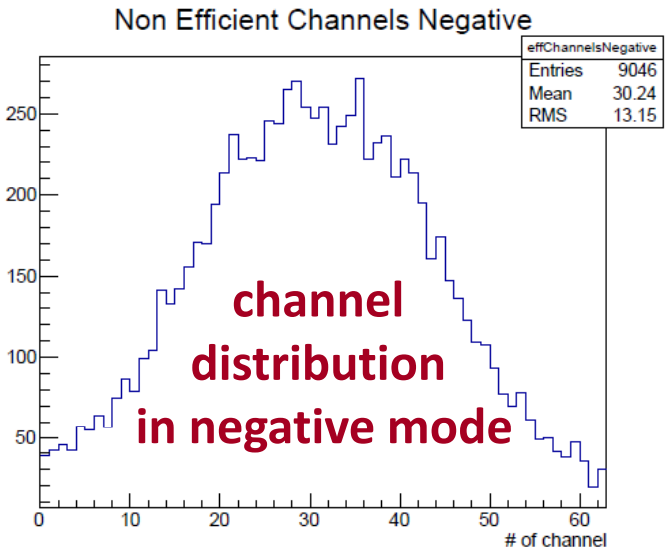
- **Possible workaround** - Operate sTGC at 50ns

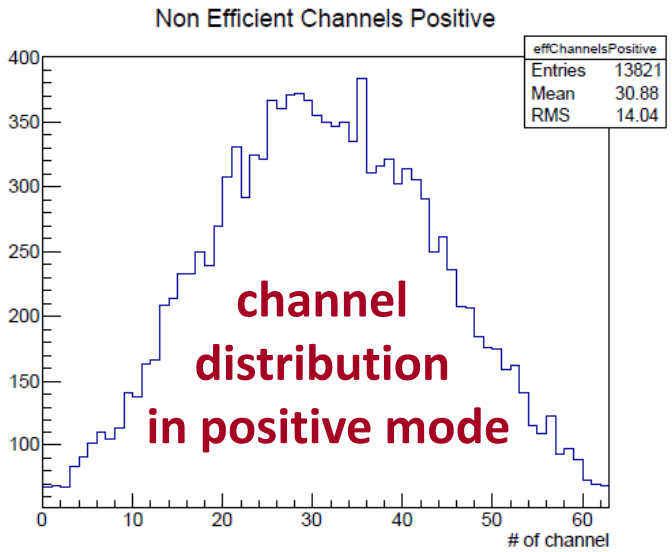
- **Fix** - Increase driver size

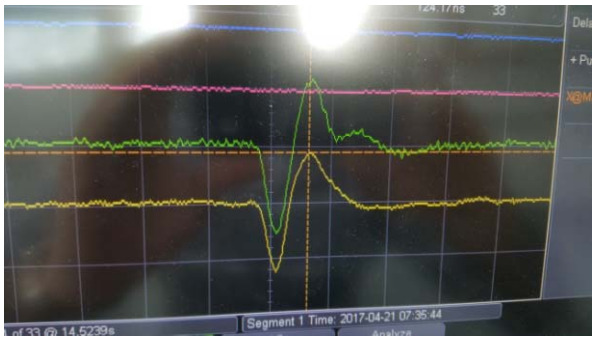
Measured Statistics on High Baseline Issue 2





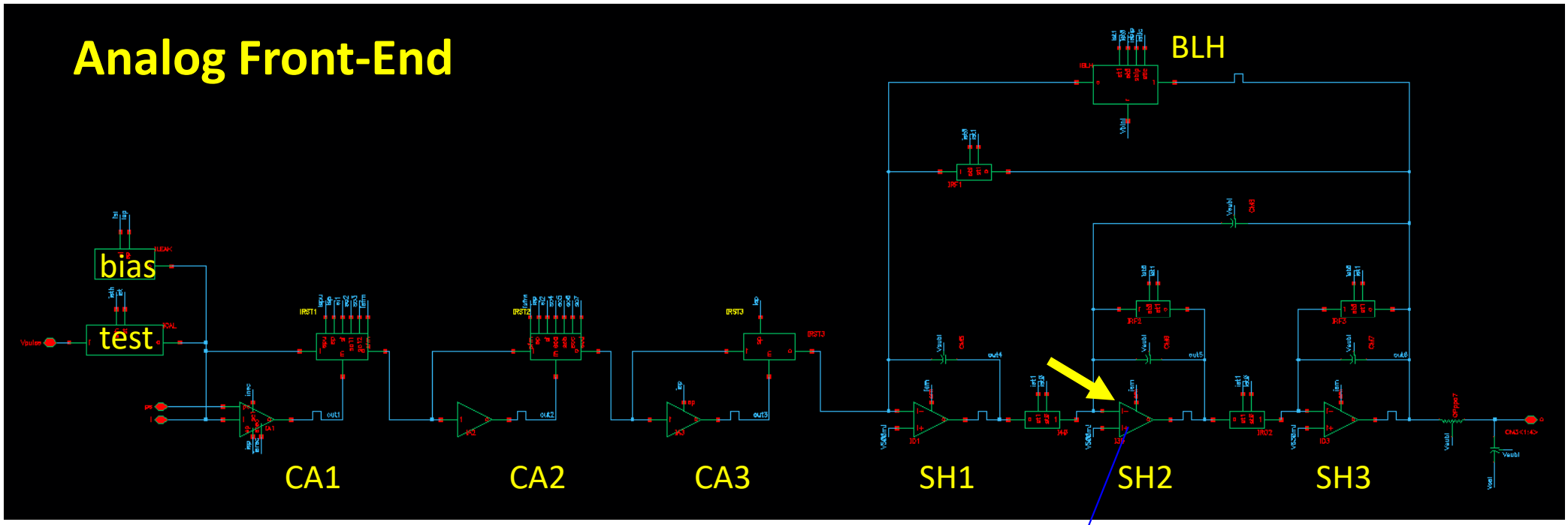


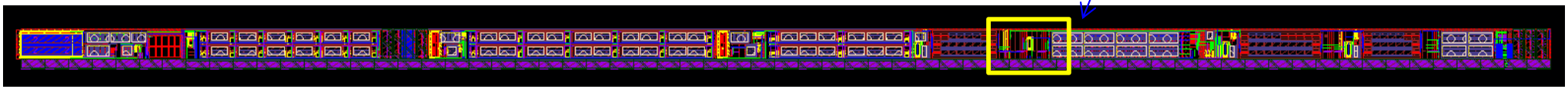




G. Iakovidis

Shaper Amplifier

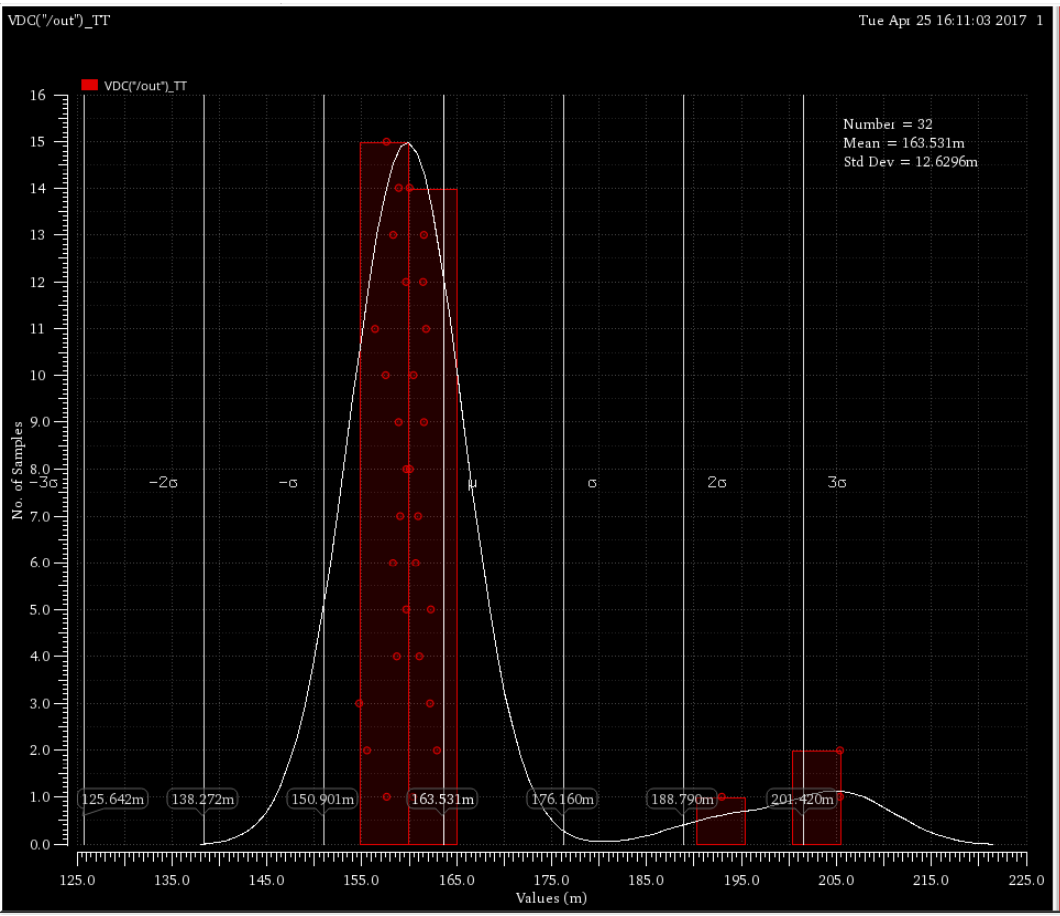


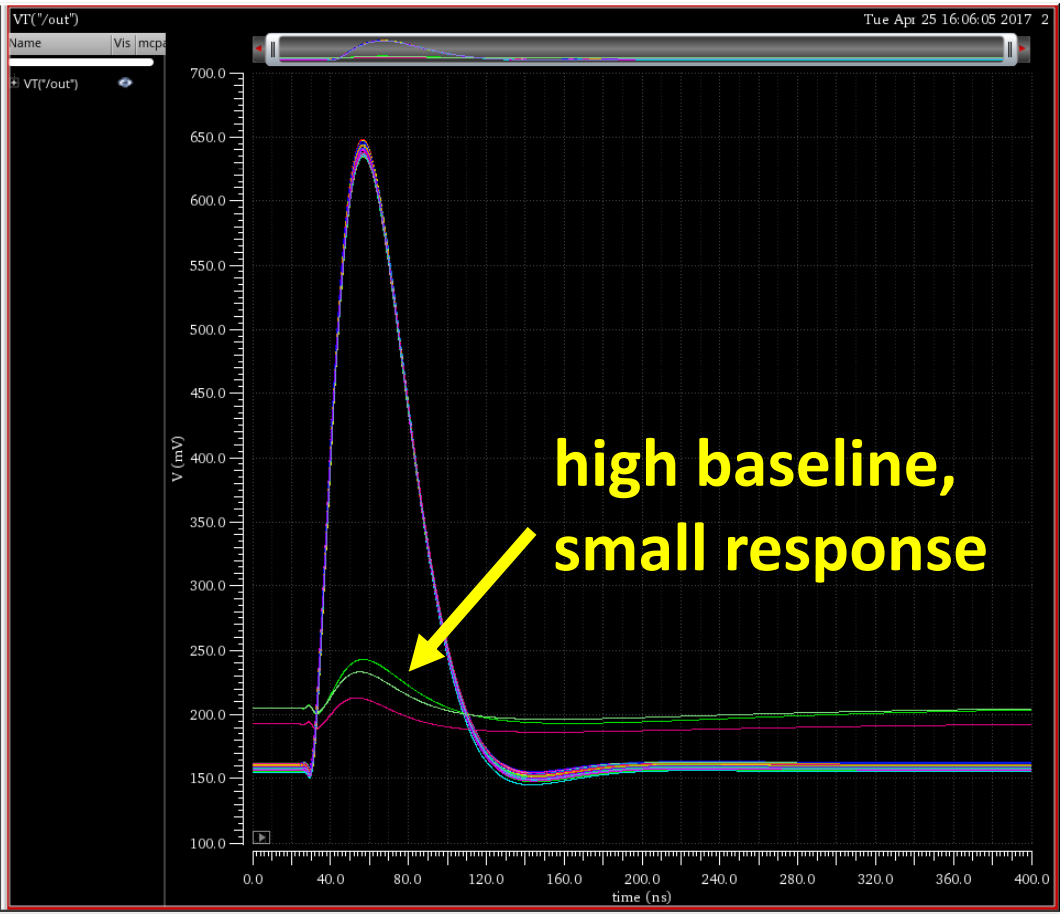


~ 4mm

- **Shaper amplifier is composed of three voltage amplifiers with programmable passive feedback in DDF configuration to realize one real pole and two complex conjugate poles.**
- **Issue is in the output stage of second amplifier, combined with voltage drop of ground at center chip**

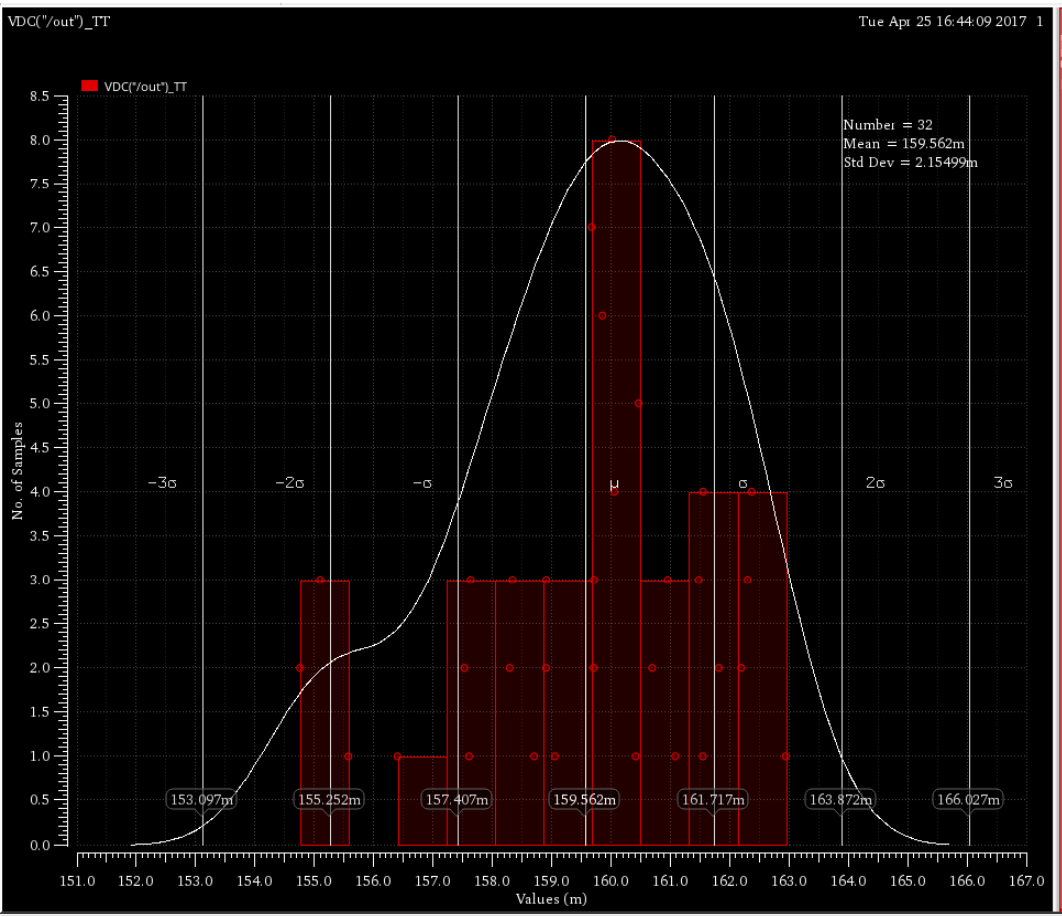
Monte Carlo at 25ns

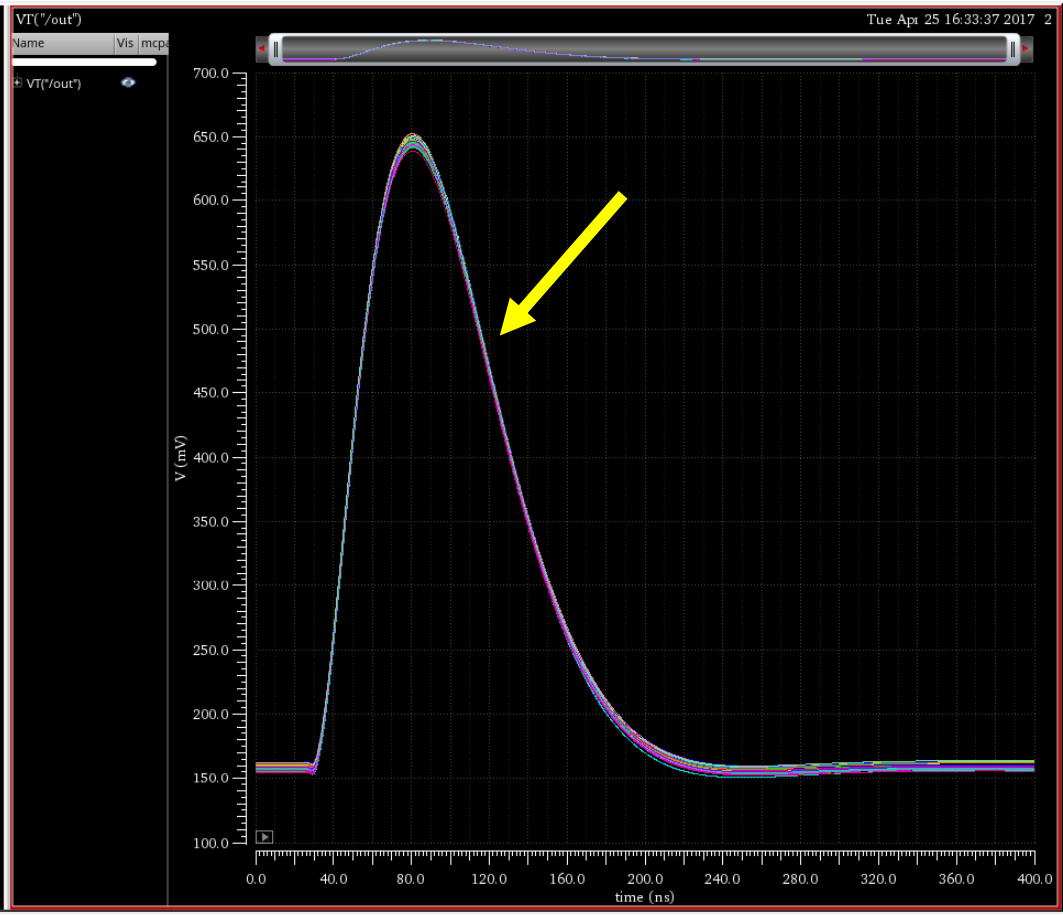




- **Monte Carlo TT simulation with 8mV ground voltage drop at 25ns. Second amplifier output stage doesn't have enough current to bring internal nodes to the correct operating point.**

Monte Carlo at 50ns





- **Monte Carlo TT simulation with 8mV ground voltage drop at 50ns. Larger feedback resistor allow amplifier to bring internal nodes to the correct operating point.**

VMM3 Issues

Issue	Circuit	Notes
Need start-up sequence	channel logic	**workaround**
Handle sTGC charge & rate	analog front-end	**workaround**
Locking in ToT	channel logic	**workaround**
ENA acquisition reset	control logic	**workaround**
Trimming range extension	channel trimmer amplifier	**3/4 of targeted**
High baseline	shaper	**workaround - yield 25ns***
ADC accumulation	ADCs	**improvements - yield MSB***

***new**

Conclusions

- **VMM3 is the first full prototype front-end ASIC for the ATLAS Muon upgrade**
- **Seven issues have been found:**

Issue	Circuit	Notes
Need start-up sequence	channel logic	workaround
Handle sTGC charge & rate	analog front-end	workaround
Locking in ToT	channel logic	workaround
ENA acquisition reset	control logic	workaround
Trimming range extension	channel trimmer amplifier	3/4 of targeted
High baseline	shaper	workaround - yield 25ns*
ADC accumulation	ADCs	improvements - yield MSB*

- **Most issues have workaround or may be acceptable**
- **Two may severely impact the yield**

Design Time Required for Fixes (VMM3a)

Fix		Complexity	Risk	Confidence	Time (hrs)
ADC	linearity	medium	low	moderate	~ 80
	yield	medium	low	moderate	~ 120
Reset		low	low	high	~ 30
SFM		low	low	high	~ 30
Baseline	stlc	very low	very low	high	~ 20
	yield	very low	very low	high	~ 40
Trim DAC		very low	negligible	very high	~ 15
Startup		very low	negligible	very high	~ 15
DRC, LVS					~ 20

If going directly for production, please allow margins for extra checks

Backup Slides

Summary of ADC Accumulation Issue

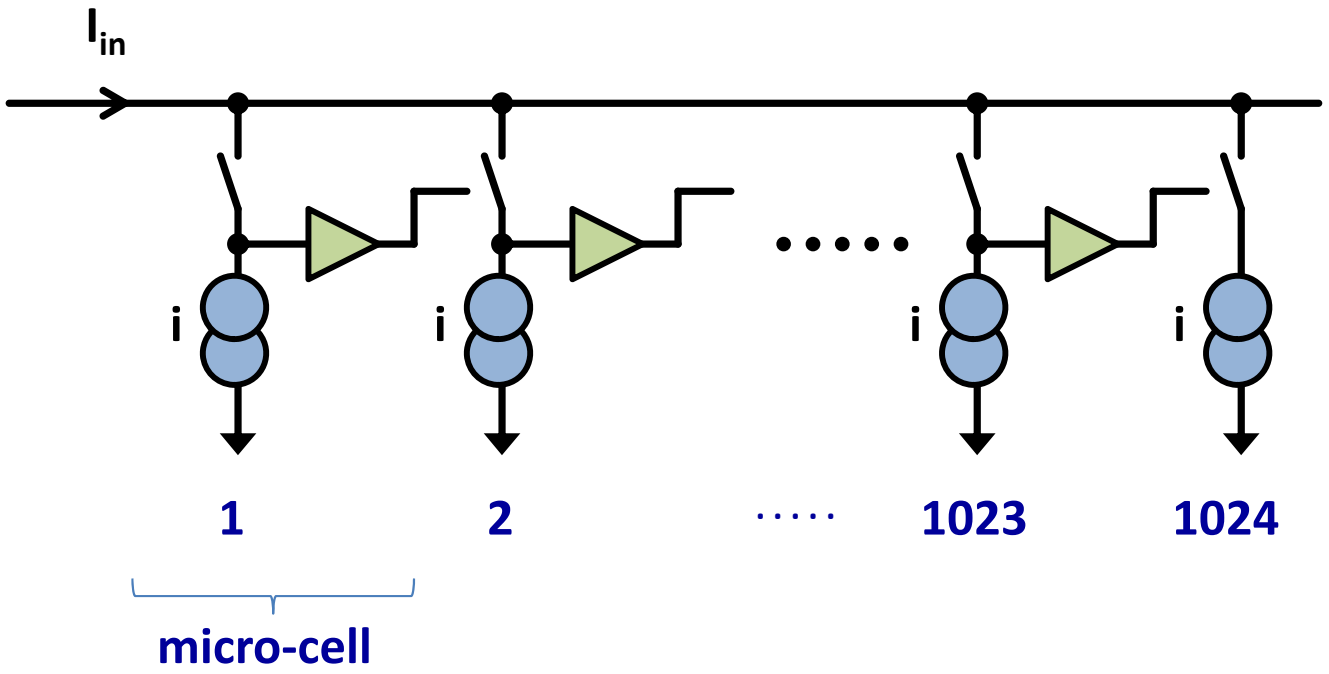
- **Issue - Both 10-bit ADC (charge) and 8-bit ADC (timing) exhibit residual accumulations at the MSB transitions; effective resolution reduced by ~3 bits and ~2 bits respectively**

- **Probable origin - Parasitic current from the MSB phase**

- **Workaround - None**

- **Fix - TBD, simulations queued**

ADC: CMD Architecture



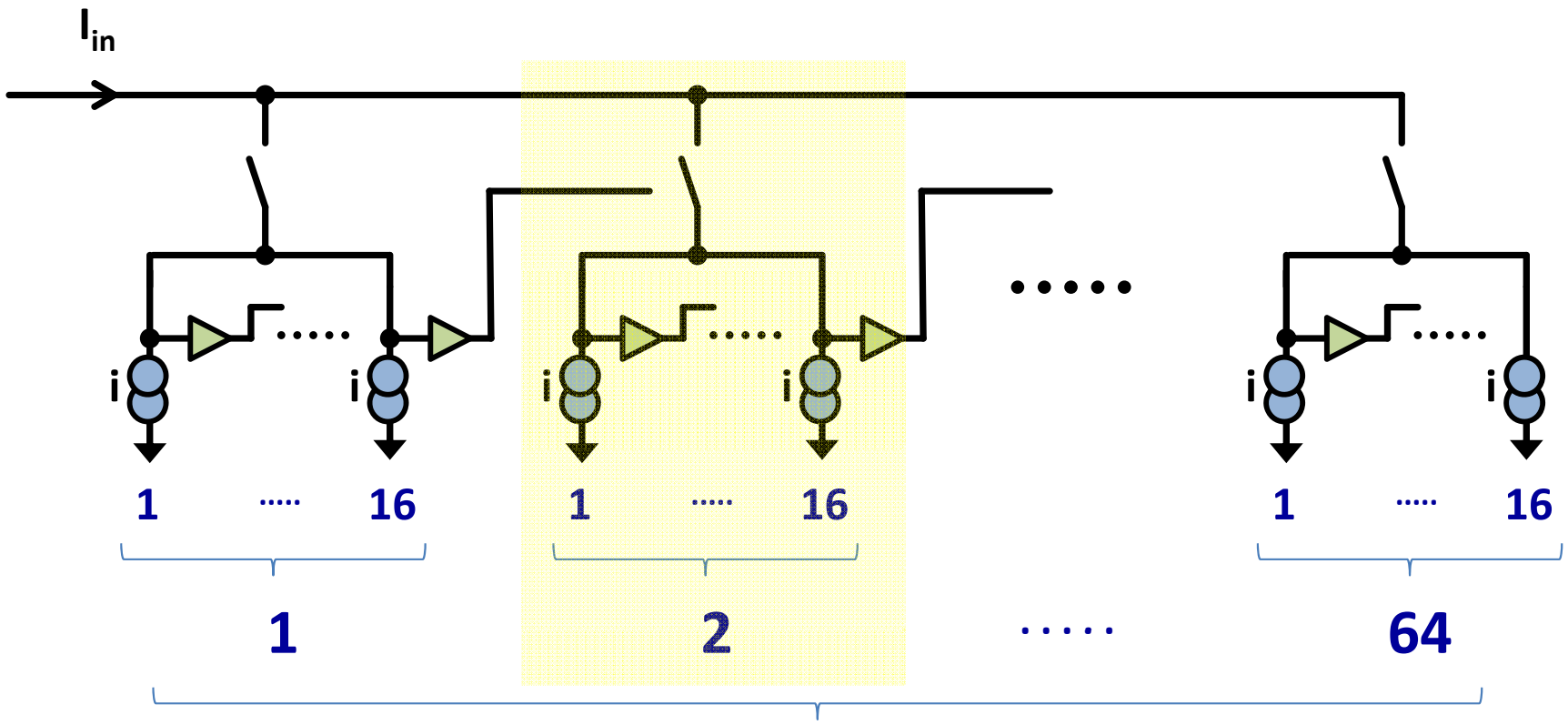
1024 micro-cells

Current-Mode Domino
- no clock required
- early conversion start
- proven in single phase
- **two-phase concept**

Two-Phase ADC Architecture

phase 1: macro-cell selection

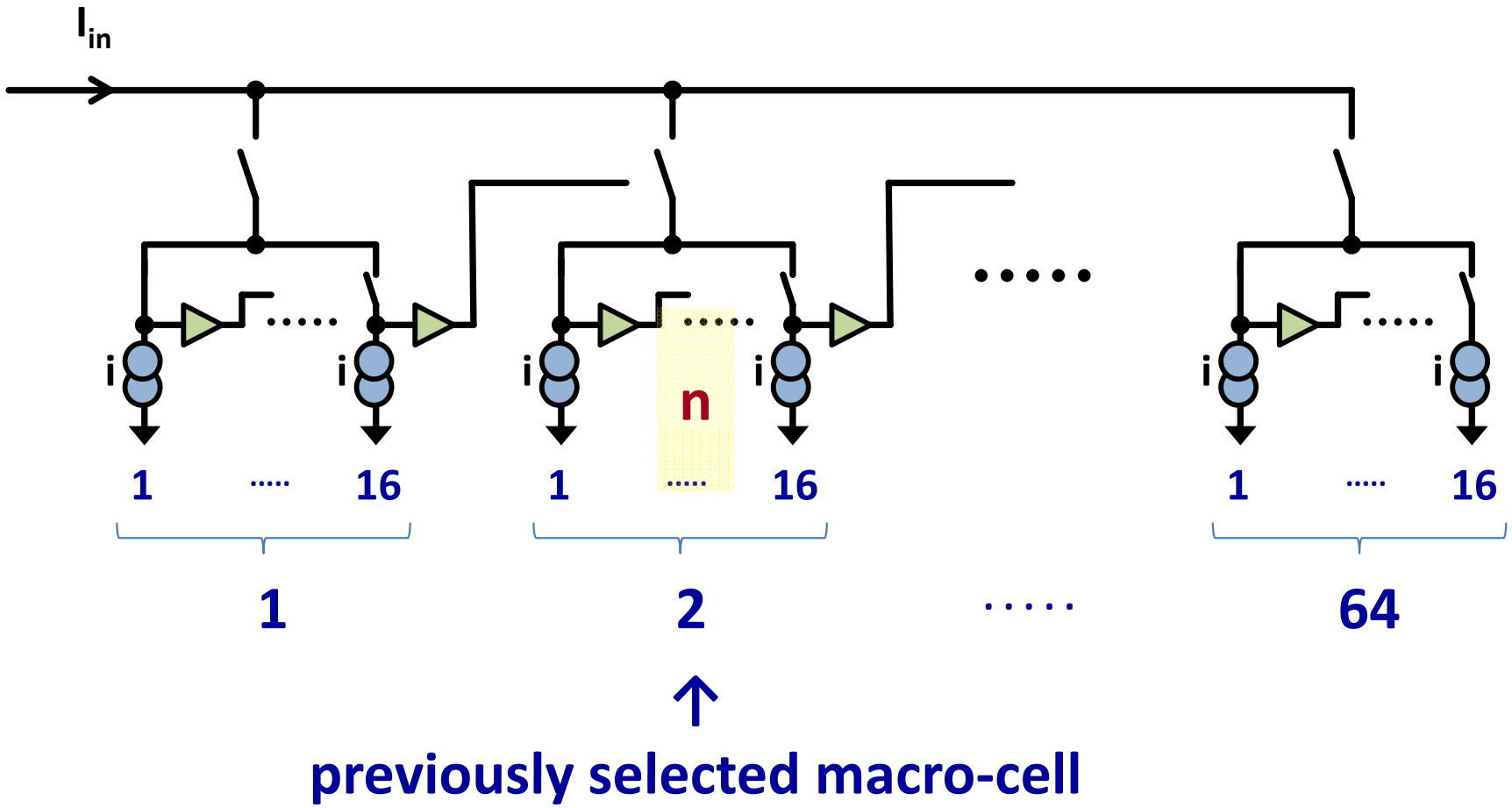
micro-cells are shorted together in groups of 16



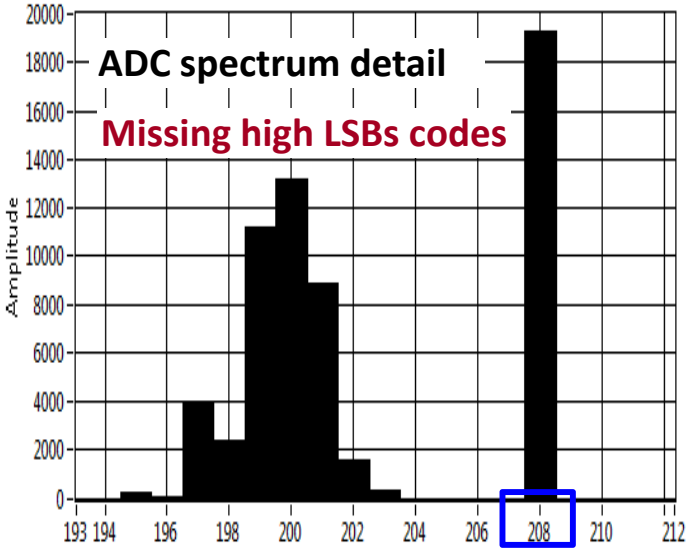
Two-Phase ADC Architecture

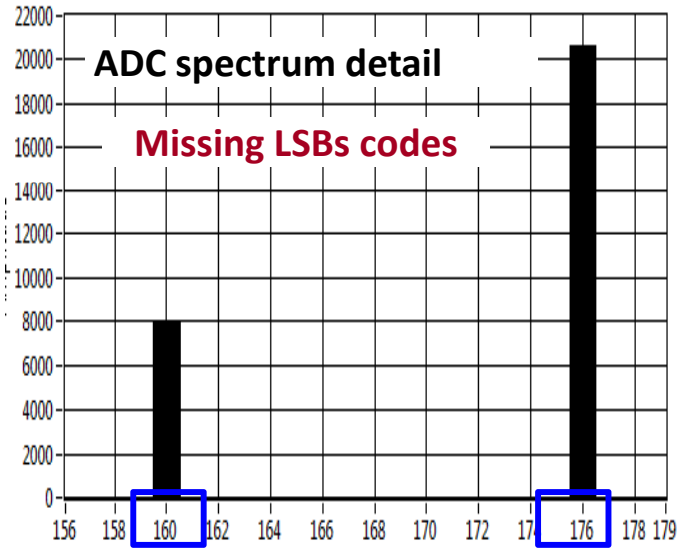
phase 2: micro-cell selection

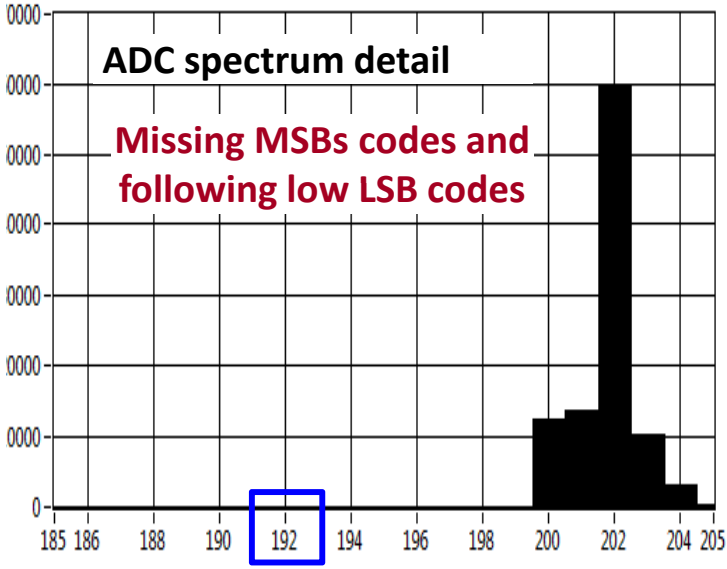
micro-cells are separated individually

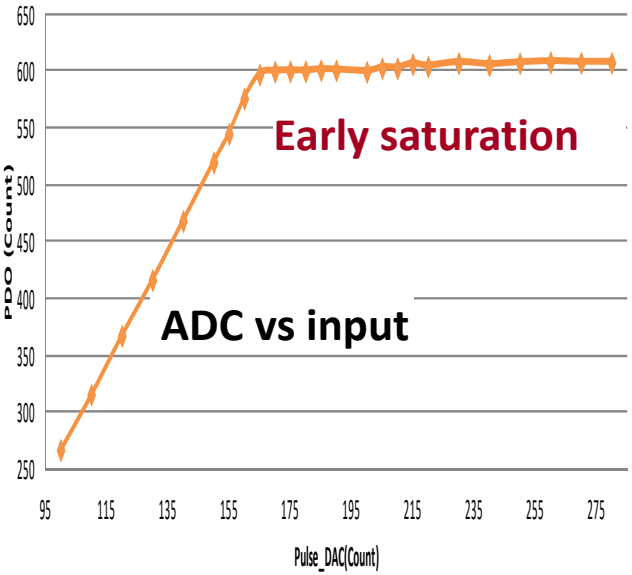


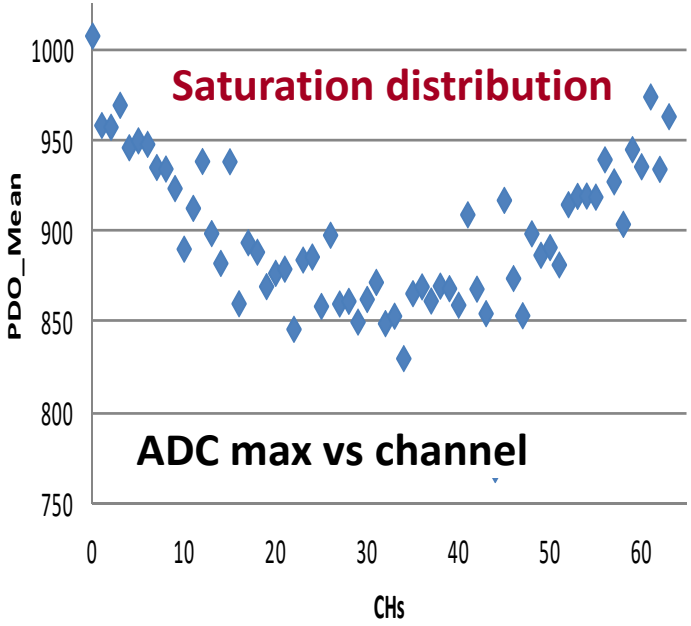
Relevant Issues in VMM2

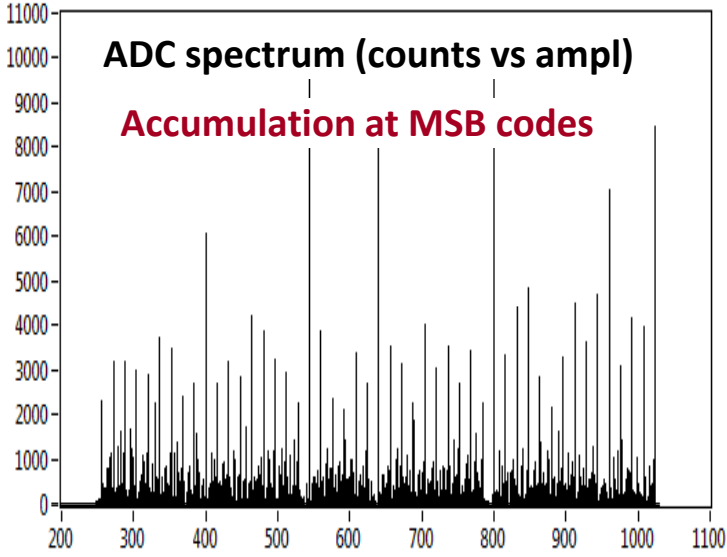






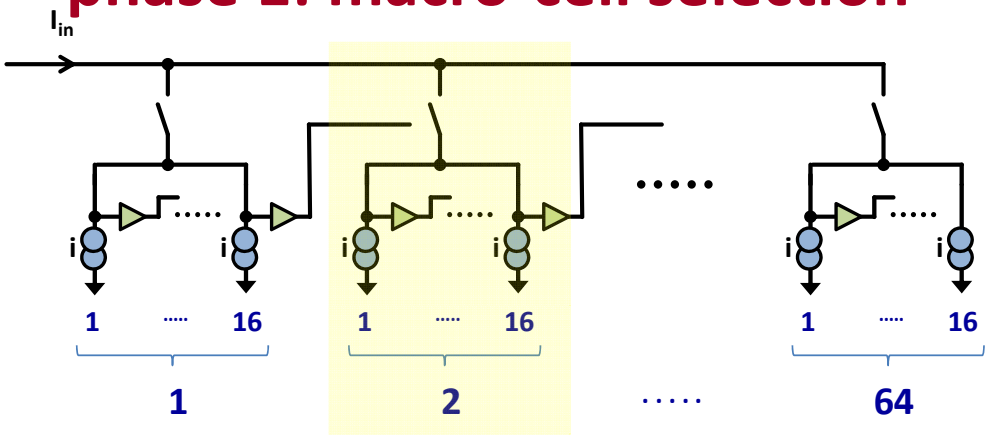




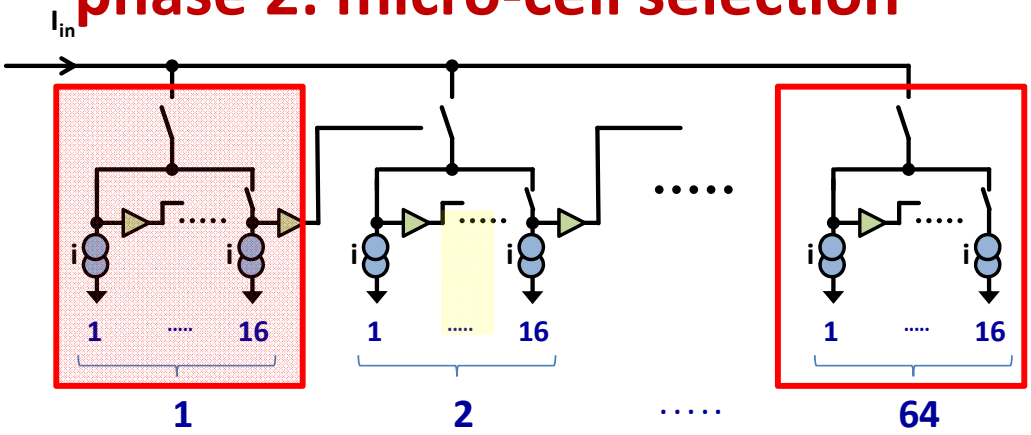


Major Issue in VMM2 Architecture

phase 1: macro-cell selection



phase 2: micro-cell selection

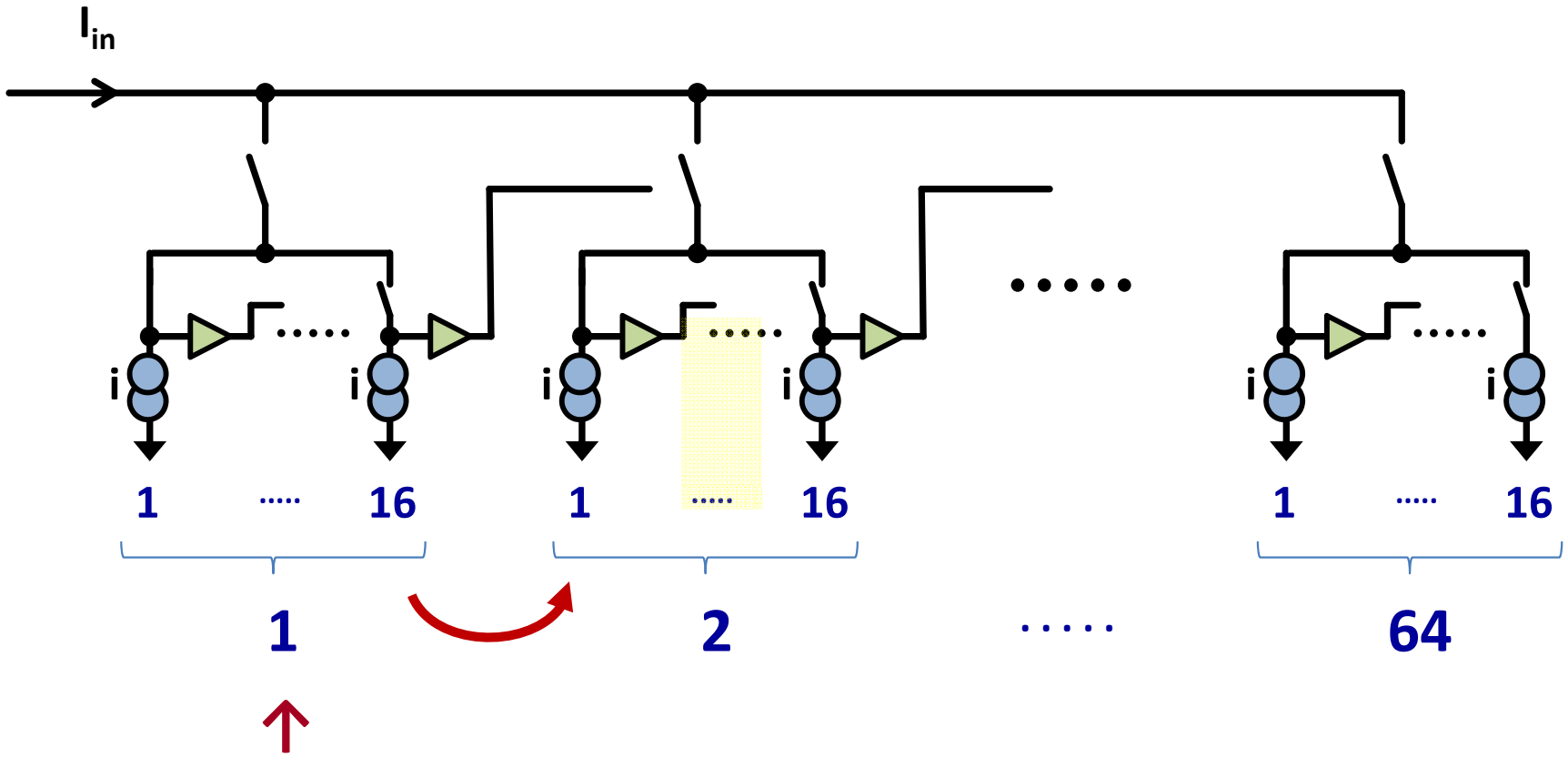


If wrong macro-cell selected (from ringing, pickup, …)

↓

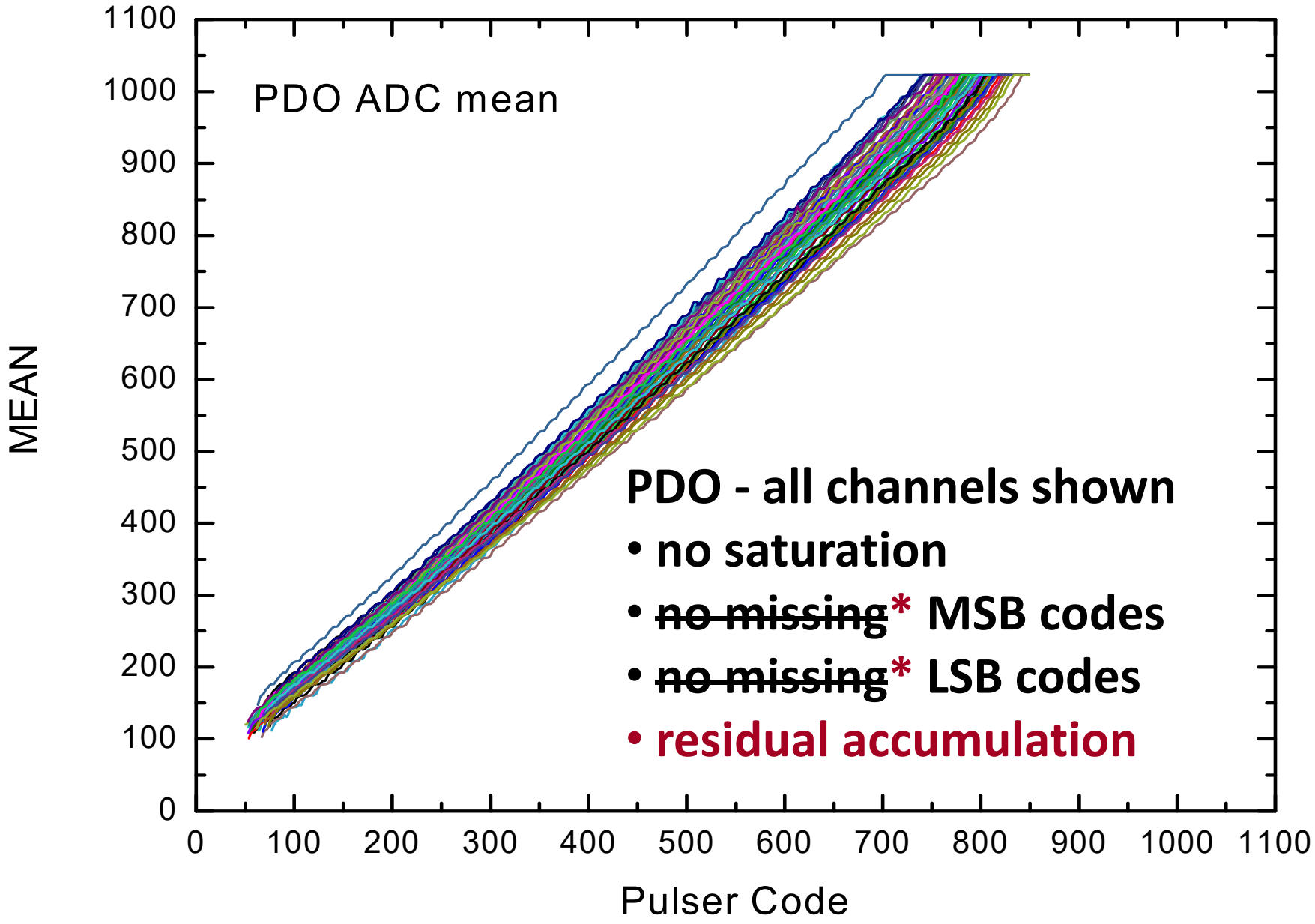
micro-cell selection fails

Pre-Cell Concept in VMM3



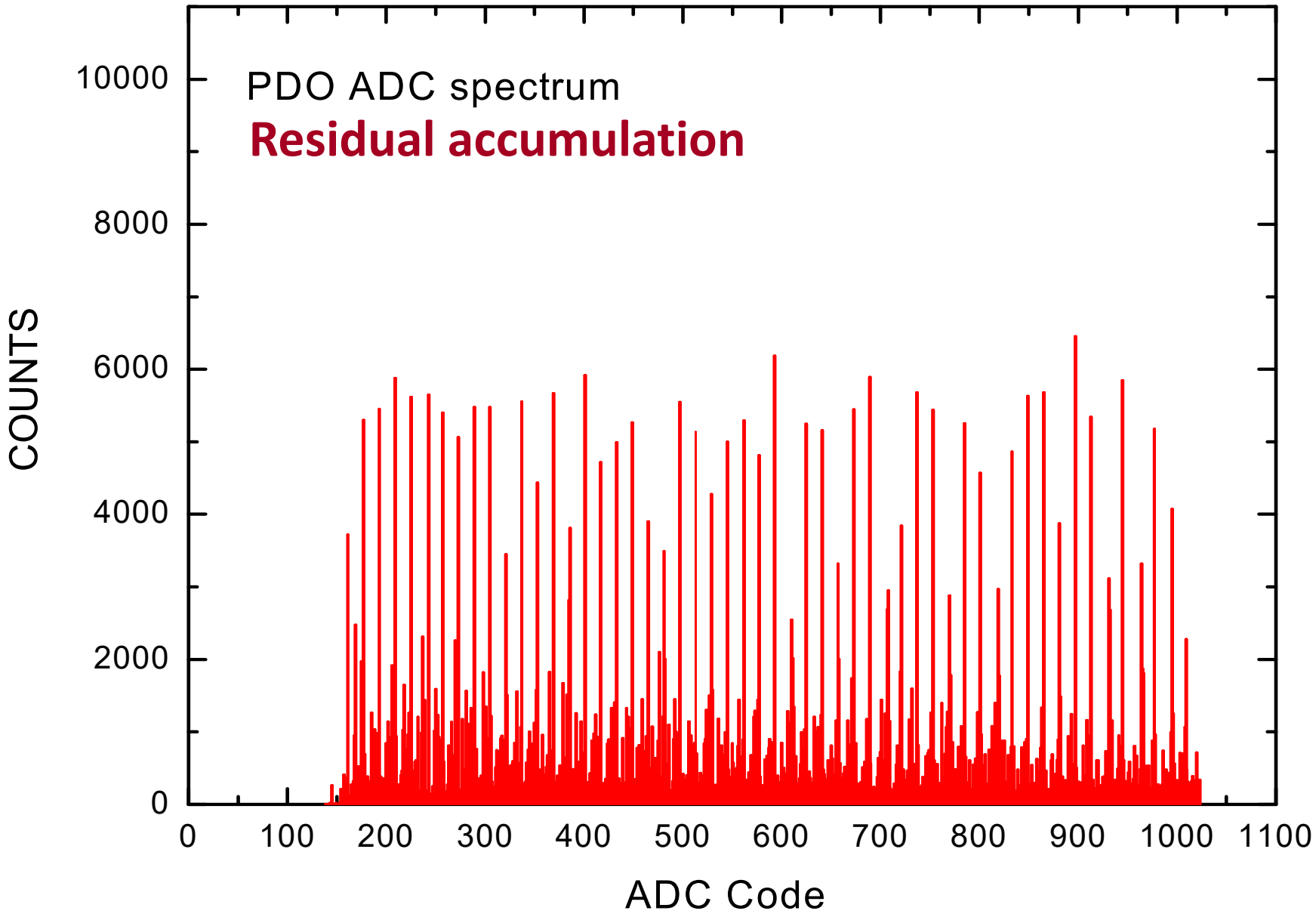
Phase1: same - Phase 2: micro-cell selection starts from preceding macro-cell, able to transition to the next macro-cell

ADC Results in VMM3



*** occasional missing MSB and LSB codes still present**

ADC Results in VMM3



Working with Reduced ADC Resolution

"... which results in ENOB = 7.4 bits" see Vinnie's backup slides

10-bit amplitude ADC with 7-bit effective resolution

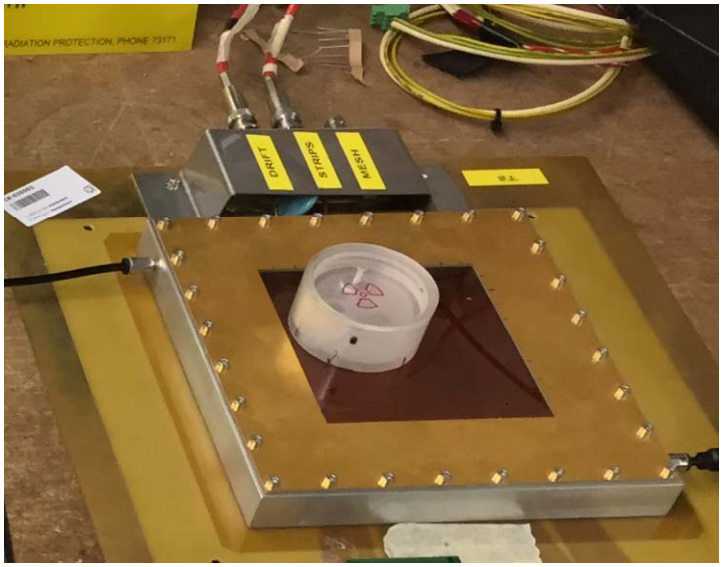
ADC noise at 6mV/fC: $\frac{1}{\frac{6 \cdot 10^{-3}}{2^{10-7} \cdot \sqrt{12}}} = 0.38 \text{ fC rms}$

8-bit timing ADC with 6-bit effective resolution

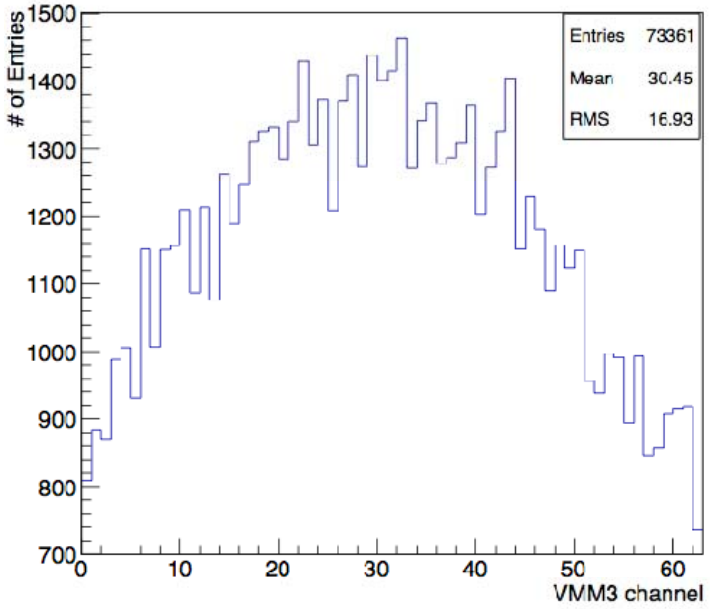
ADC noise at 60ns TAC: $\frac{1}{\frac{6 \cdot 10^{-3}}{2^{10-7} \cdot \sqrt{12}}} = 270 \text{ ps rms}$

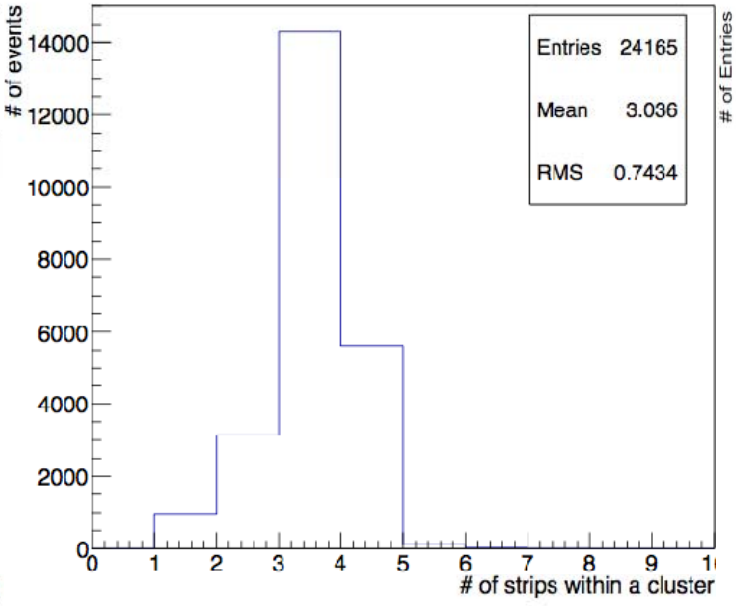
Micromegas measurements with ^{55}FE

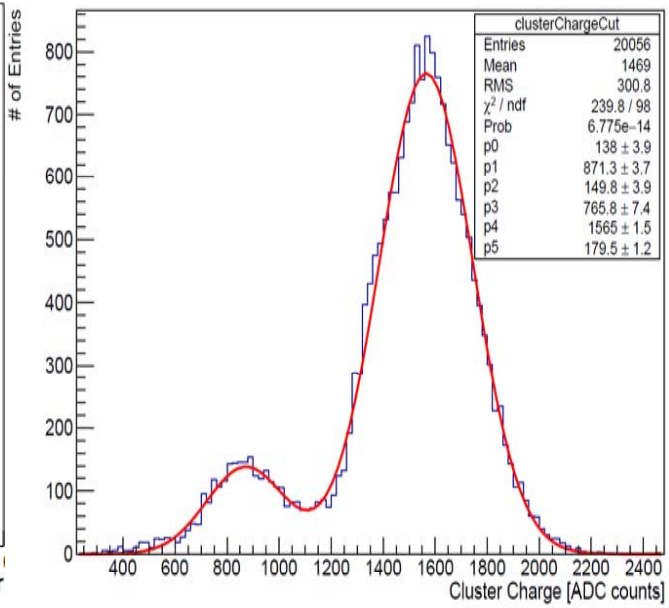
- Micromegas Test chamber with Ar+7%CO_2
- One mini1 (socket based) and packaged VMM3
- Strip voltage at 510V, Drift Voltage at 300V
- VMM3 at 50 ns integration time, 6mV/fC gain
- Random trigger at 1kHz rate
- Hit map complete, no dead channel or inefficient ones
- Simple clustering done, distribution shows a mean value of 3 strips
- Energy resolution at a good level ~27% FWHM, good Ar escape separation and relative height



Cluster Charge (cut on size)

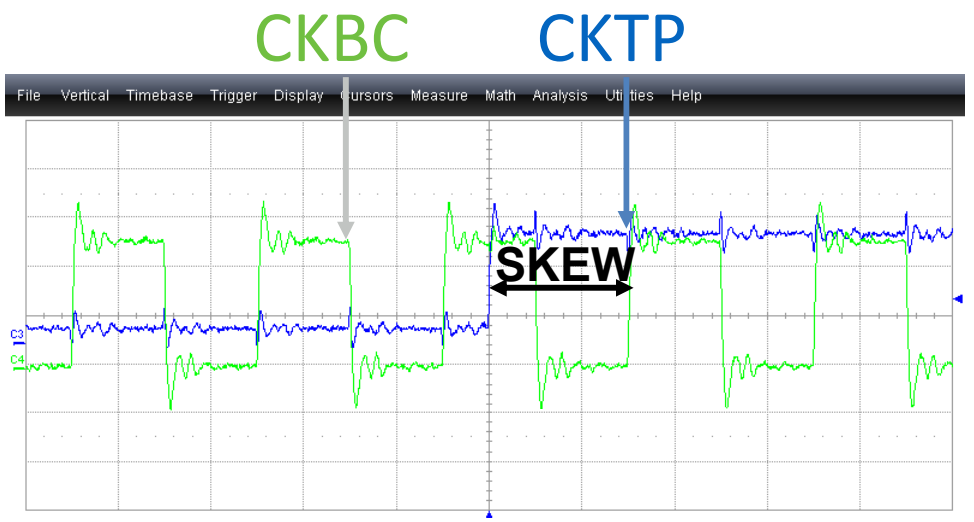


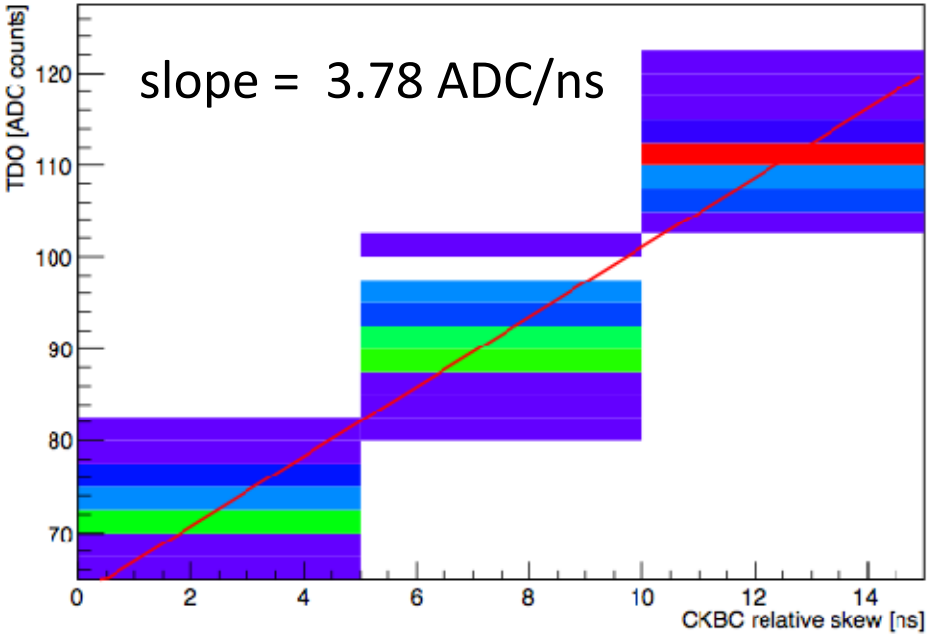


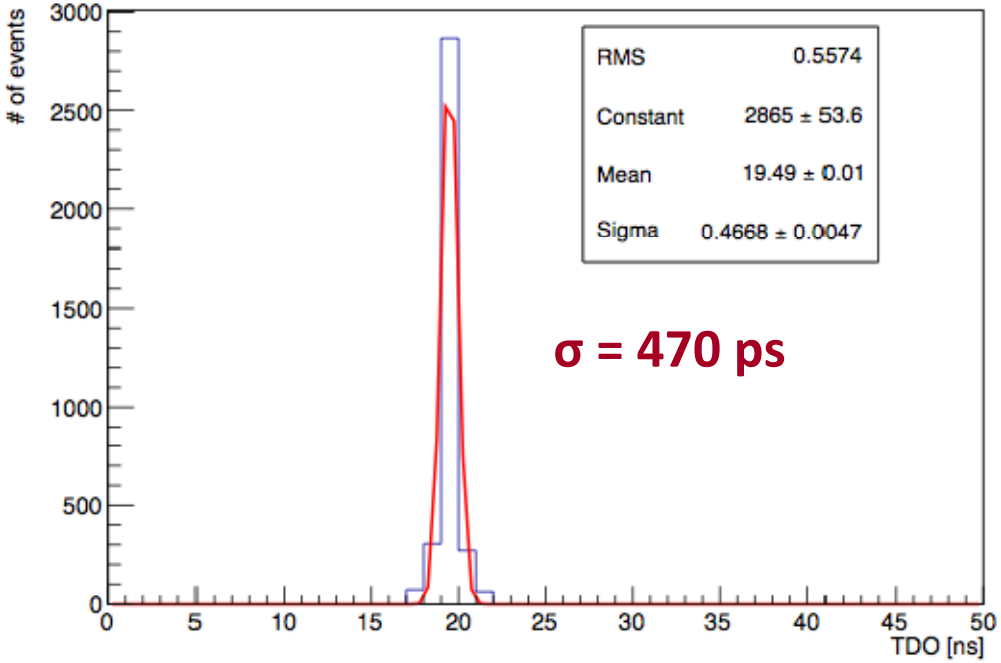


Timing resolution - 25ns integration time

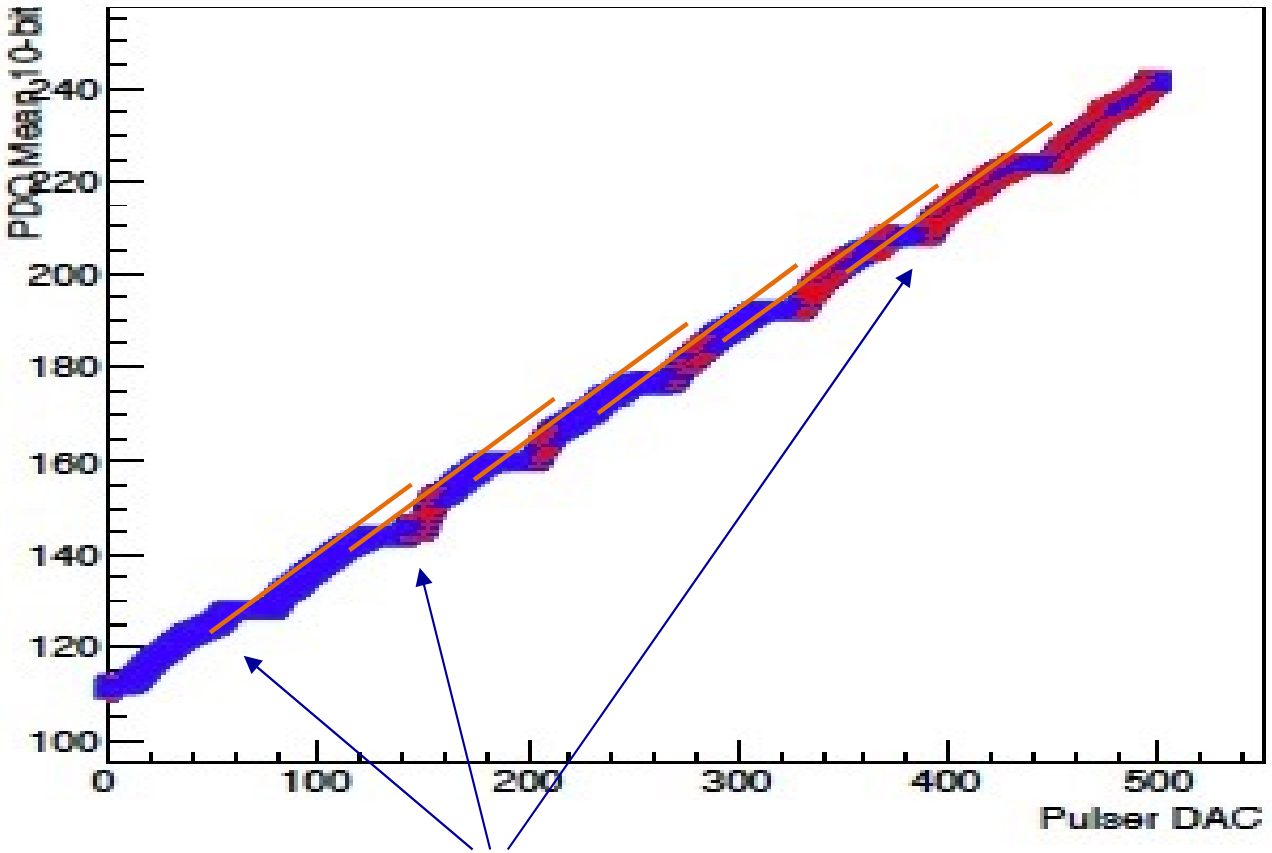
- As known each channel in VMM has a Time to Amplitude Converter which provides timing information (8-bit).
- Calibration involves the TAC calibration for precise timing measurements
- The way it is done on VMM3 is to skew the CKBC with respect to CKTP and measure the TDO.
- Steps of 5 ns used.
- Linear fit on the resulting histogram provides a calibration constant.

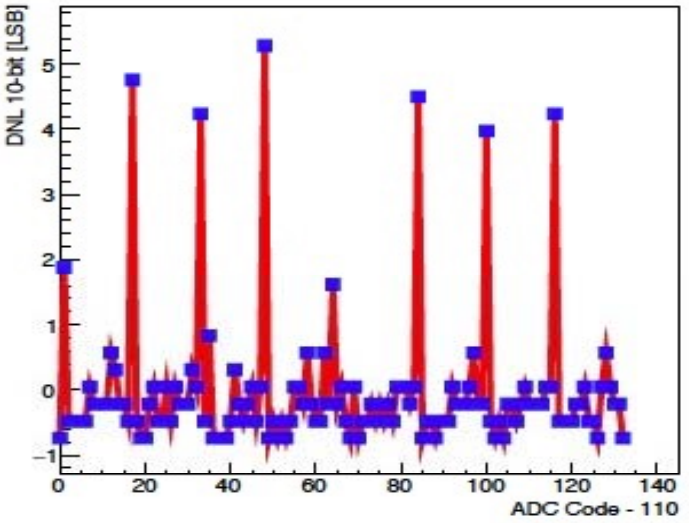




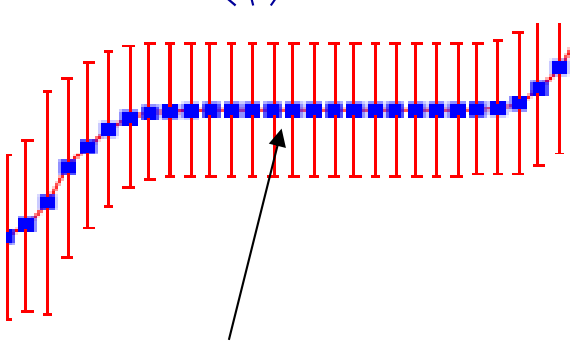


Detail of Residual Issue





V. Polychronakos

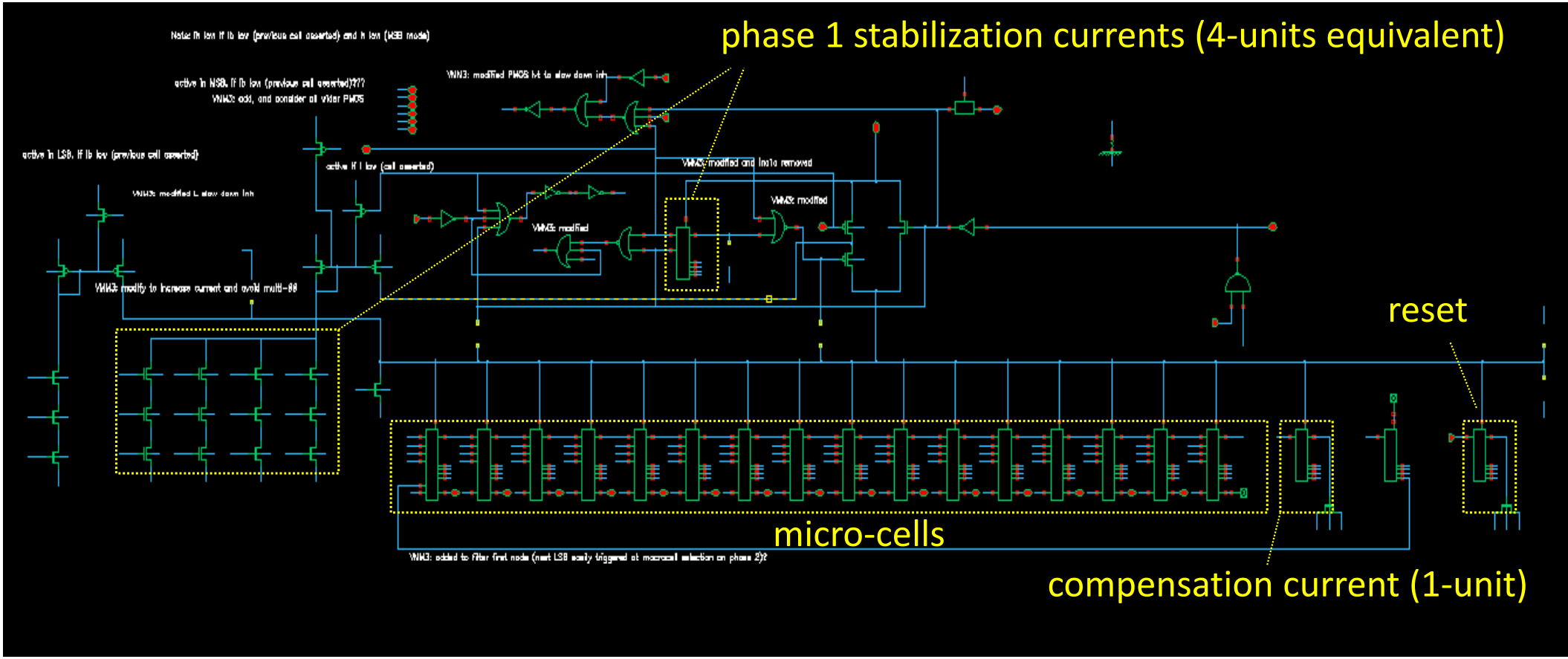


code xxxxxx0000

In phase 2: added parasitic current of ~4 micro-cells → bin ~5 times larger → larger xxxxxx0000 code

Probable Origin of Residual Issue

Macro-Cell Schematic



One of the phase 1 stabilization currents remains enabled during phase 2, resulting in the larger code xxxxxx0000 - to be simulated

Summary of High Baseline Issue

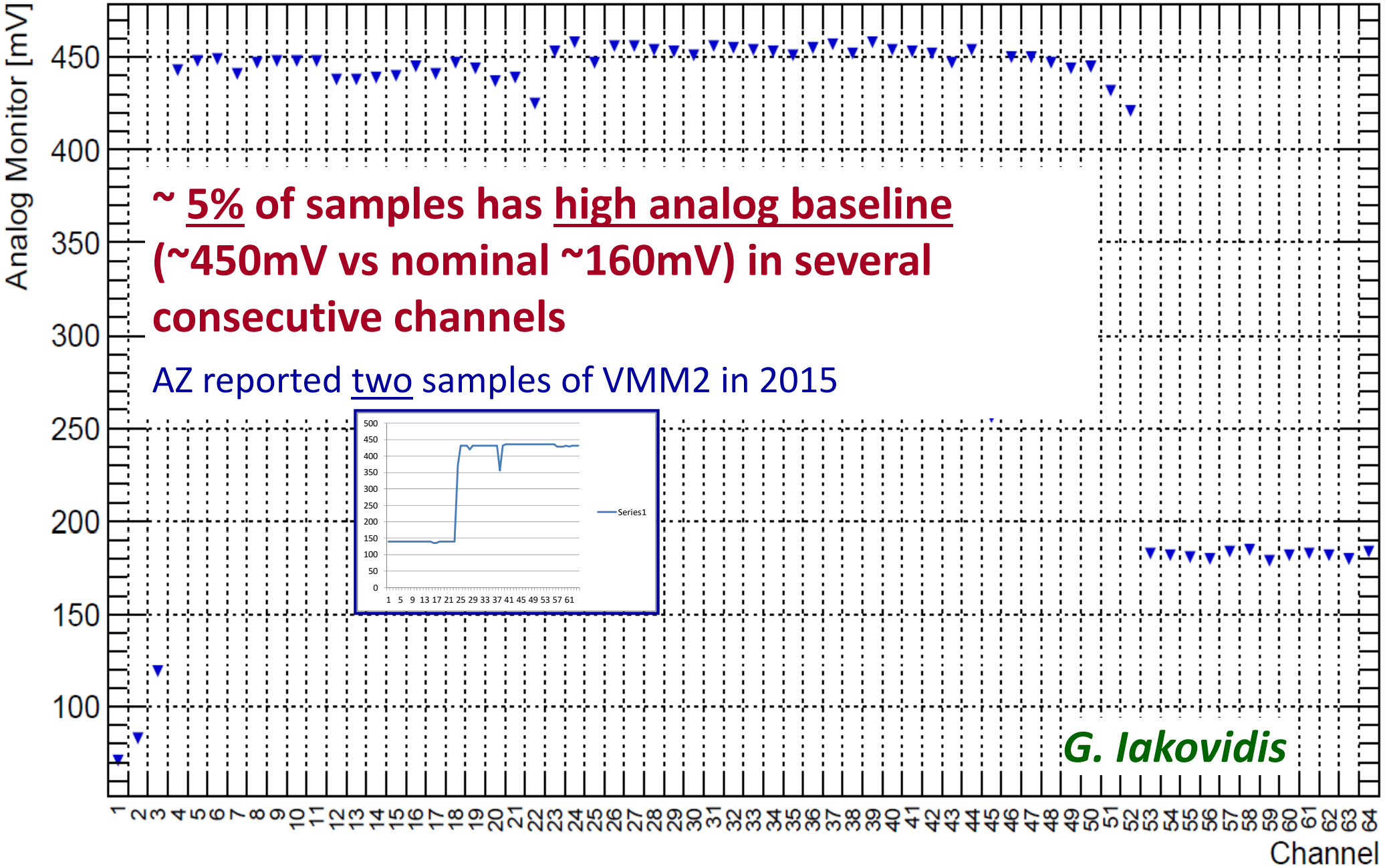
- **Issue** - About 5% of tested samples exhibit a high analog baseline (>400mV, compared to the nominal ~160mV) in several consecutive channels

- **Origin** - Disengagement of low-pass filter in stabilizer, simulations in progress

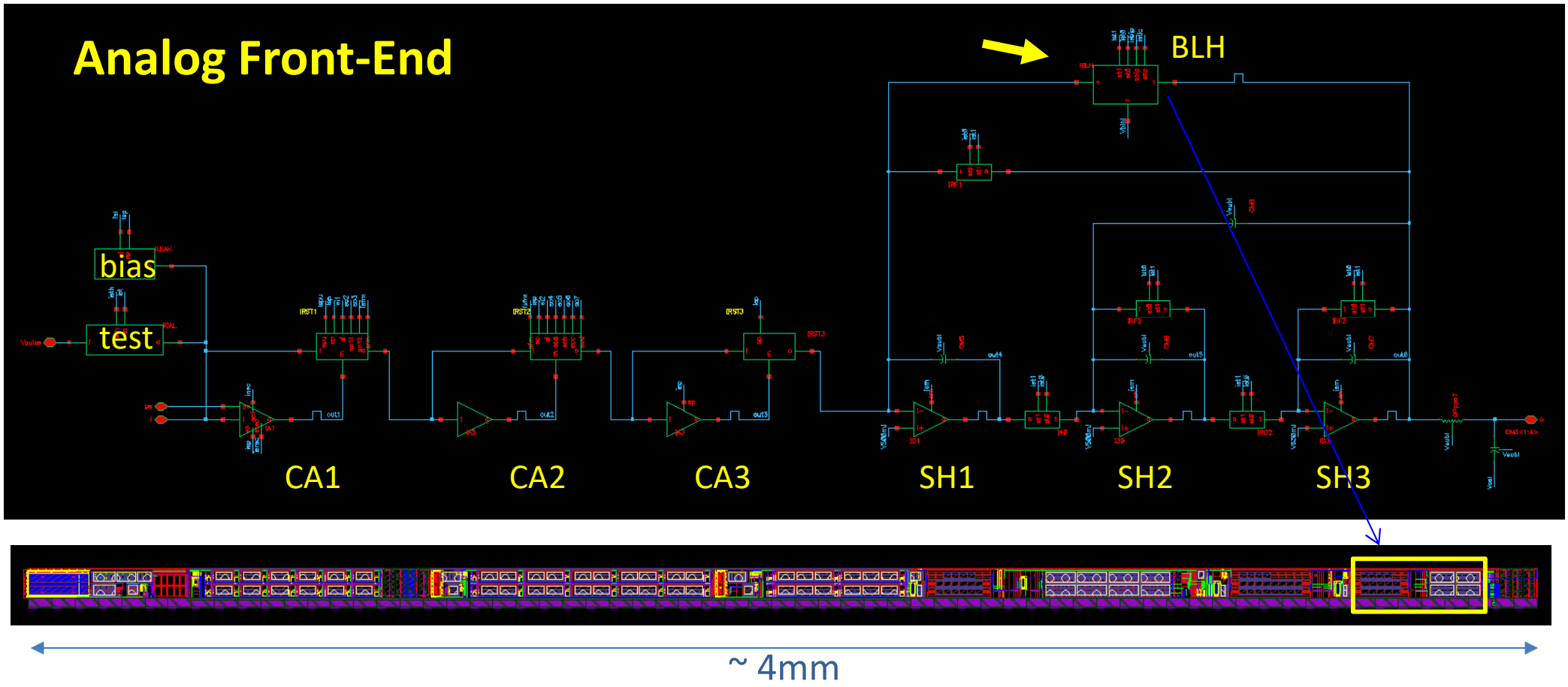
- **Workaround** - The baseline is correct when tail cancellation modes are enabled (STLC or SBIP)

- **Fix** - TBD, simulations queued

Measured High Baseline



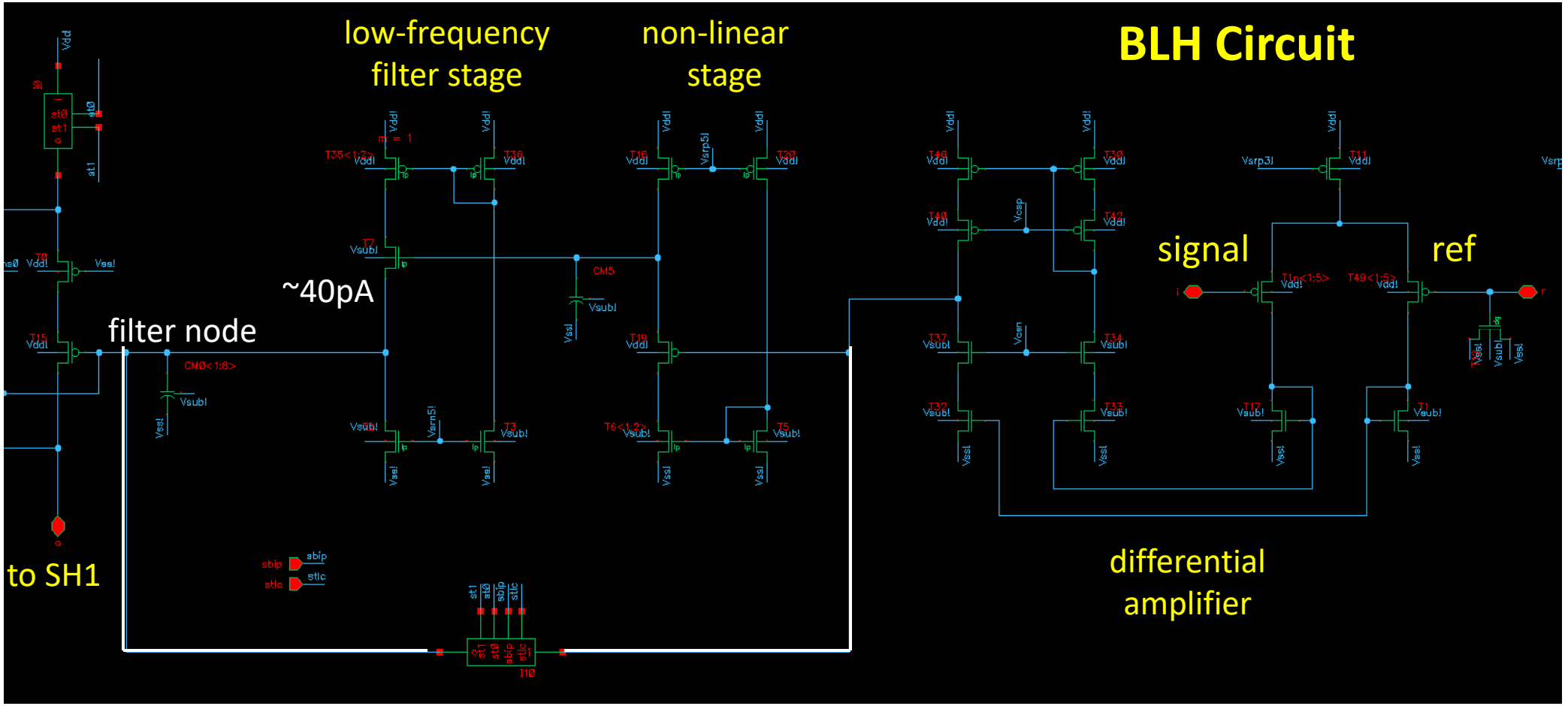
Baseline Stabilizer



~ 4mm

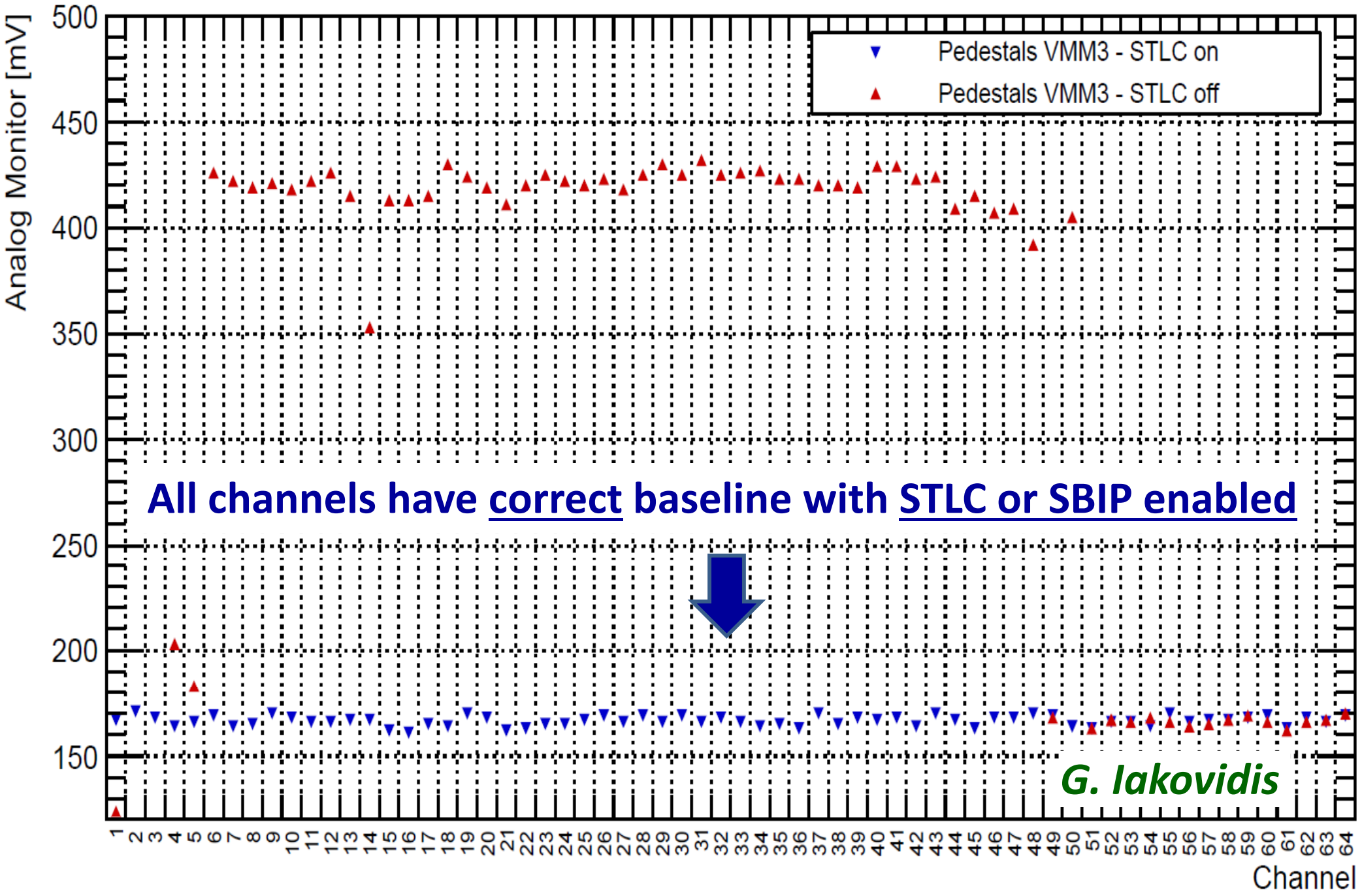
- **Feedback around shaper (BLH) provides stable output baseline by using a precision 160mV reference.**
- **Composed of a differential amplifier, a non-linear stage, and a very-low-frequency filter which operates with very low current**

Bypass for Tail Suppression



- **~450mV baseline → filter node shifted to 1.2V supply, no more control from BLH.**
- **VMM3 implements programmable bypass for mild and strong tail cancellation (bits STLC and SBIP)**

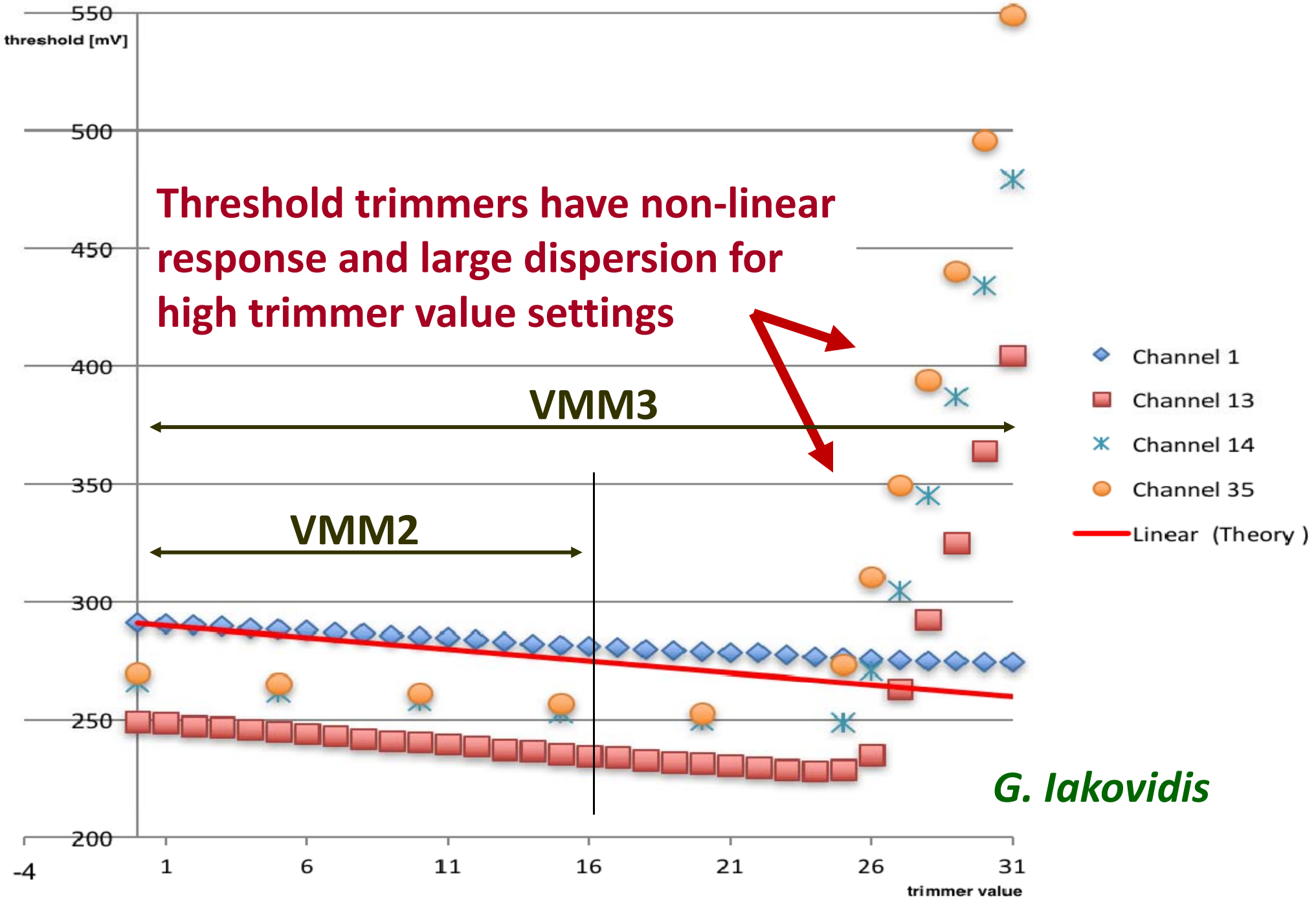
Measured Baseline with STLC or SBIP



Summary of Threshold Trimming Issue

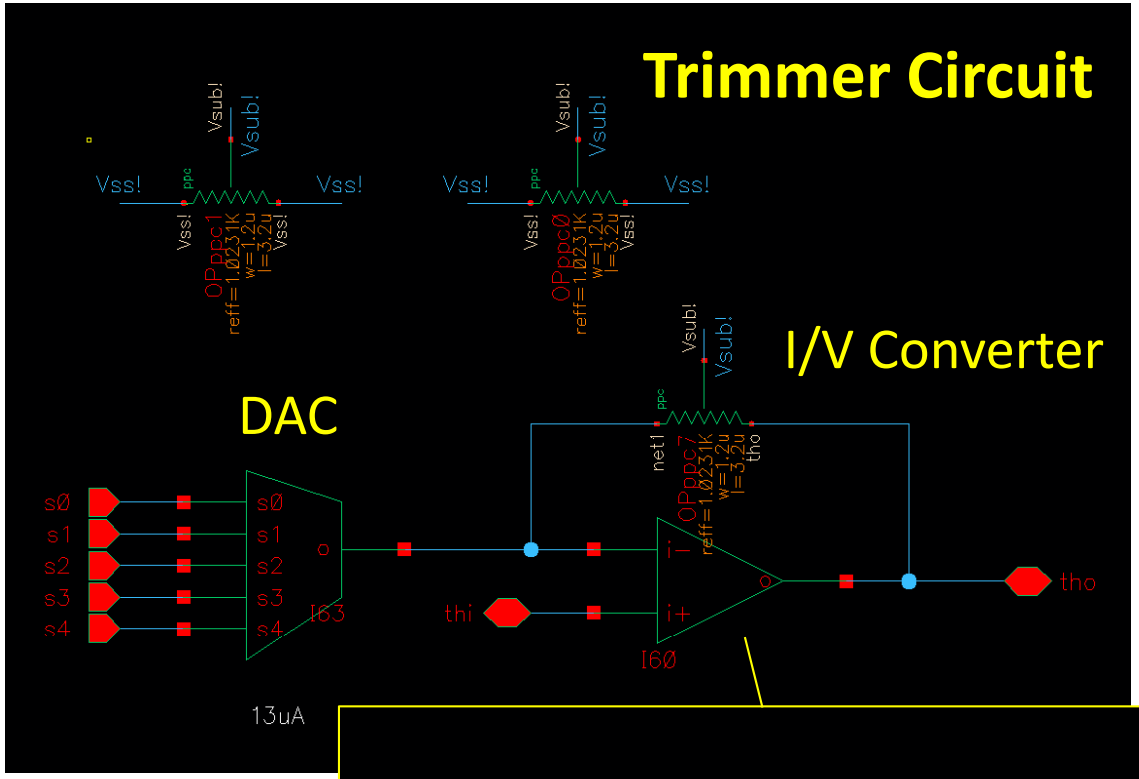
- **Issue - Trimming voltage exhibits saturation and return back; effective range is ~x1.5 instead of planned x2**
- **Origin - Limited drive capability of trimming amplifier**
- **Workaround - None**
- **Fix - Increase driver size**

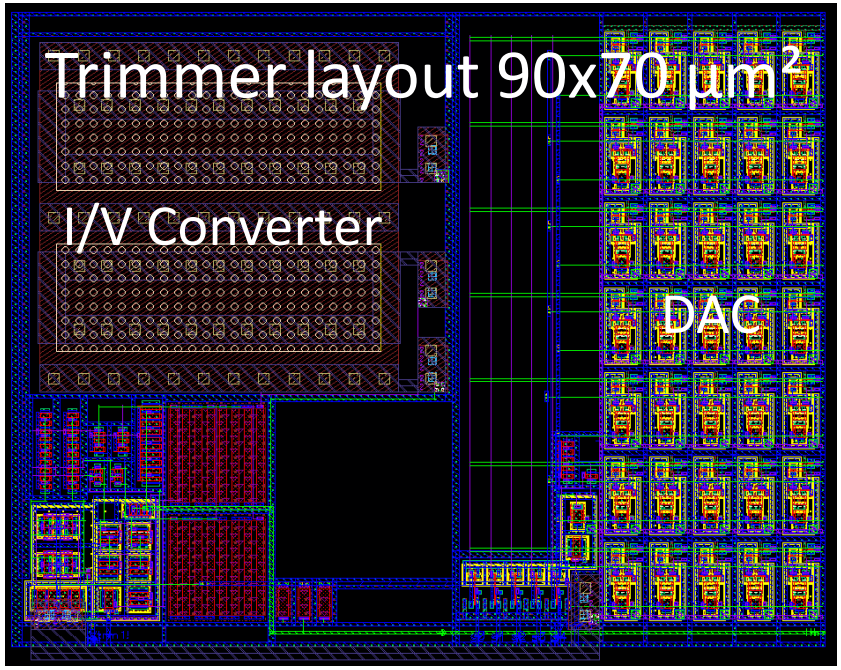
Threshold Trimming Issue

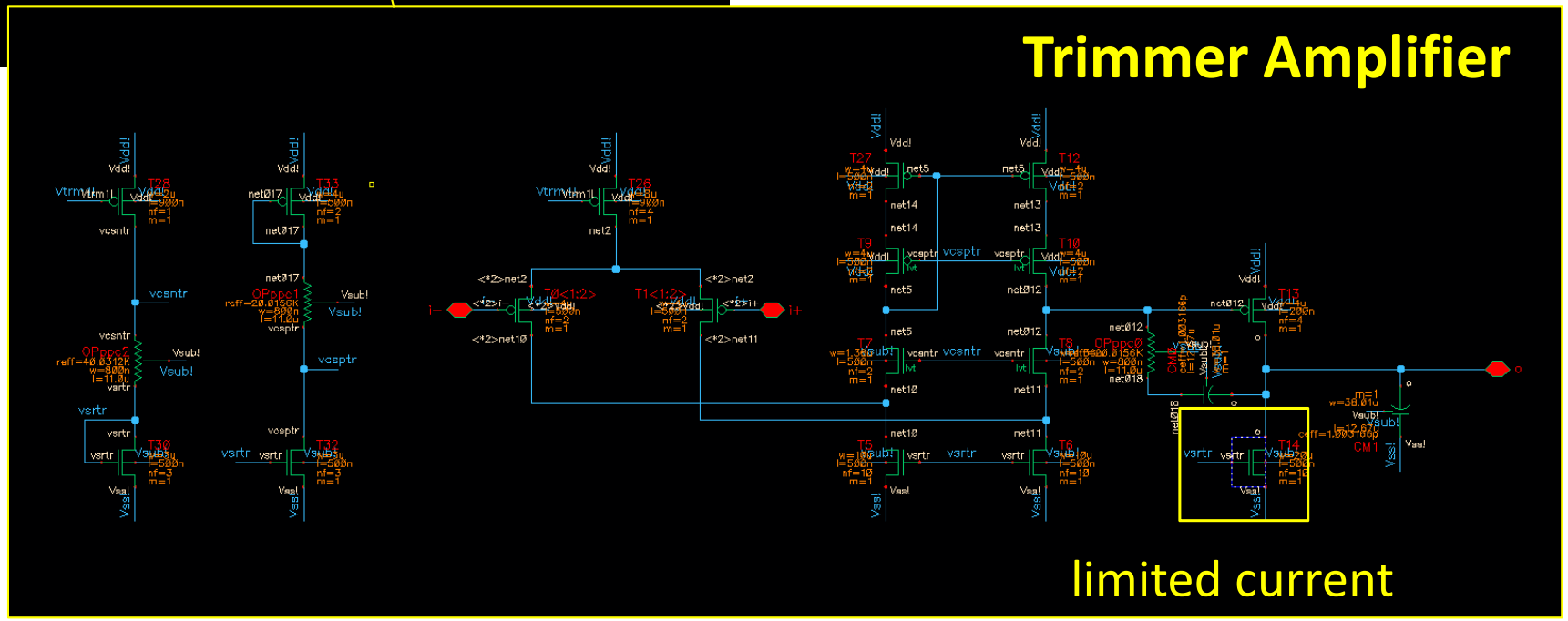


G. Iakovidis

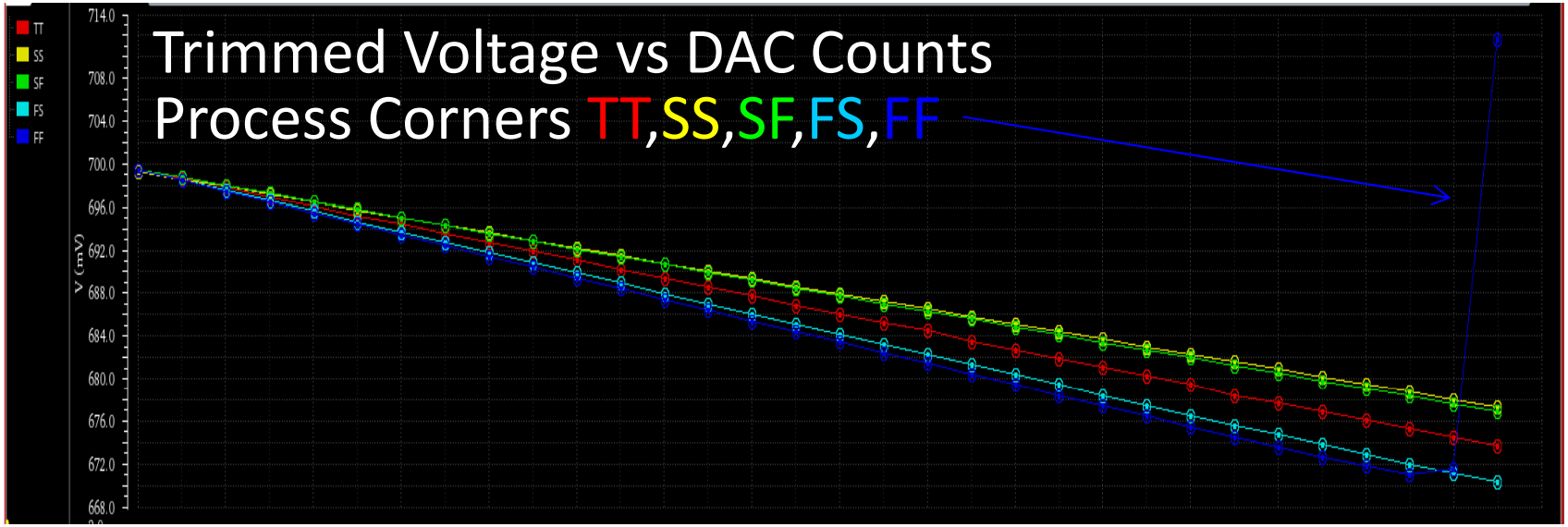
Threshold Trimming Issue Circuit Detail

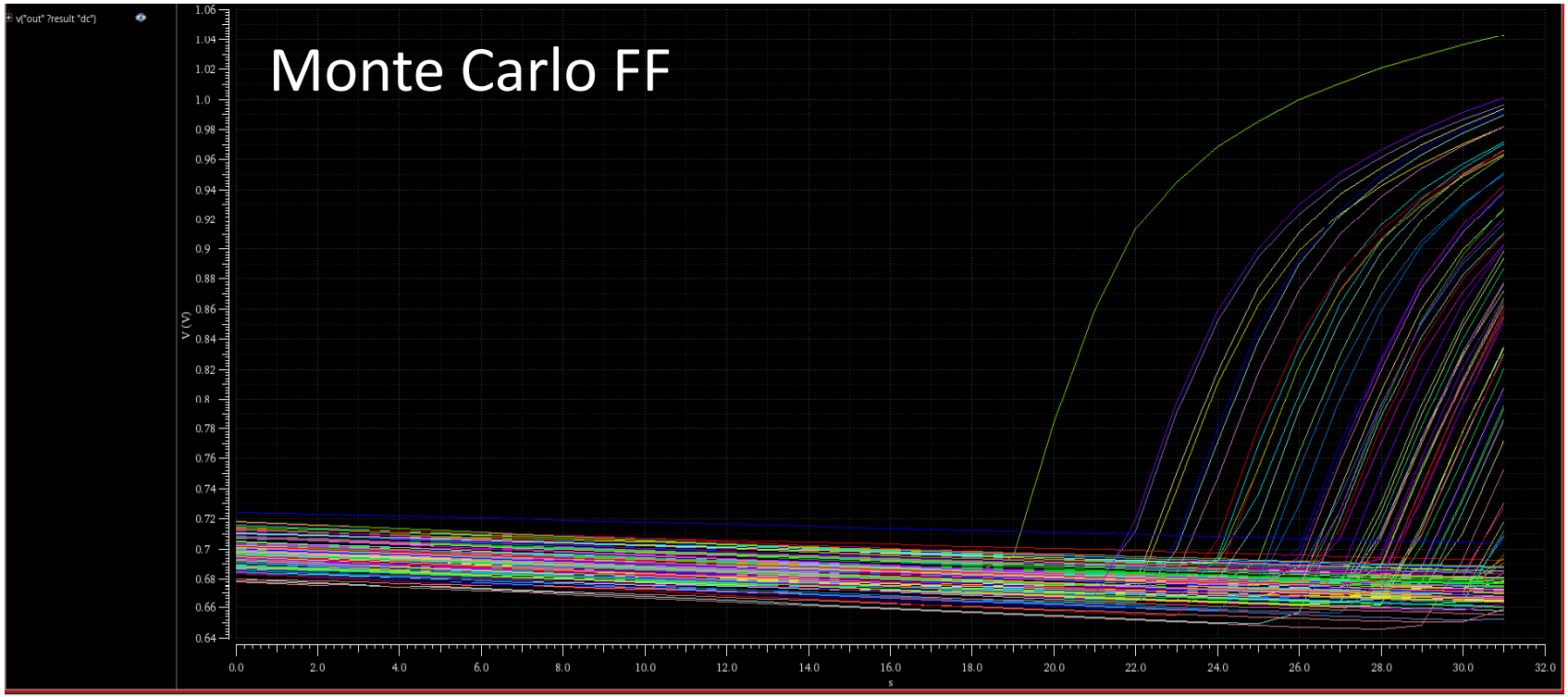




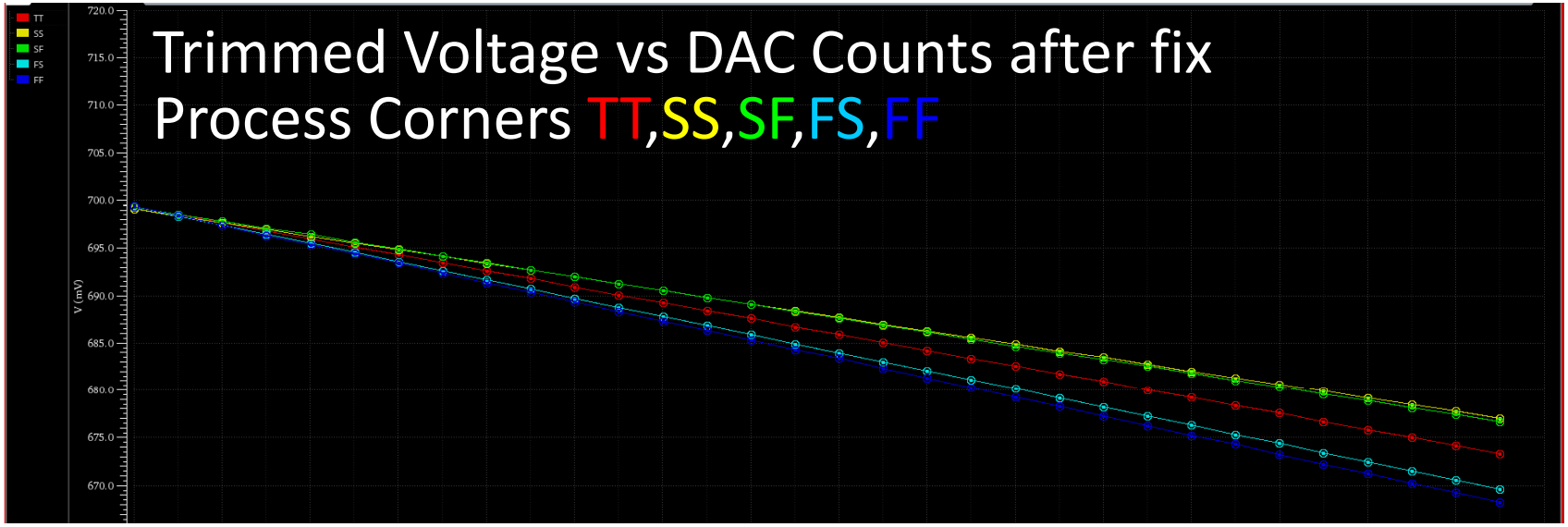


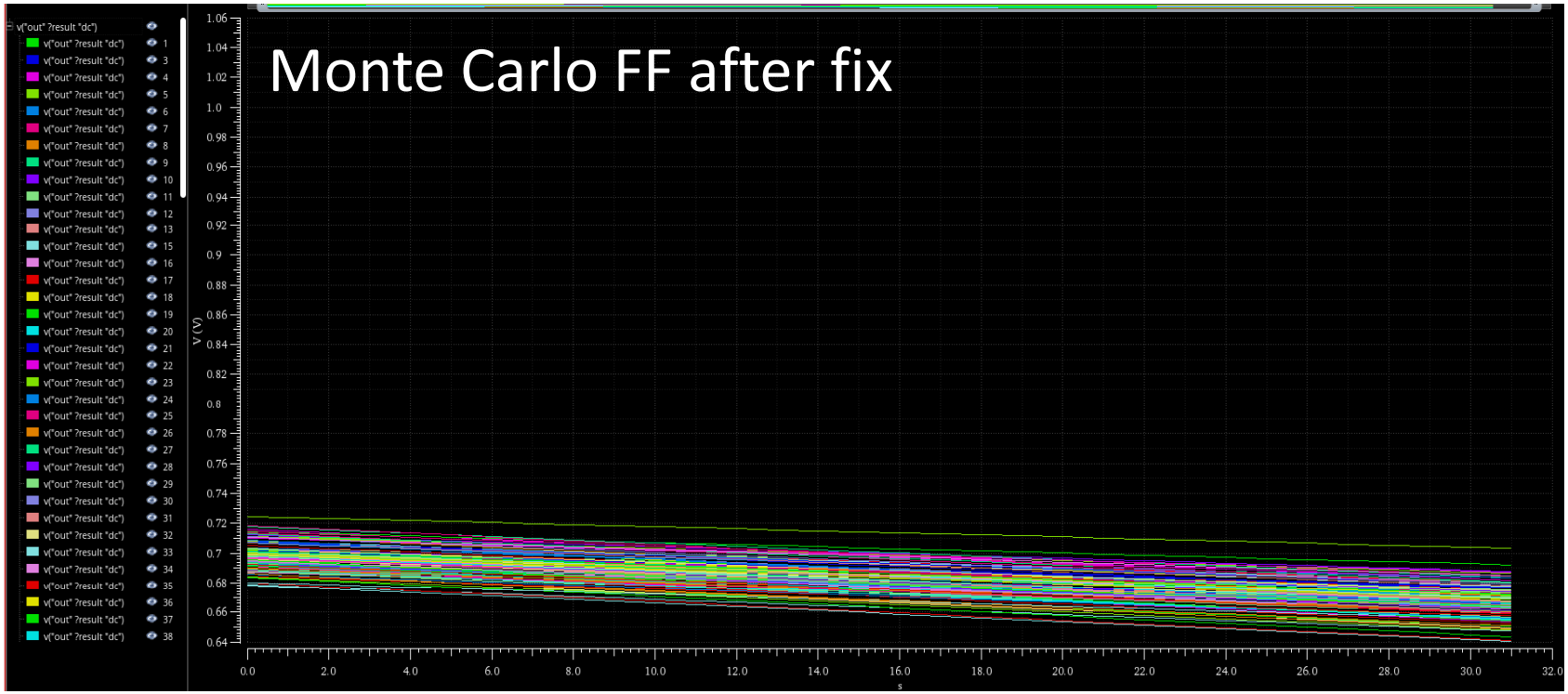
Threshold Trimming Issue Simulation





Threshold Trimming Simulation after Fix





Summary of Locking Issue

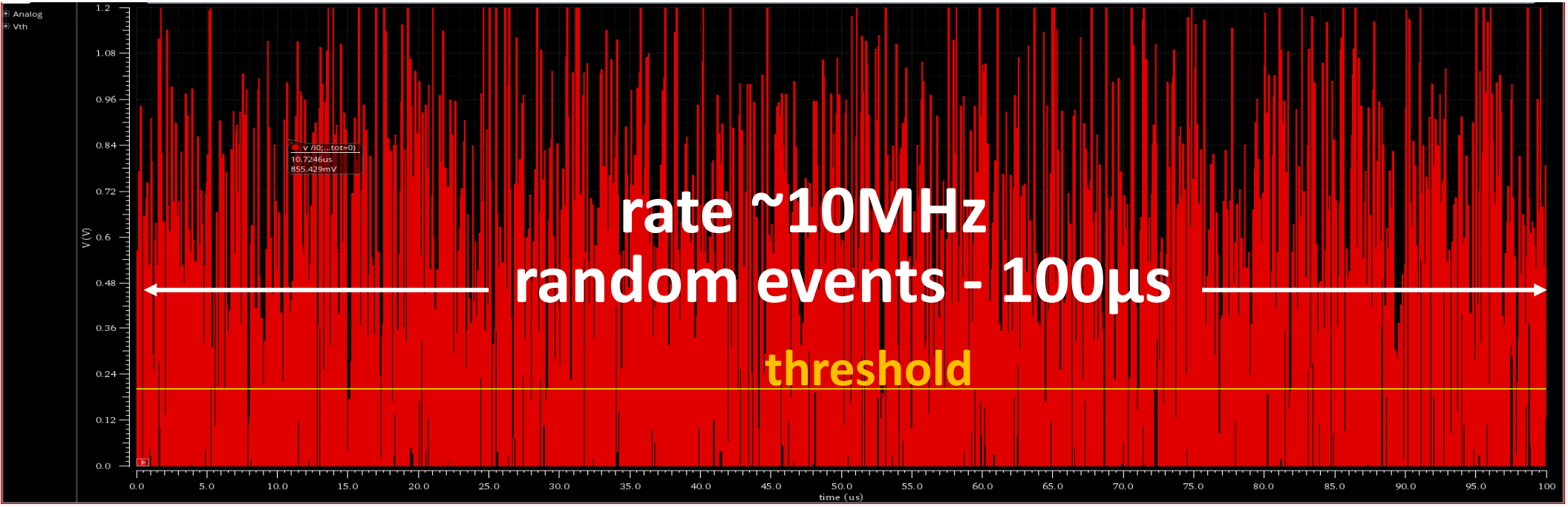
- **Issue** - In time-over-threshold (ToT) the channel locks after few events; unlocking requires acquisition-reset

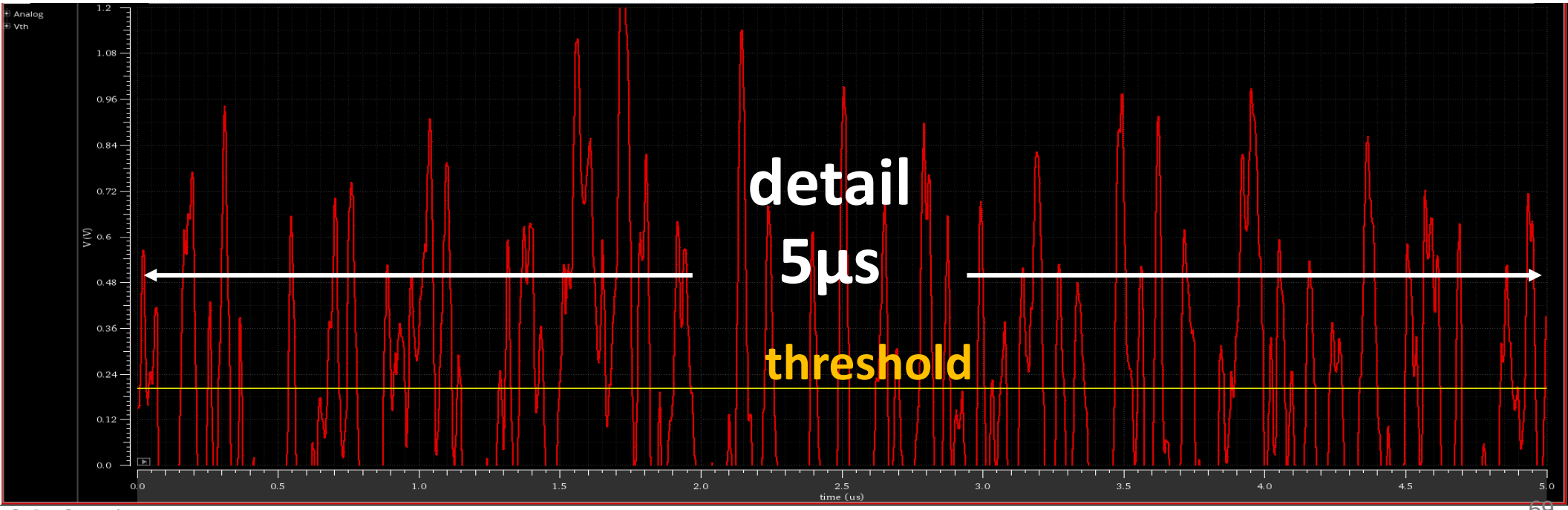
- **Origin** - Conflict between reset signals in discrimination logic; may also result in occasional single event miss at high rate for some settings

- **Workaround** - No locking occurs when operating in threshold-to-peak (TtP)

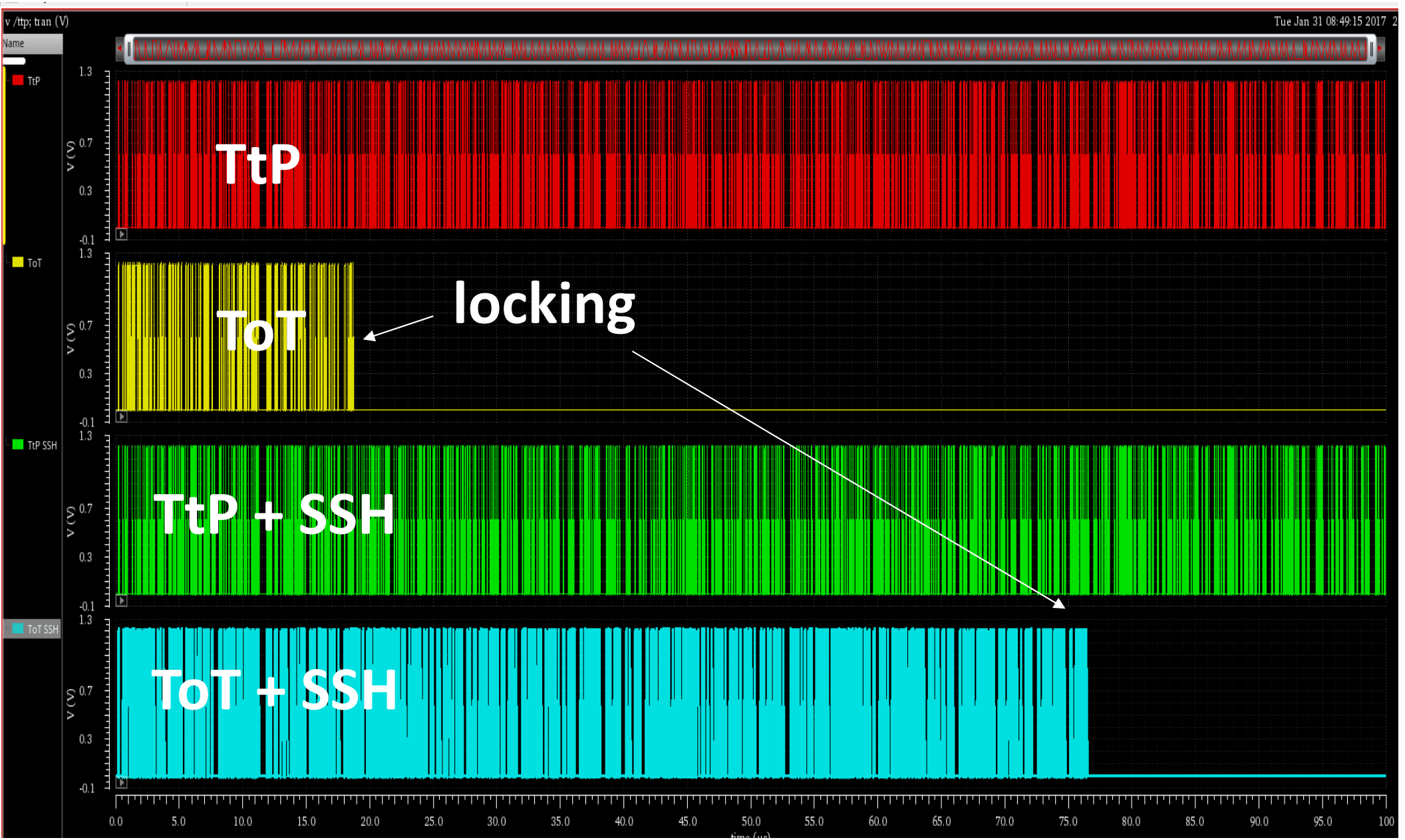
- **Fix** - Small logic fix

Simulated Random High-Rate Input

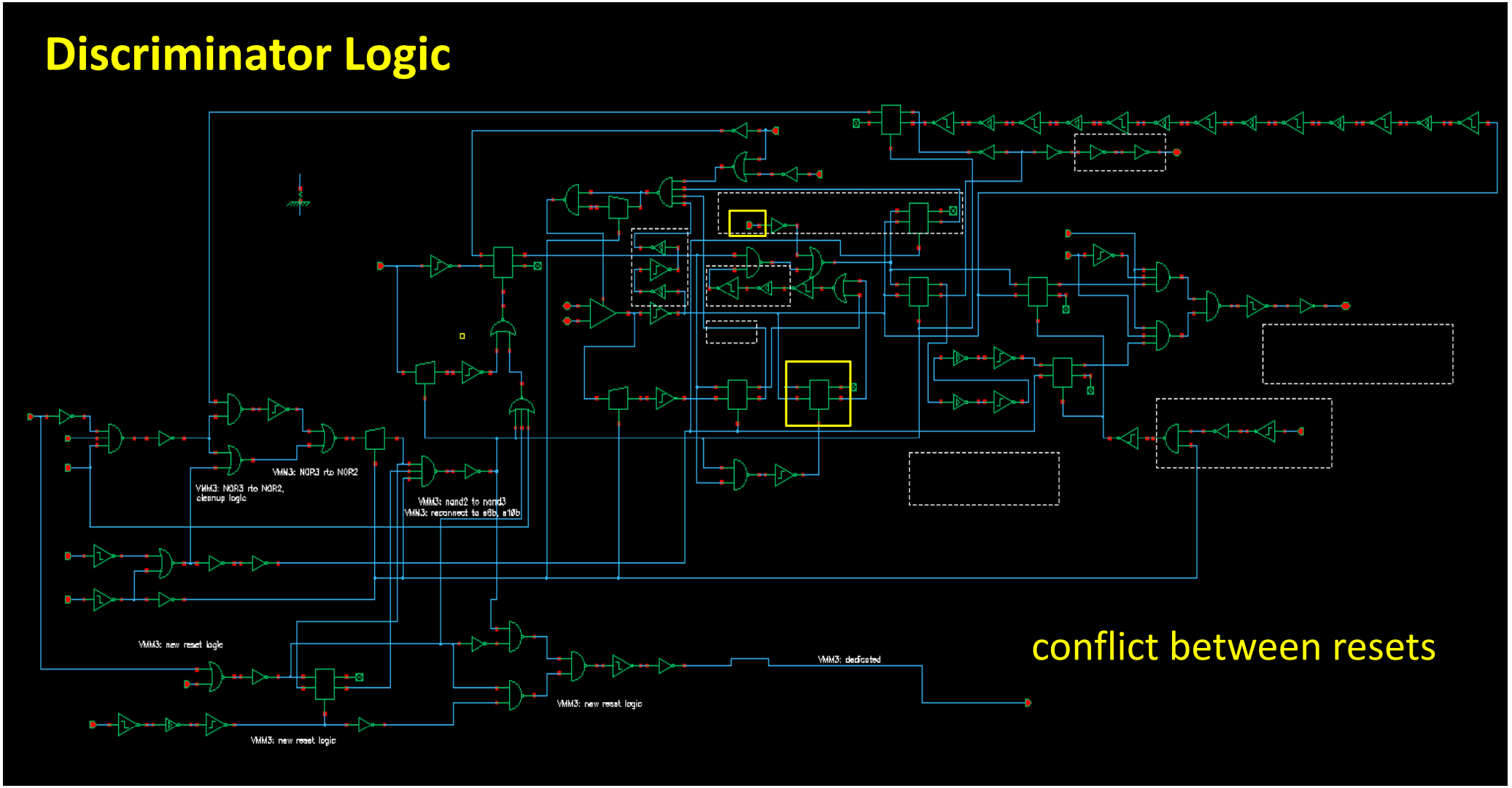




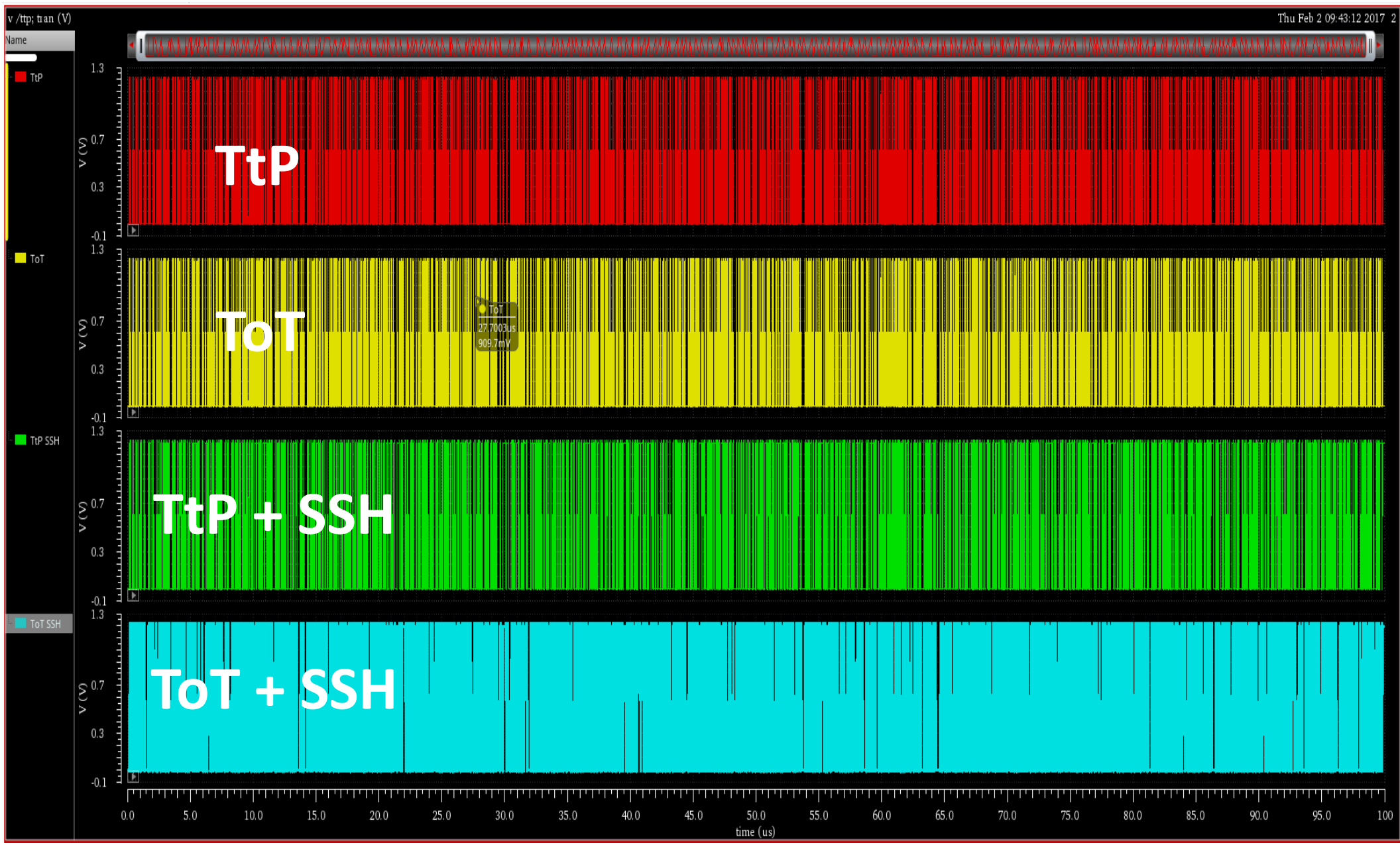
Locking Simulation at Random High Rate



Locking Origin - Circuit Detail



Simulation after Fix



Summary of Acquisition-Reset Issue

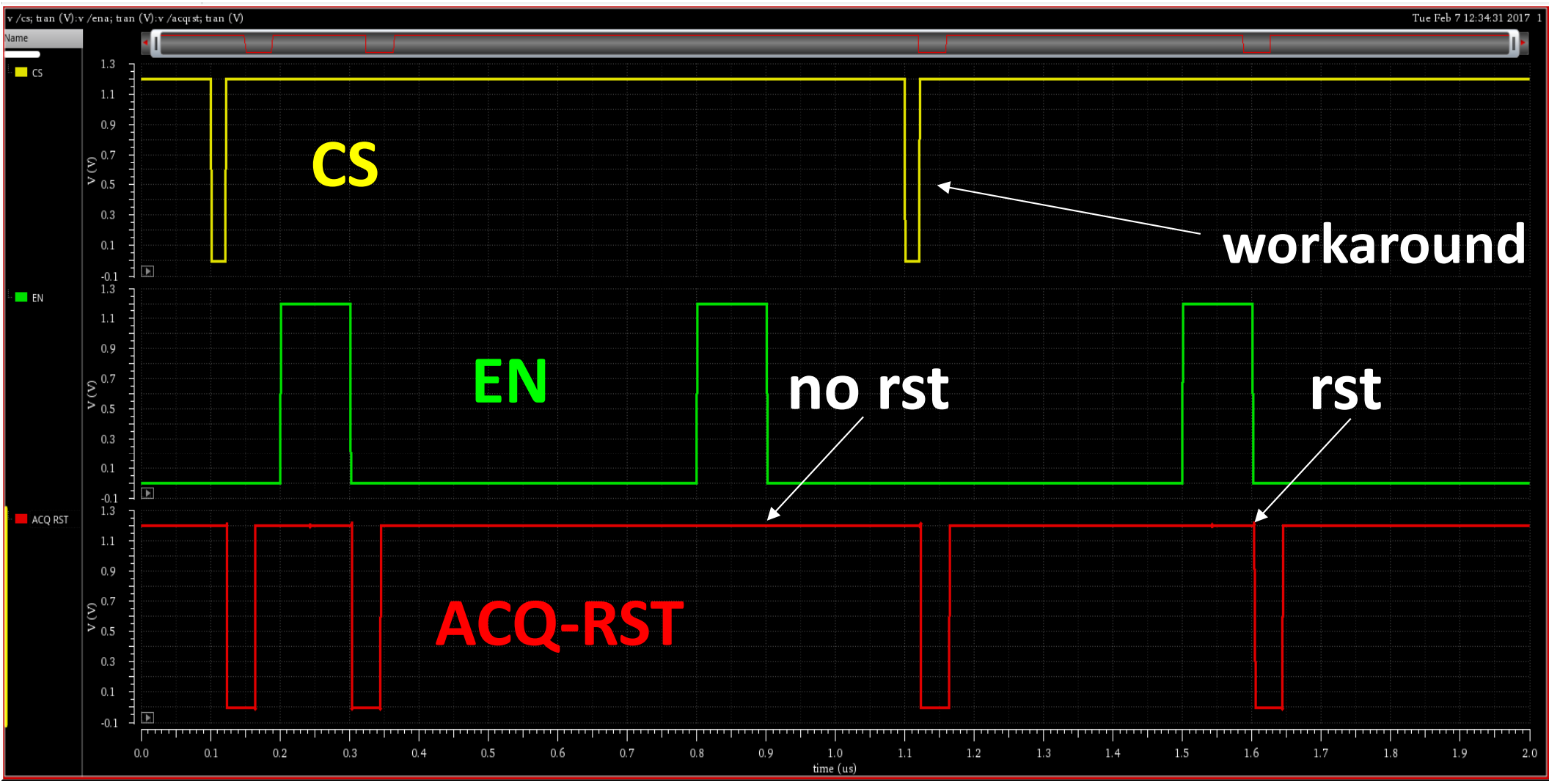
- **Issue** - Acquisition-reset with Enable (EN) works only for one cycle

- **Origin** - Wrong reset logic on dedicated register

- **Workaround** - Acquisition-reset with Chip-Select (CS) pulse at the end of each cycle

- **Fix** - Small logic fix

Acquisition Reset - Simulation



- Acquisition-reset with EN only with first cycle
- CS can be used as workaround

Acquisition Reset - Circuit Detail