VMM L0 testing - Update

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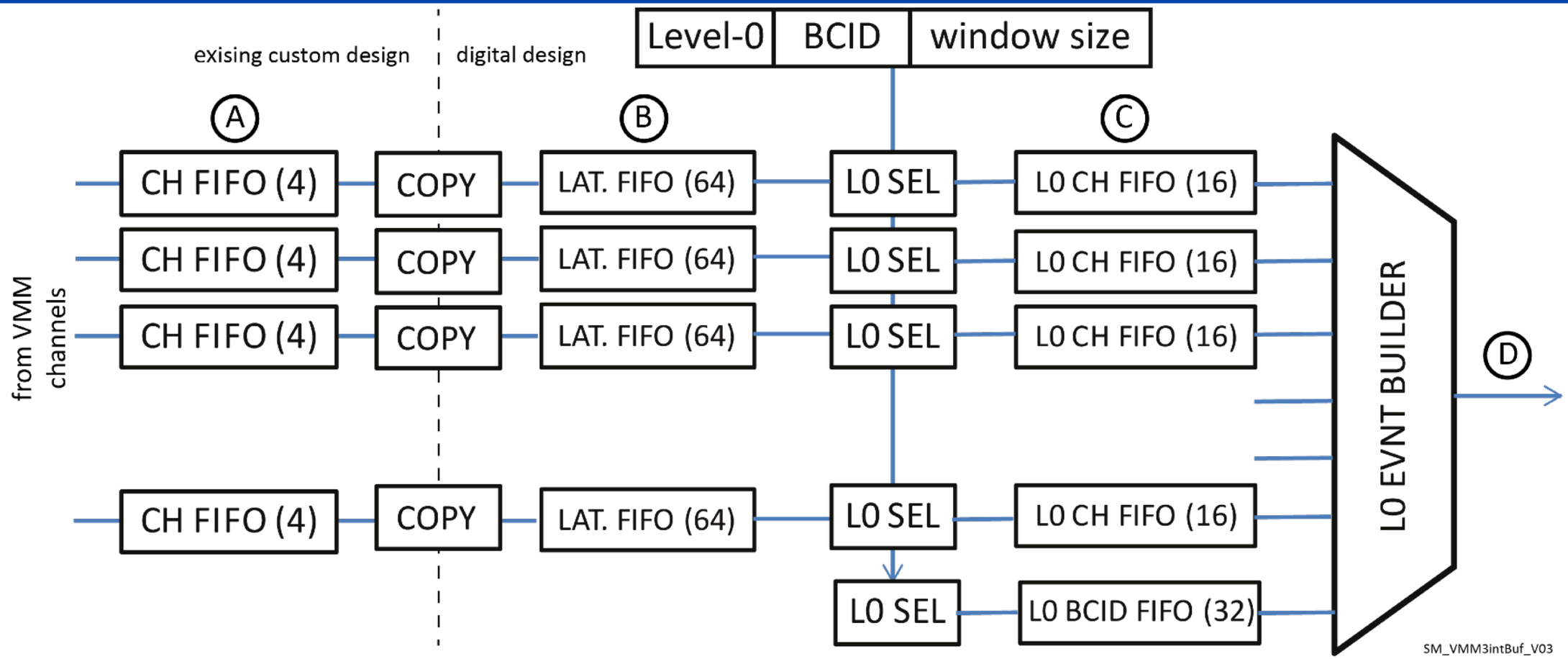
L0 functionality



- Each channel has a Level-0 Selector circuit which is connected to the output of the channel's latency FIFO. The selector finds events within the BCID window (maximum size of 8 BCs) of a Level-0 Accept and copies them to the L0 Ch FIFO
- On every BC clock, if the hit data becomes older than the Level-0 window, the data is flushed from the latency FIFO.
- If a Level-0 Accept is received for the given BCID and the BCID field of the hit data is inside the Level-0 window the hit data is copied to the following Level-0 FIFO and send out.
- If a channel's L0 Sel circuit does not find a hit with a BCID falling within the window, a 'no data' item (first bit equal 0) is passed to the L0 Ch FIFO for that BCID.

L0 Data format and registers

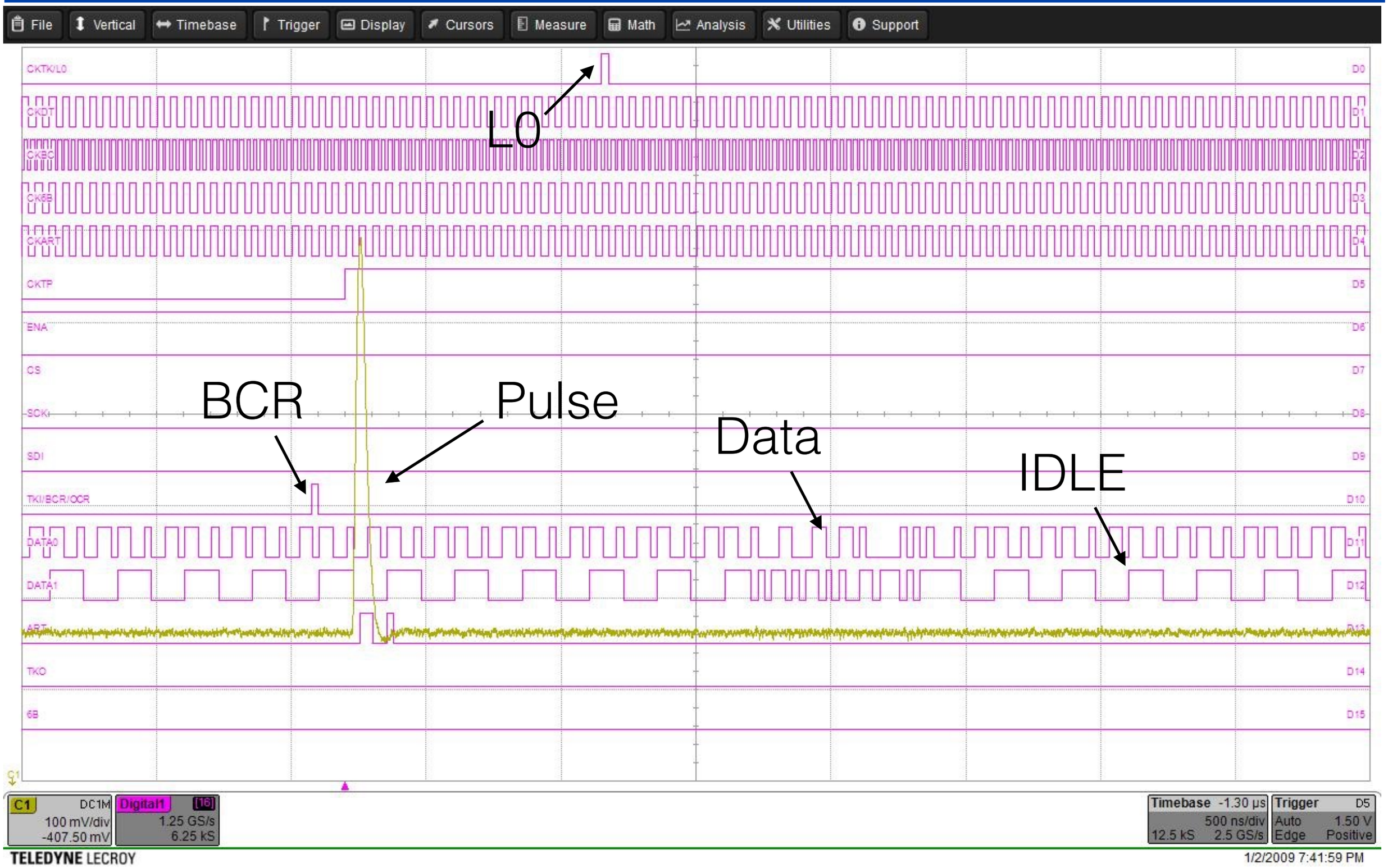
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
header	V	P	orb		BCID (12)												1st word after comma															
hit data	1	P	*R*	T	Chan# (6)						ADC (10)										TDC (8)								N	rel BCID		

LL_format_VMM3out_V04

- The header, and at least two preceding commas, is always sent, even when there are no following hits. The truncation bit, “T”, indicates that the number of hits exceeded the (configurable) maximum for a VMM and that further hits for this Level-0 trigger have been discarded. It is set in the last hit that is transferred.
- Once the overflow bit, “V”, in the BCID word is active, only the header is output; the BCID read from the BCID FIFO is the first BCID for which the overflow occurred.
- If a BCID word written into the BCID FIFO would cause the FIFO to be full, it is written with a BCID of 0xFE8 (magic BCID).

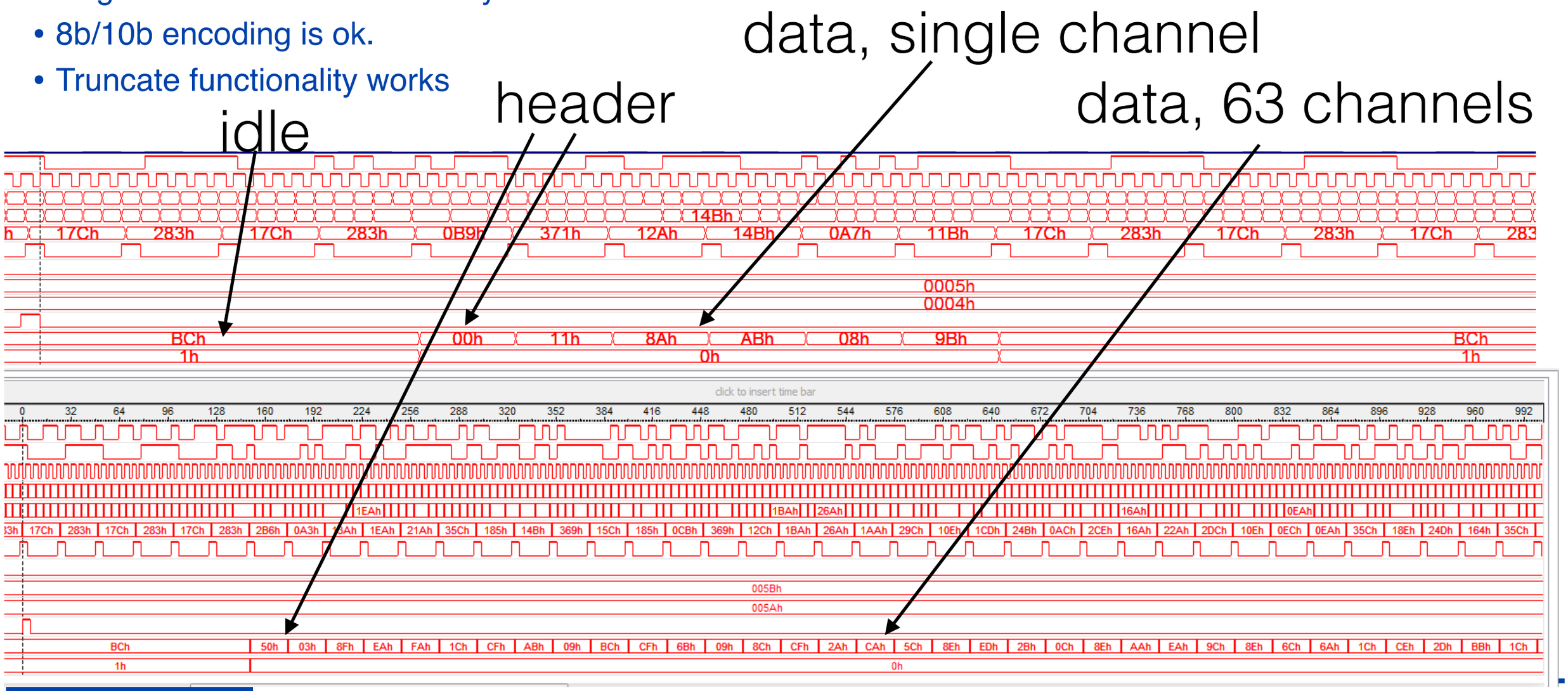
Global bits (defaults are 0)	**Description**
sL0enaV	disable mixed signal functions when L0 enabled
sL0ena	enable L0 core / reset core & gate clk if 0
l0offset_i0:11	L0 BC offset
offset_i0:11	Channel tagging BC offset
rollover_i0:11	Channel tagging BC rollover
window_i0:2	Size of trigger window
truncate_i0:5	Max hits per L0
nskip_i0:6	Number of L0 triggers to skip on overflow
sL0cktest	enable clocks when L0 core disabled (test)
sL0ckinv	invert BCCLK
sL0dckinv	invert DCK
nskipm_i	magic number on BCID - 0xFE8

L0 testing - Screenshot from the scope



L0 Data readout

- L0 logic enable works correctly, the core is functioning, no additional noise if observed.
- IDLE state works (**swapped the Data0/1 lines found**), comma character 0xBC is ok after swapping (k28.5)
- Header format is correct, BCID is identified correctly
- Data format, relative BCID, channel ID, OCR, BCR works correctly are correct.
- Multiple L0 give the correct amount of DATA
- Registers are handled correctly
- 8b/10b encoding is ok.
- Truncate functionality works

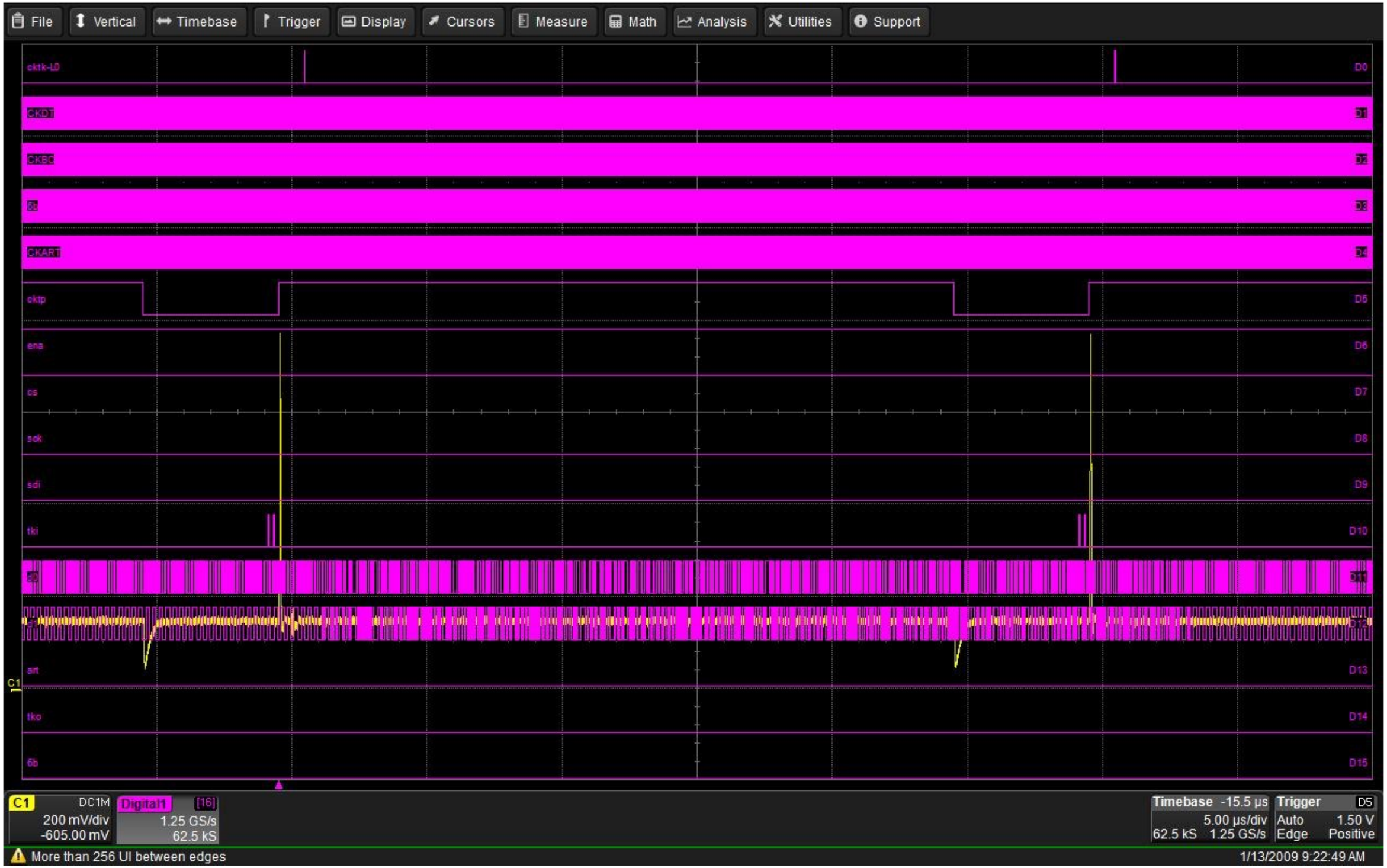


L0 testing - Rate calculation

- Total 63 out of 64 channels giving data (one channel was dead).
- Event size is 32-bits data per channel + 16-bits headers, total 2438-bits (including 8b/10b encoding).
- Readout clock is set at 20MHz (limitation of the test system I currently have).
- Readout rate DDR, 2 Data lines, 80Mbps
- Overflow should not be seen if data are ~31μsec apart (channel FIFO)
- Magic BCID should be seen if data are <15μsec apart

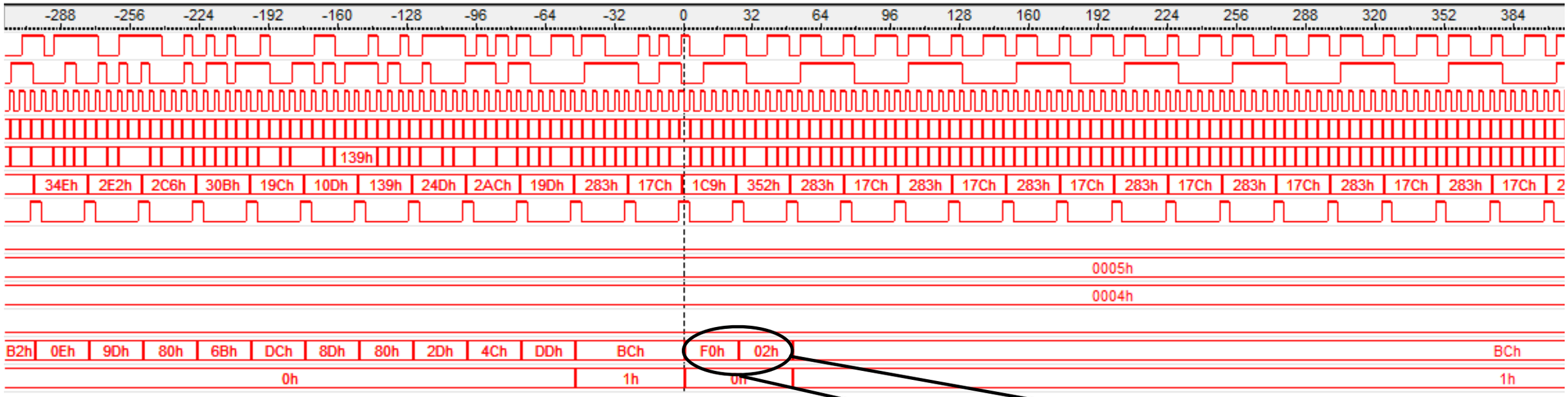
L0 testing - Data feed

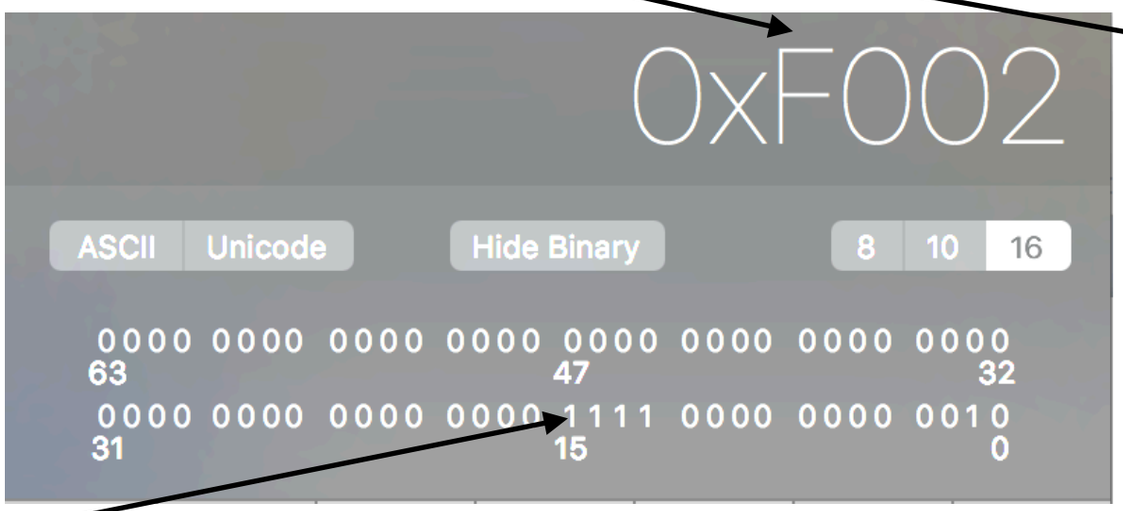
- Data are sent every 30µsec



L0 testing - Channel fifo Saturation

- Saturation occurs at Channel Fifo as expected, Bit “V” is on. Only header is sent followed by IDLE.





only header
no data

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
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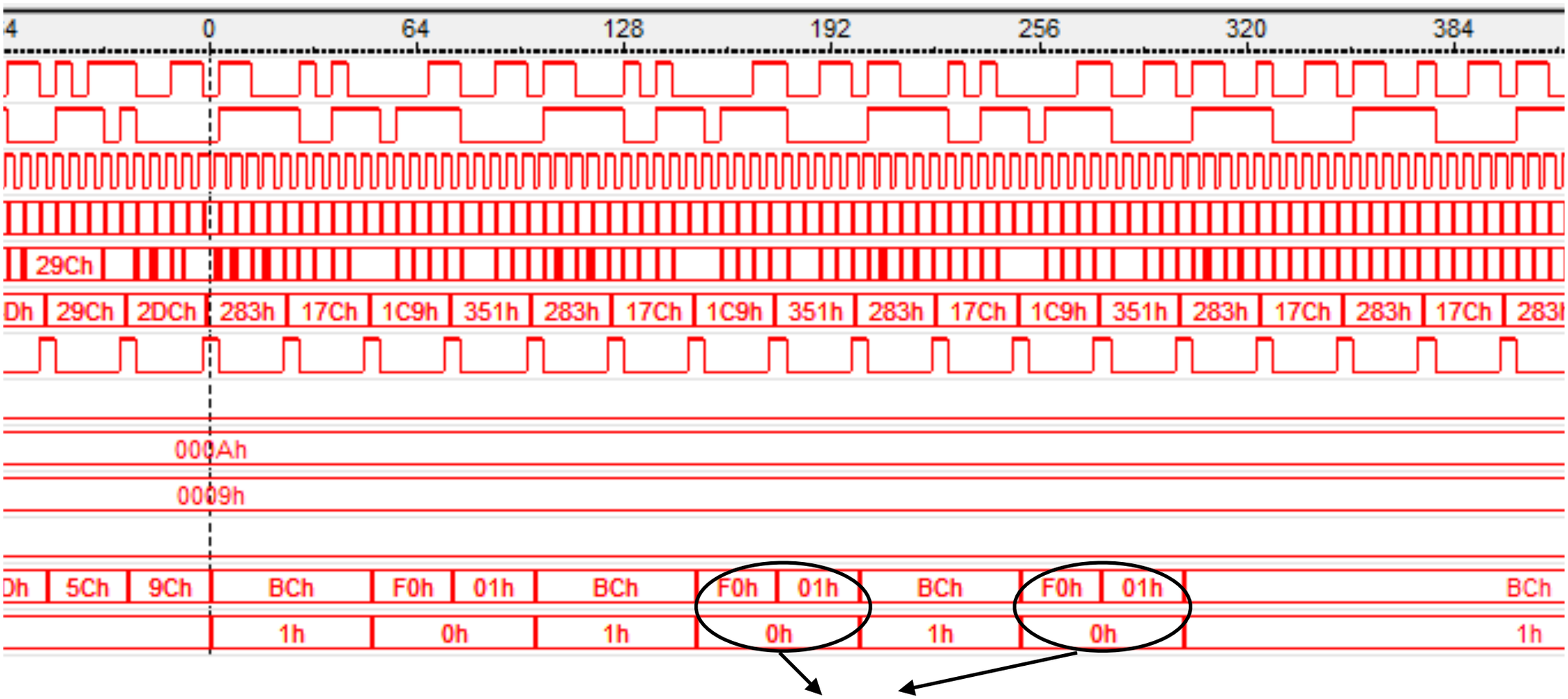
L0 testing - Channel Saturation

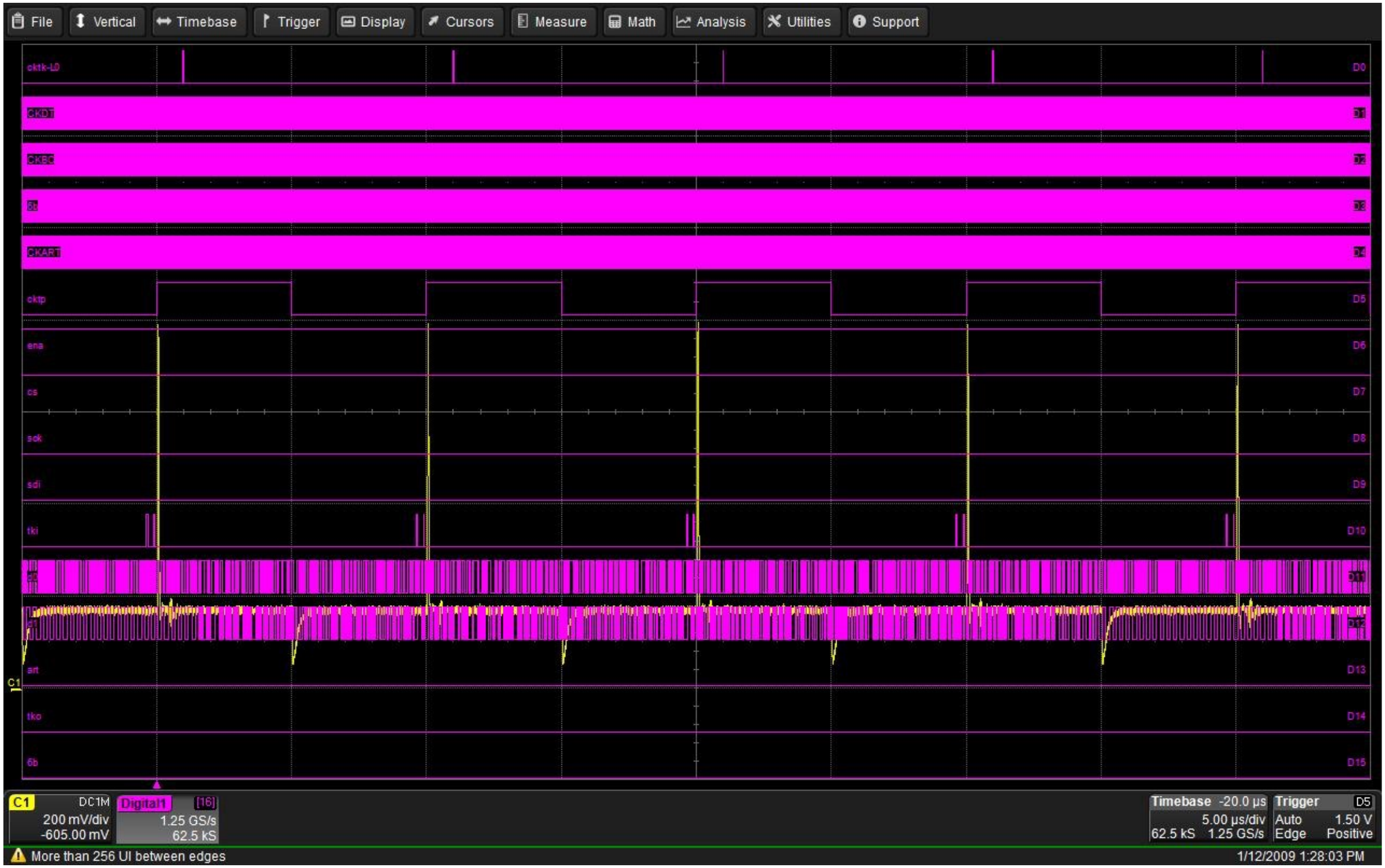
- Once the rate becomes even higher then multiple headers indicating saturation are coming…



multiple saturation

BCID fifo testing - Saturation

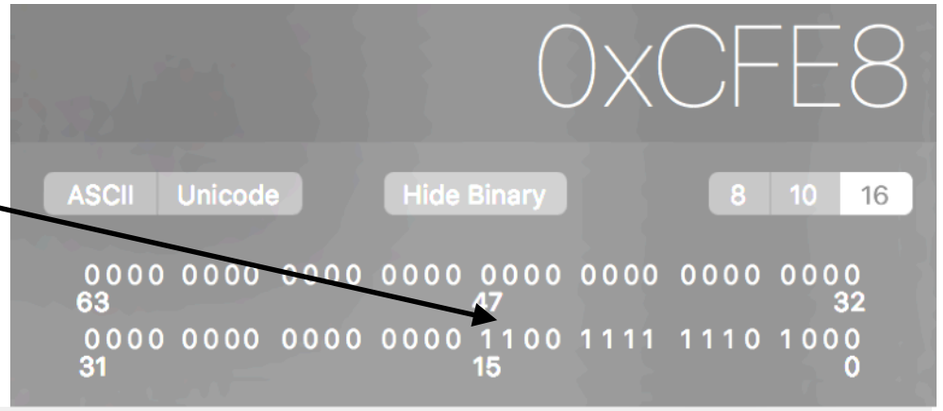
- Data are sent every 10µsec

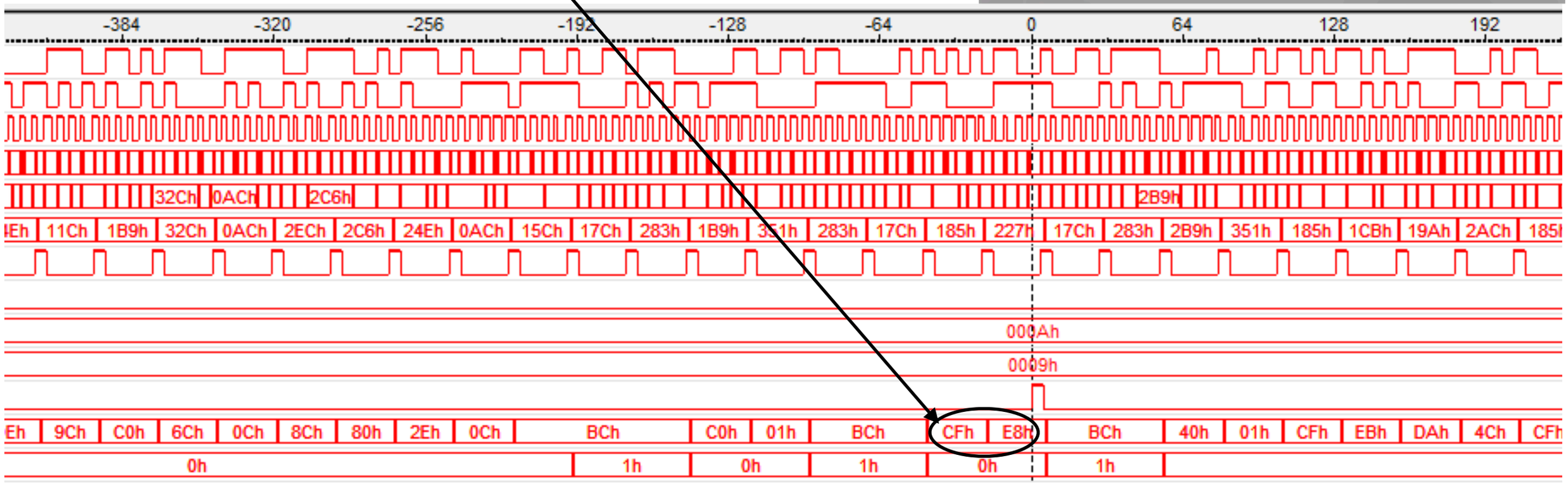


L0 testing - Magic BCID on BCID fifo saturation

- If a BCID word written into the BCID FIFO would cause the FIFO to be full, it is written with a BCID of 0xFE8 (this BCID cannot occur with the LHC) and the parity bit in the header is set to indicate a parity error. The overflow bit, “V” is set depending on whether the corresponding hit word was entered or not in the channel FIFO. When the ROC receives this header it knows not to expect even a header from the next ‘Nskip’ Level-0 Accepts.

parity bit is also on





Summary

- **L0 core works as expected, Data lines look swapped though**
- **Register functionality is correct**
- **Data format, headers are according to the specifications**
- **FIFO overflow is handled correctly and identified correctly**
- **BCID overflow works as expected**
- **System should though be tested with a 160MHz clock to see if the functionality remains unchanged, no surprises expected.**
- **More testing will be done by dumping the data for many events. This should be done to check for problems if any that are more rare.**