Electronics, Trigger and Data Acquisition

part 1

Summer Student Programme 2017, CERN

July 5, 2017

Roberto Ferrari
Instituto Nazionale di Fisica Nucleare

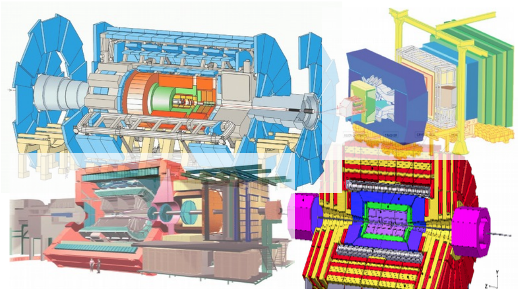
roberto.ferrari@pv.infn.it

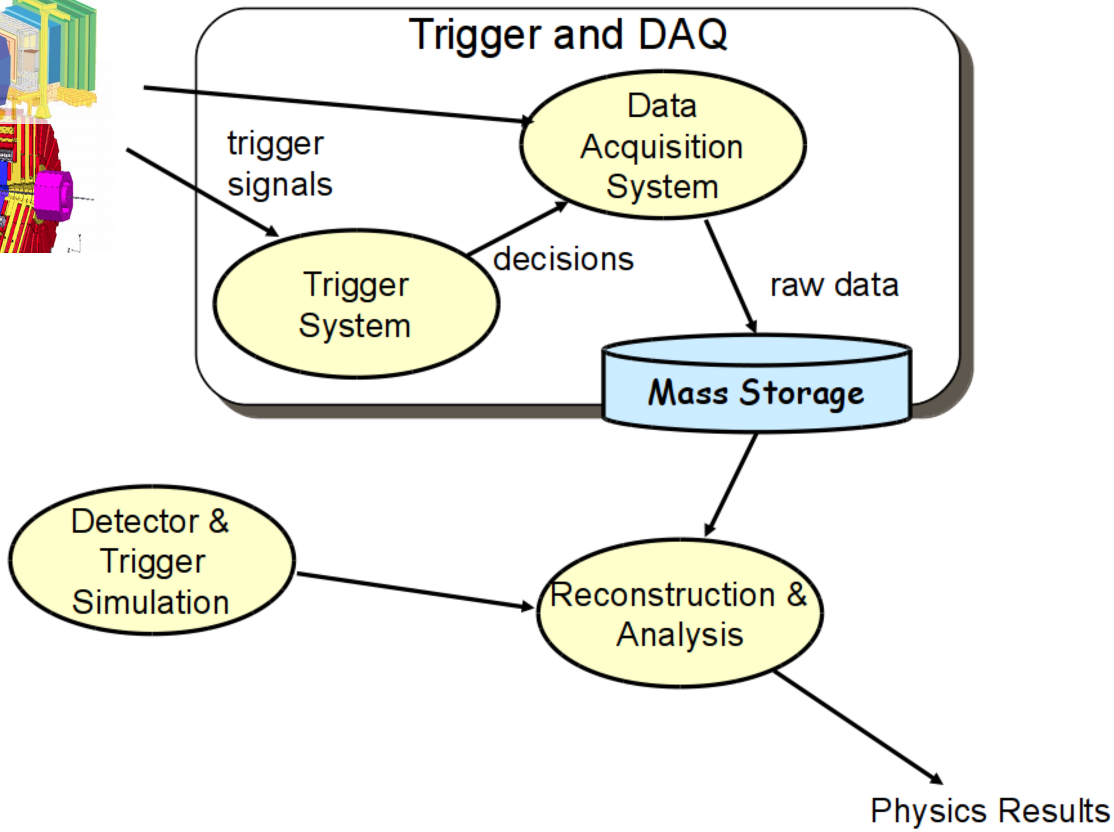
Introduction

- Lectures will be concerned with Data Acquisition (DAQ) in High-Energy Physics …
- Data acquisition is an **alchemy** of electronics, computer science, networking, physics
  - …, resources and manpower matter as well, …
- Topics are pretty much correlated → you will realise this in the lecture non-linearity

Credits: material and ideas come largely from my predecessor (Wainer Vandelli) and from the lectures of ISOTDAQ schools (http://isotdaq.web.cern.ch/isotdaq/isotdaq/Home.html)

General Overview





- main role of Electronics, Trigger & DAQ is to process signals generated in “a detector”, likely storing all useful information in some safe place

Signals ?

- Sometimes, somewhere in our detector, something (“one event”) happens, i.e. in some short time several particles interact within it.
- In High-Energy Physics, even a single event is composed by sequences of many different probabilistic (quantum-mechanics) processes → fluctuations are built-in
- At the end, “electrical” signals arrive at detector output terminals. Different signals:

  a) have different characteristics (size, arrival time, duration, …)

  b) carry different, (likely) independent, information

  c) need quite some electronics in order to become “profitable”

Electronics

[Horowitz & Hill, The Art of Electronics]

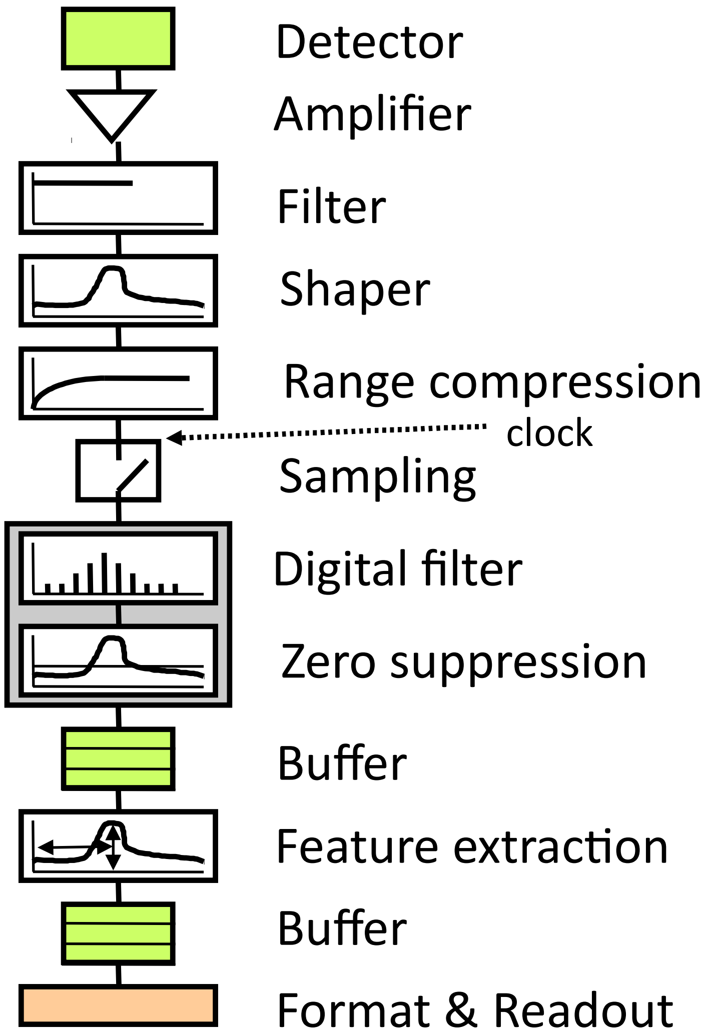
Role ?

- Sense, transform and collect electrical signals from detector(s) – very often short current/light pulses (i.e. bunches of electrons or photons)
  - you may be interested in total charge or in signal time or in both

- Adapt signals to optimize different, **conflicting**, characteristics → balance:
  - minimum detectable signal (min. noise and max. signal-to-noise ratio)
  - maximum detectable signal (dynamic range)
  - speed (signal rate)
  - timing
  - pulse shape dependence

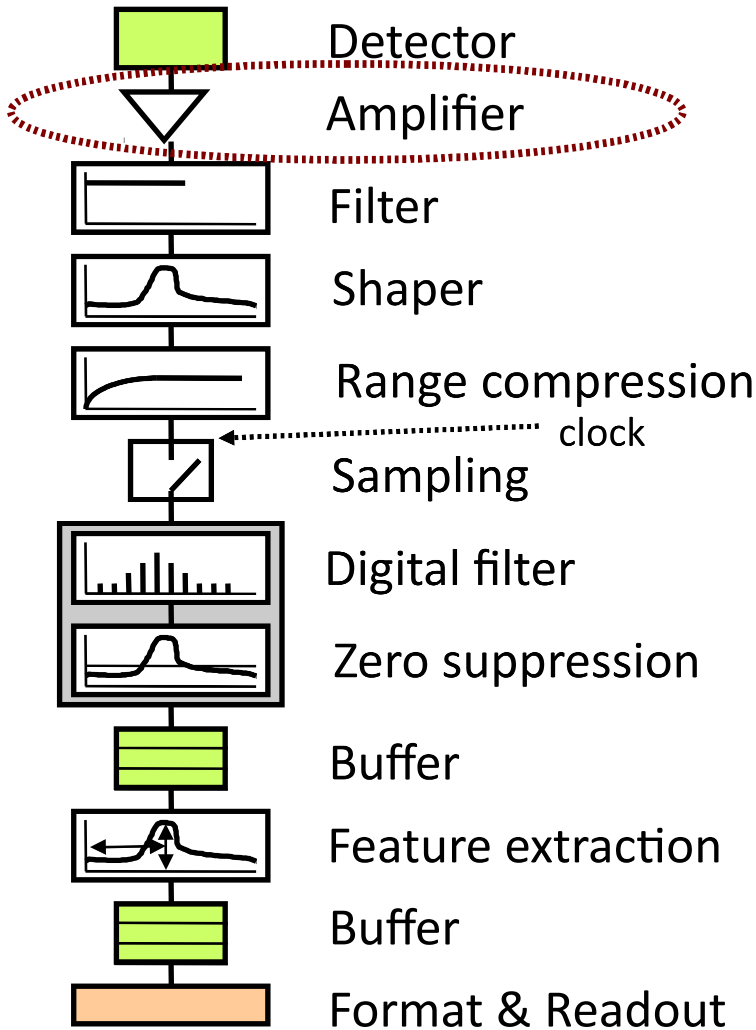
- Digitize and preserve information
  - allow for subsequent processing, transmission, storage using digital electronics → computers, networks, …

Read-Out Chain



- Front-end electronics very specialized
  - custom-built to match detector characteristics
- Cannot discuss all design and architecture details
  - if you are into electronic design you already know more than me
- Find yourself dealing or choosing commercial electronics
  - provide you with base guidelines
- Selected functions and principles

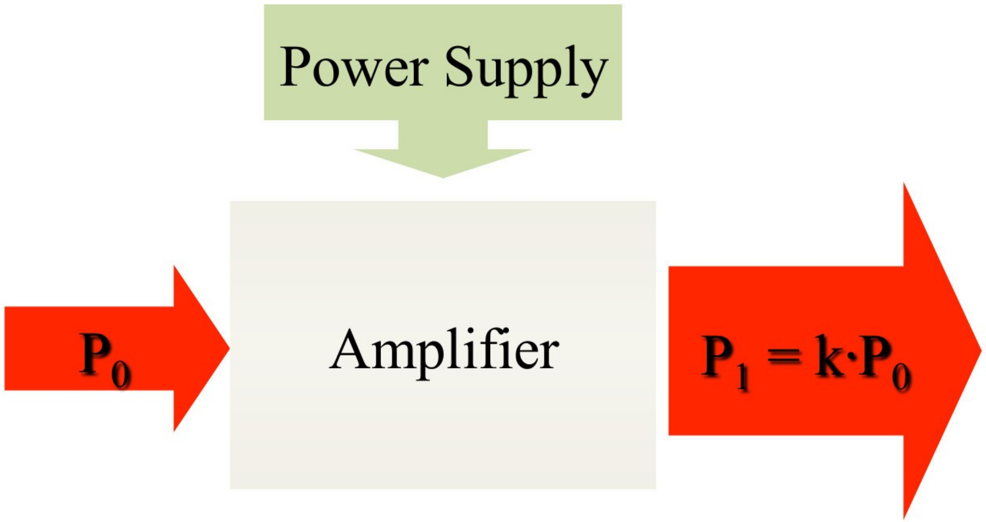
Read-Out Chain



Amplifiers

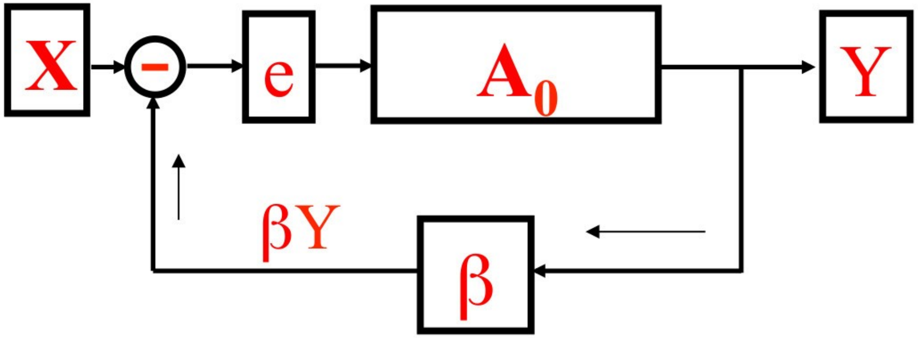
Amplifier: *powered black box connected that receives an input signal with power* P_0 *and produces an output signal with amplified power* P_1

Open loop gain: $k = P_1 / P_0$ *(usually very large)*



Negative Feedback

Part of the output signal Y is sent back to cancel some of the input:



$$Y = A_0 e = A_0(X - \beta Y) \rightarrow Y\,(1 + A_0\beta) = A_0 X$$

$$Y = \frac{A_0}{1 + \beta A_0} X$$

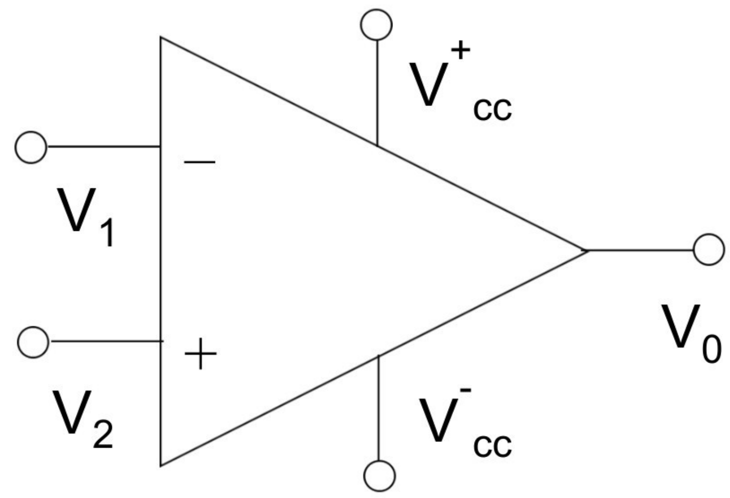
If $A_0 >> 1 \rightarrow Y = X/\beta$

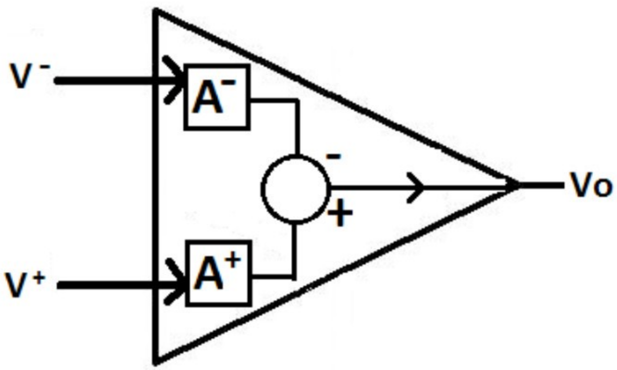
$\rightarrow$ *stable and controlled gain (1/β)*

Operational Amplifiers

Voltage amplifiers with:

- *differential input*
- *high gain ($A^+ = A^- = \infty$)*
- *high input impedence ($Z_{in} = \infty$)*
- *low output impedence ($Z_{out} = 0$)*



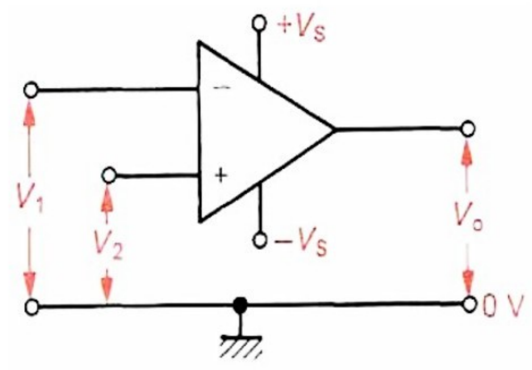


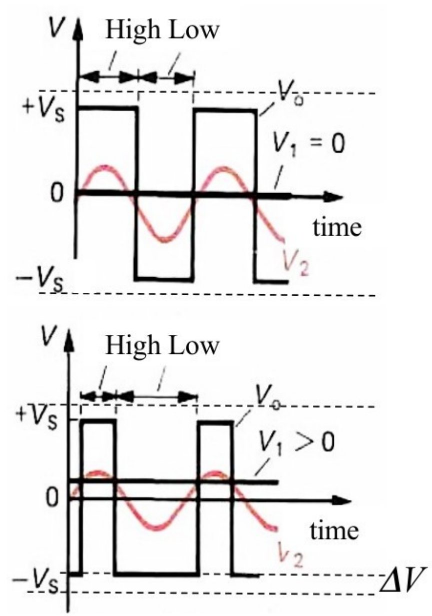
$$\mathbf{V_0 = A^+ V_2 - A^- V_1 = A^+ V^+ - A^- V^-}$$

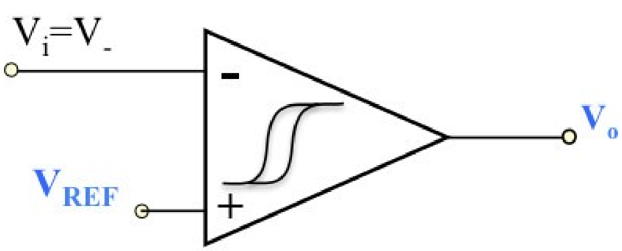
The output voltage V0 is the sum of:

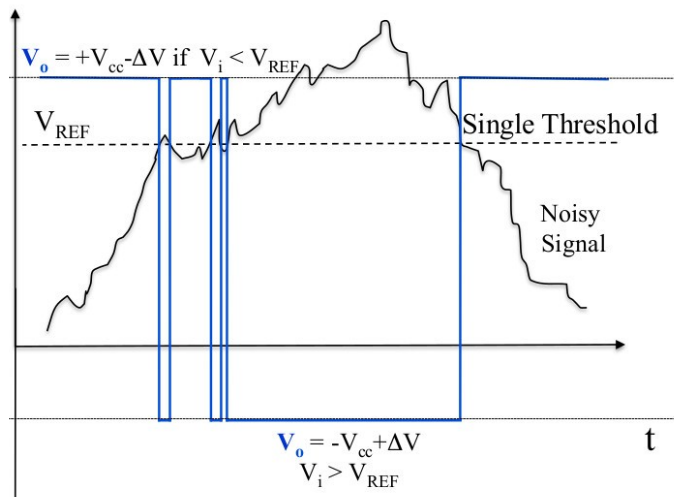
- the signal at the inverting input (-) , V_1 , inverted and amplified by A^-
- the signal at the non-inverting input (+) , V_2 , non-inverted and amplified by A^+

Open-loop Configuration: Comparator

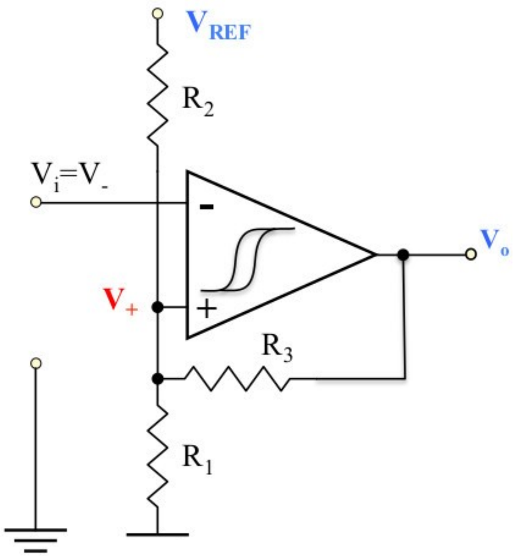


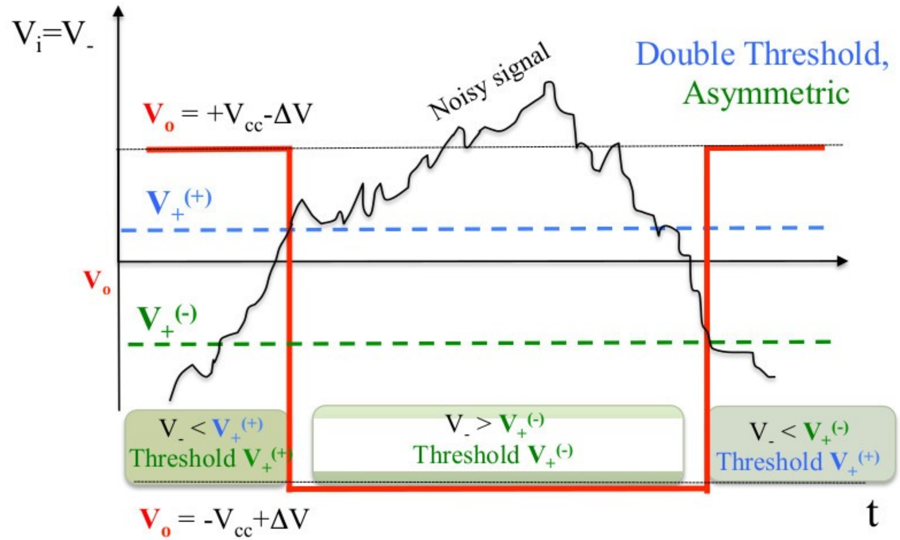


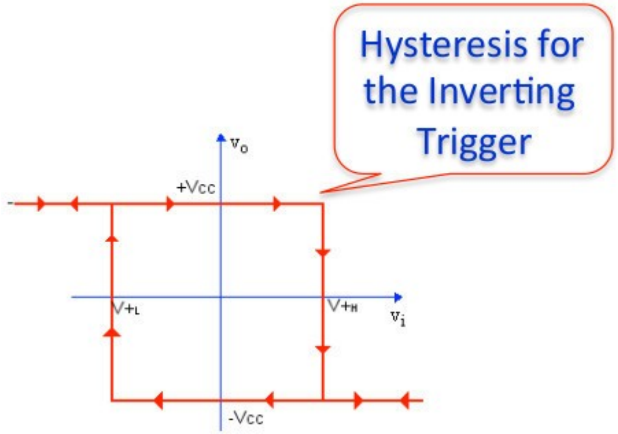




Positive Feedback → Schmitt Trigger







Positive feedback:

- transition speedup

- hysteresis (both output and threshold depend on recent history)

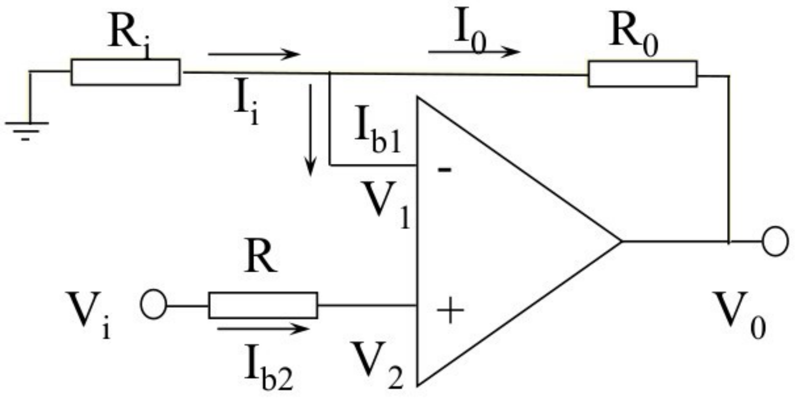
Negative Feedback ...

Golden rules:

1) output keeps zero voltage difference between inputs

2) inputs draw no current

Non-Inverting Amplifier



→

1: $V_1 = V_2$

2: $I_{b1} = I_{b2} = 0$; $I_0 = I_i$

→

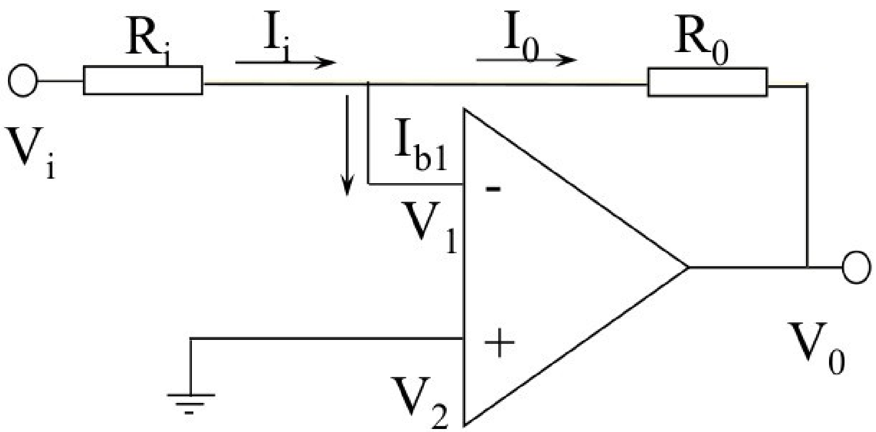
$V_1 = V_i$

$V_0/(R_0+R_i) = V_1/R_i = V_i/R_i$

→

$G = V_0/V_i = 1+R_0/R_i > 1$

Inverting Amplifier



→

1: $V_1 = V_2$

2: $I_{b1} = I_{b2} = 0$; $I_0 = I_i$

→

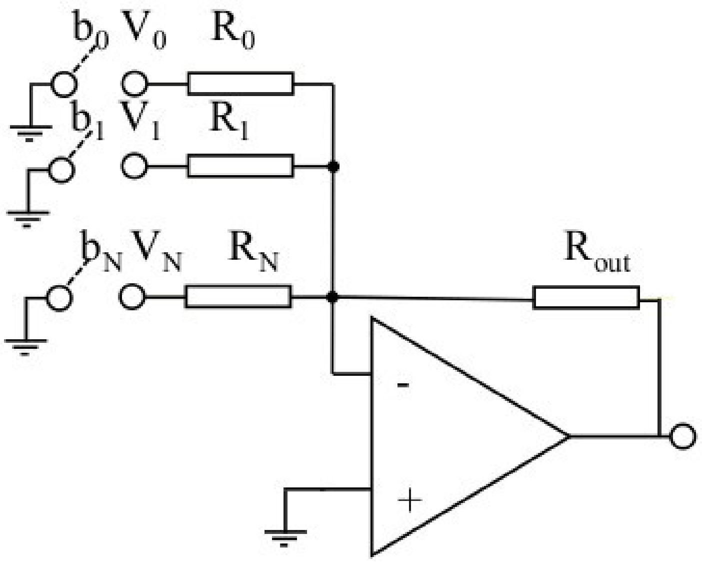
$V_1 = 0$

$V_0/R_0 = -V_i/R_i$

→

$G = V_0/V_i = -R_0/R_i$

Inverting Amplifier → Current Adder → DAC



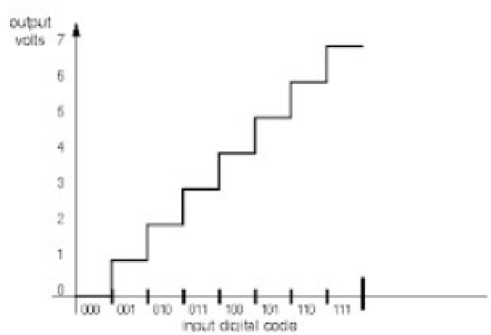
If $V_N = 0$, then R_N is short-circuited (bit at 0)

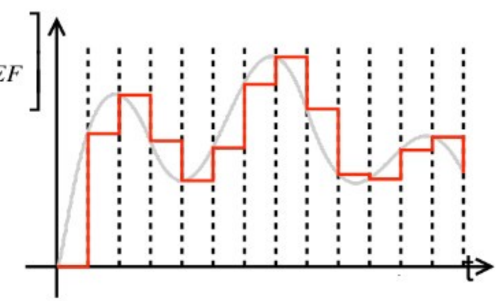
Set $R_{out} = R_0$, $R_1 = 2R_0$, $R_2 = 4R_0$, etc. etc.

$$V_0 = -R_{out}\left(\frac{1}{R_N}V_N + \frac{1}{R_1}V_1 + \frac{1}{R_0}V_0\right) \quad \text{… case N=3}$$

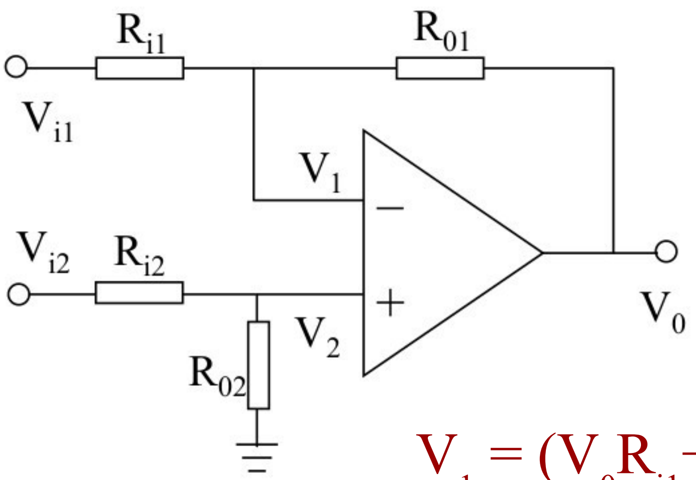
$$V_0 = -V_{REF}\sum_{i=0}^{N-1=2}\frac{b_i}{2^{N-i}} = -V_{REF}\left(\frac{b_2}{2} + \frac{b_1}{4} + \frac{b_0}{8}\right)$$

$$V_0 \in -\left[0, \frac{1}{8}V_{REF}, \frac{2}{8}V_{REF} \cdots\cdots \frac{7}{8}V_{REF}\right]$$





Differential Amplifier



$$V_1 = (V_0 R_{i1} + V_{i1} R_{01})/(R_{i1} + R_{01})$$

$$V_2 = V_{i2} R_{02}/(R_{i2} + R_{02})$$

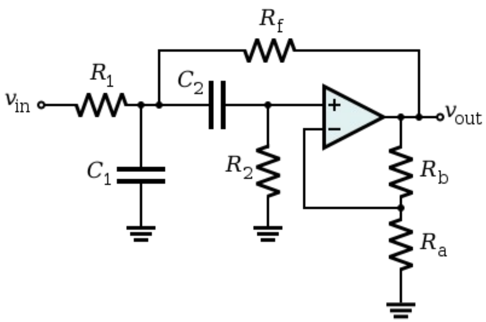
$$\rightarrow V_0 = (1 + R_{01}/R_{i1}) \cdot V_{i2} R_{02}/(R_{i2} + R_{02}) - V_{i1} R_{01}/R_{i1}$$

$$\text{if } R_{02}/R_{i2} = R_{01}/R_{i1} = G$$

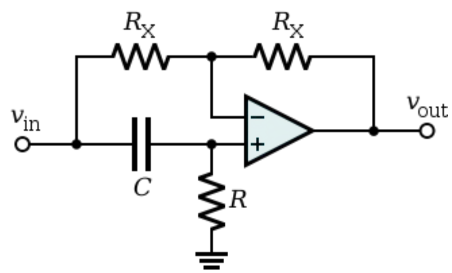
$$\rightarrow V_0 = G \cdot (V_{i2} - V_{i1})$$

Some Magics …

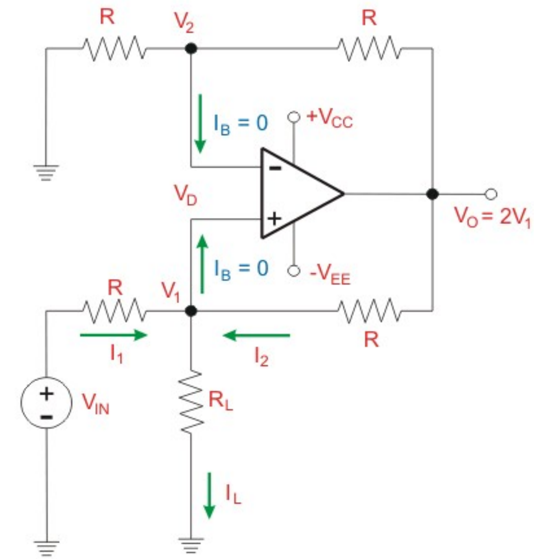
Band-pass Filter



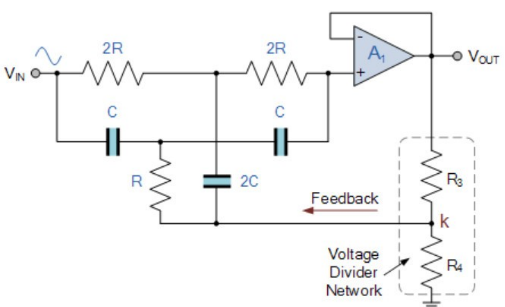
Phase Shifter



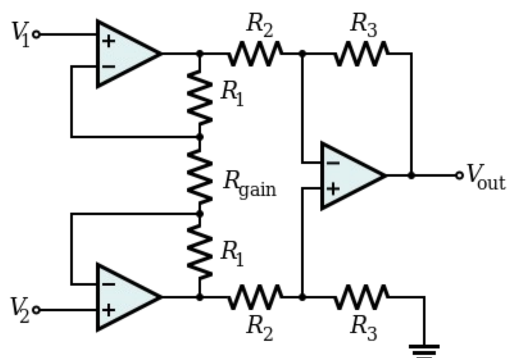
Voltage-to-Current Converter



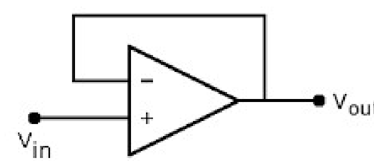
Band-stop Filter



Instrumentation Amplifier (High CMRR amplifier)



Buffer!

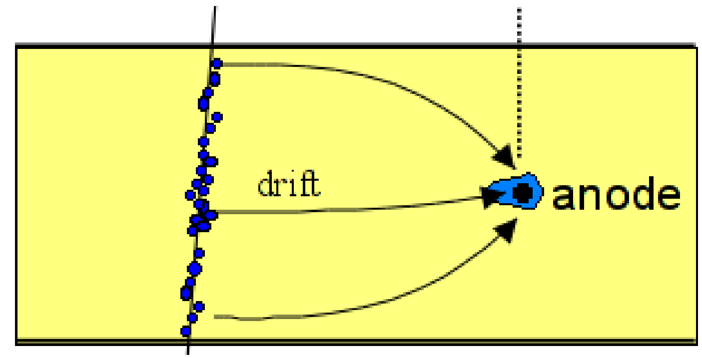


and billions of others …

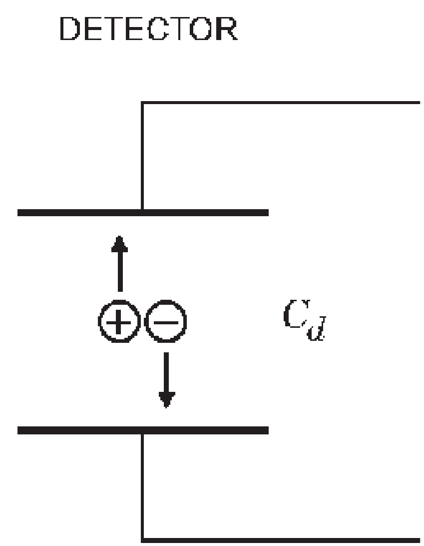
Back to signals: what can a signal be ?

- Detectors may be electrically represented as a capacitor (Cd)
  - more realistic schemes will include other contributions

- Interactions of passing particle → energy release E → short current pulse i_s



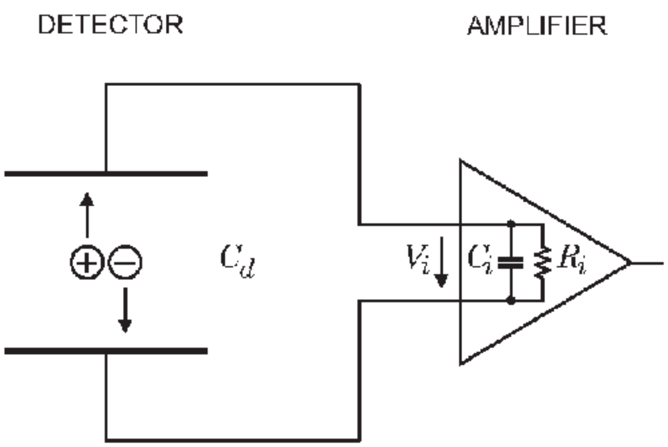
$$E \propto Q_s = \int i_s(t)\,dt$$



- Pulse duration may range from O(100 ps) up to O(10 μs)

Voltage-Sensitive Amplifier

- Signals are possibly very small, amplify to:
  - improve signal resolution, adapt it to next stages
  - avoid SNR degradation ...



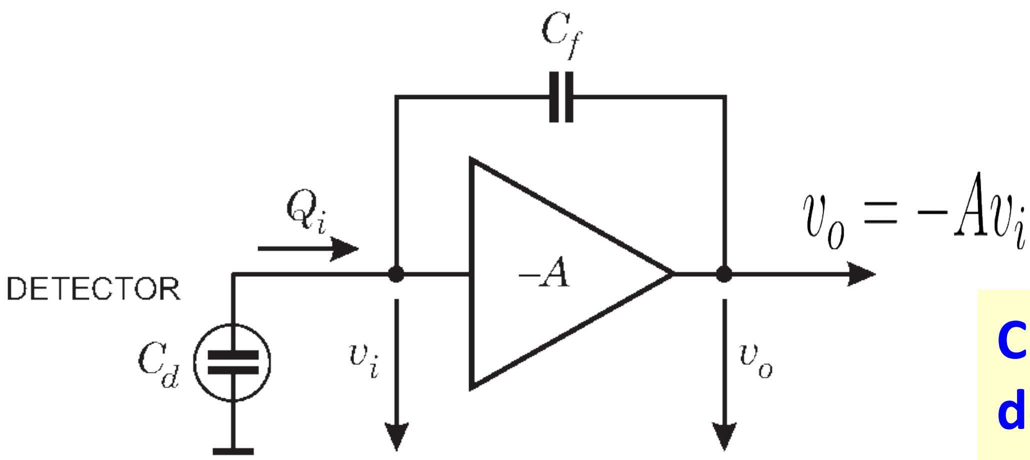
Using a simple voltage amplifier, the sensed **input voltage V_i depends on the detector capacitance.**

Detector capacitance could be a function of the operation point (e.g. high voltage) and/or detector dimension.

Additional **calibration** efforts

$$V_i = \frac{Q_S}{C_d + C_i}$$

Charge-Sensitive Amplifier



Charge amplification only depends on a well-controlled component

Effective (dynamic) input capacitance:

$$C_i = \frac{Q_i}{v_i} = C_f(A+1)$$

Gain:

$$A_Q = \frac{v_o}{Q_i} = \frac{Av_i}{C_f(A+1)v_i} = \frac{A}{A+1}\frac{1}{C_f} \approx \frac{1}{C_f} \quad (A \gg 1)$$

Charge Transfer

$$C_i = \frac{Q_i}{v_i} = C_f(A+1)$$

What total-charge fraction is measured ?

$$\frac{Q_i}{Q_s} = \frac{C_i v_i}{Q_{det} + Q_i} = \frac{C_i}{Q_s} \cdot \frac{Q_s}{C_i + C_{det}} = \frac{1}{1 + \frac{C_{det}}{C_i}} \approx 1 \quad (\text{if } C_i >> C_{det})$$

Need **large input capacitance** to maximize charge transfer

Signal-to-Noise Ratio (SNR)

- Improving SNR improves sensitivity (minimum detectable signal)
- Electronic noise does not necessarily dominate each measurement

$$\Delta E = \sqrt{\Delta E^2{}_{fluc} + \Delta E^2{}_{noise}}$$

Fluctuations due to physical detection process (e.g. energy deposition) or detector readout (e.g. photomultiplier)

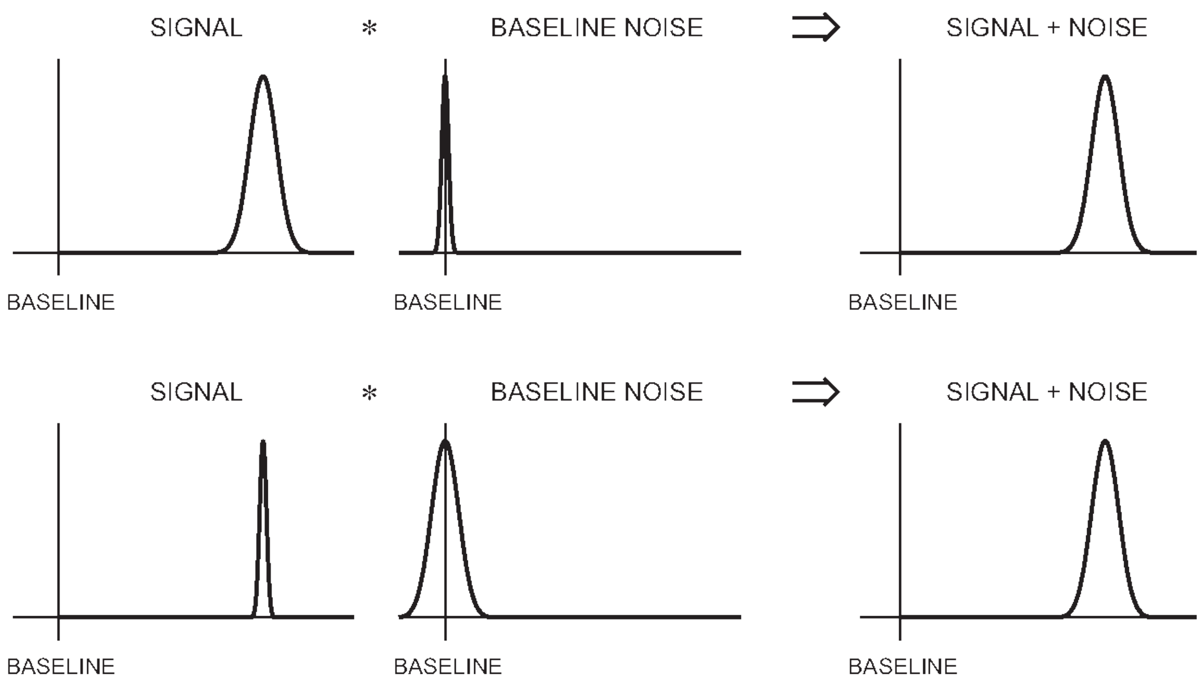
Electronic noise

- Thermal noise: velocity fluctuations in charge carriers
- Shot noise: fluctuations in carrier number (e.g. diode barrier crossing)

Signal-to-Noise Ratio (SNR)

- Improving SNR improves sensitivity (minimum detectable signal)
- Electronic noise does not necessarily dominate each measurement

$$\Delta E = \sqrt{\Delta E^2{}_{fluc} + \Delta E^2{}_{noise}}$$



S/N needs optimization

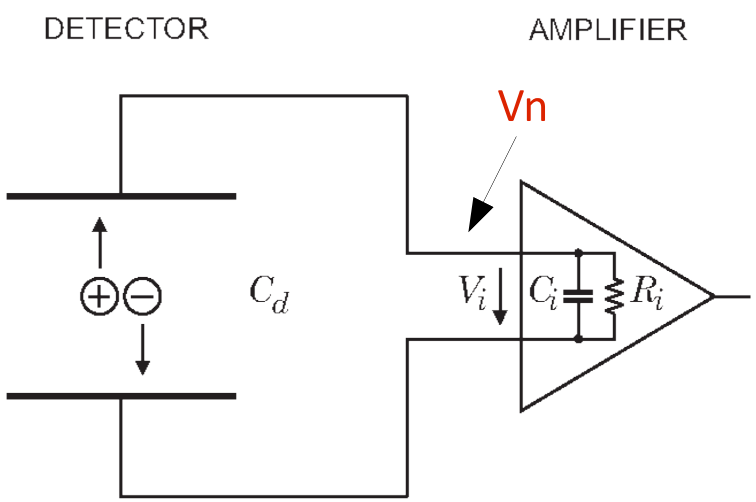
SNR .vs. Detector Capacitance

voltage-sensitive amplifier

→ given signal charge Qs

$$V_s = \frac{Qs}{C_d + C_i}$$

→ assuming input noise Vn

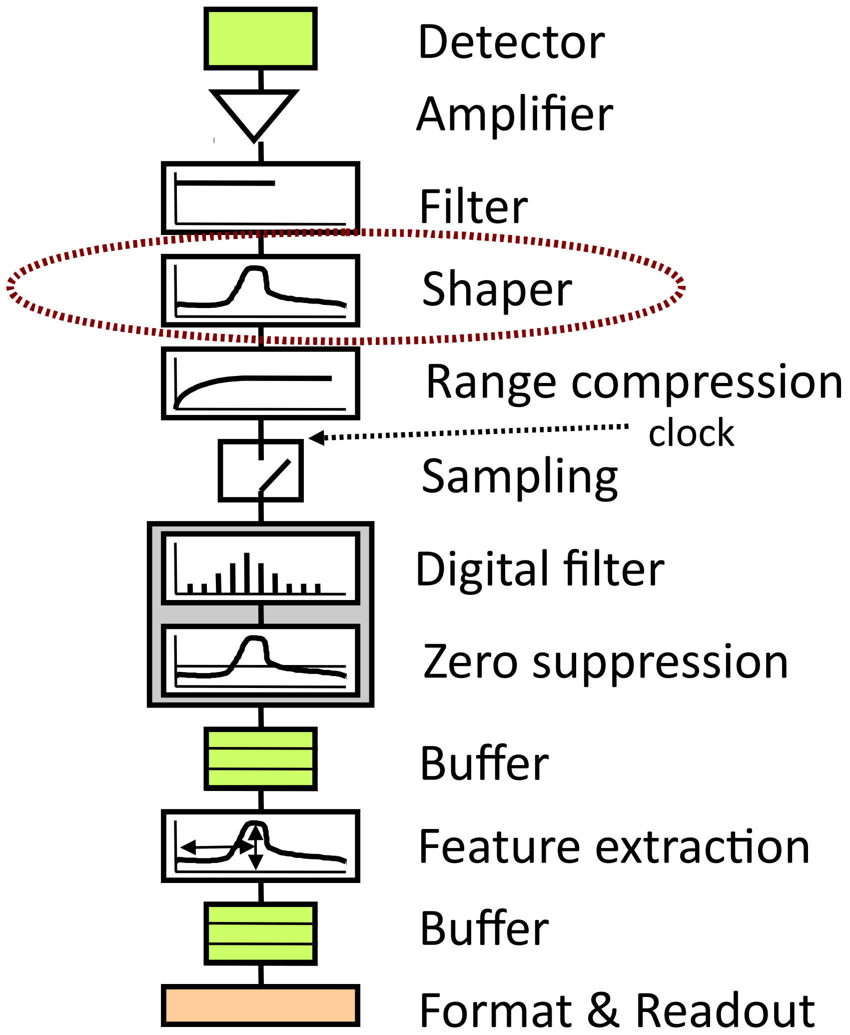


$$\frac{V_s}{V_n} = \frac{Q_s}{V_n(C_d + C_i)}$$

SNR inversely proportional to total input capacitance

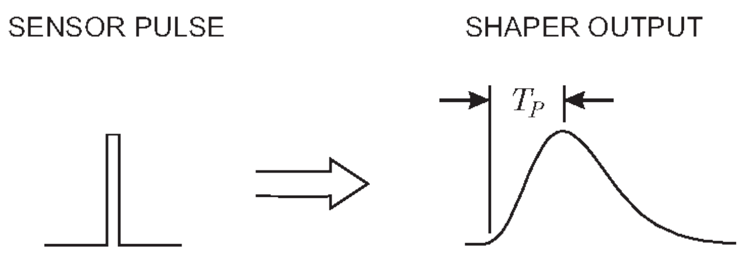
Thick detectors normally provide larger signals **and noise**

Read-Out Chain

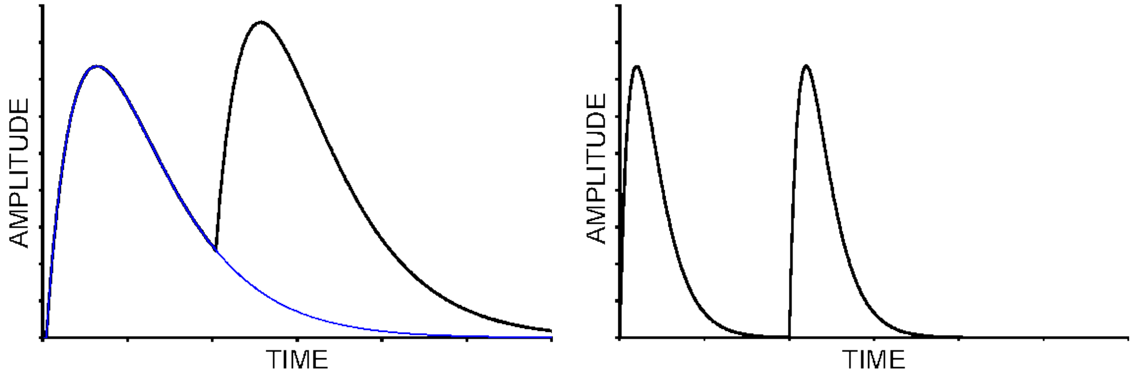


Pulse Shaping

- Reduce signal bandwidth (low-pass filter) → improve SNR
  - fast rising signals have large bandwidth
  - shaper broadens signals

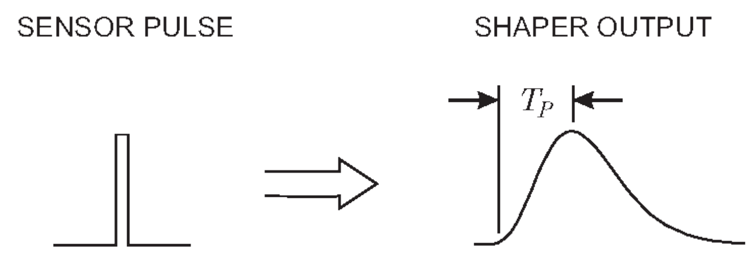


- Limit pulse width (high-pass filter) → avoid overlap of successive pulses
  - increase maximum signal rate at the cost of more noise

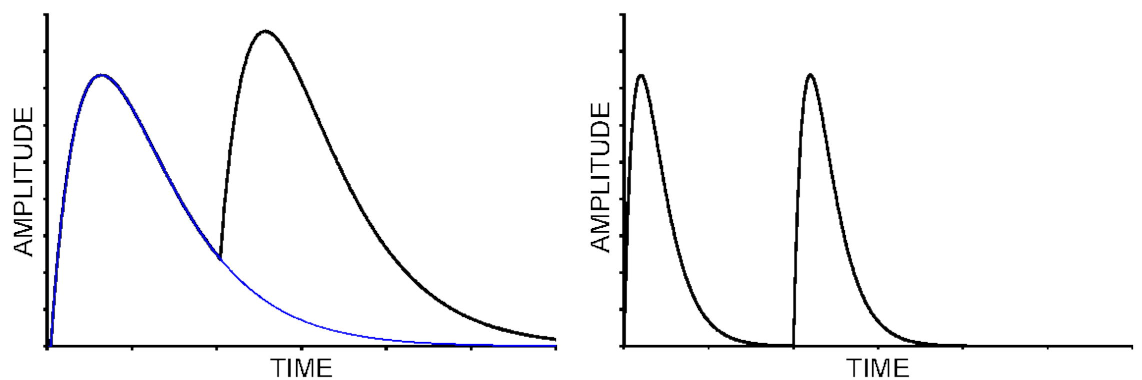


Pulse Shaping

- Reduce signal bandwidth (low-pass filter) → improve SNR
  - fast rising signals have large bandwidth
  - shaper broadens signals



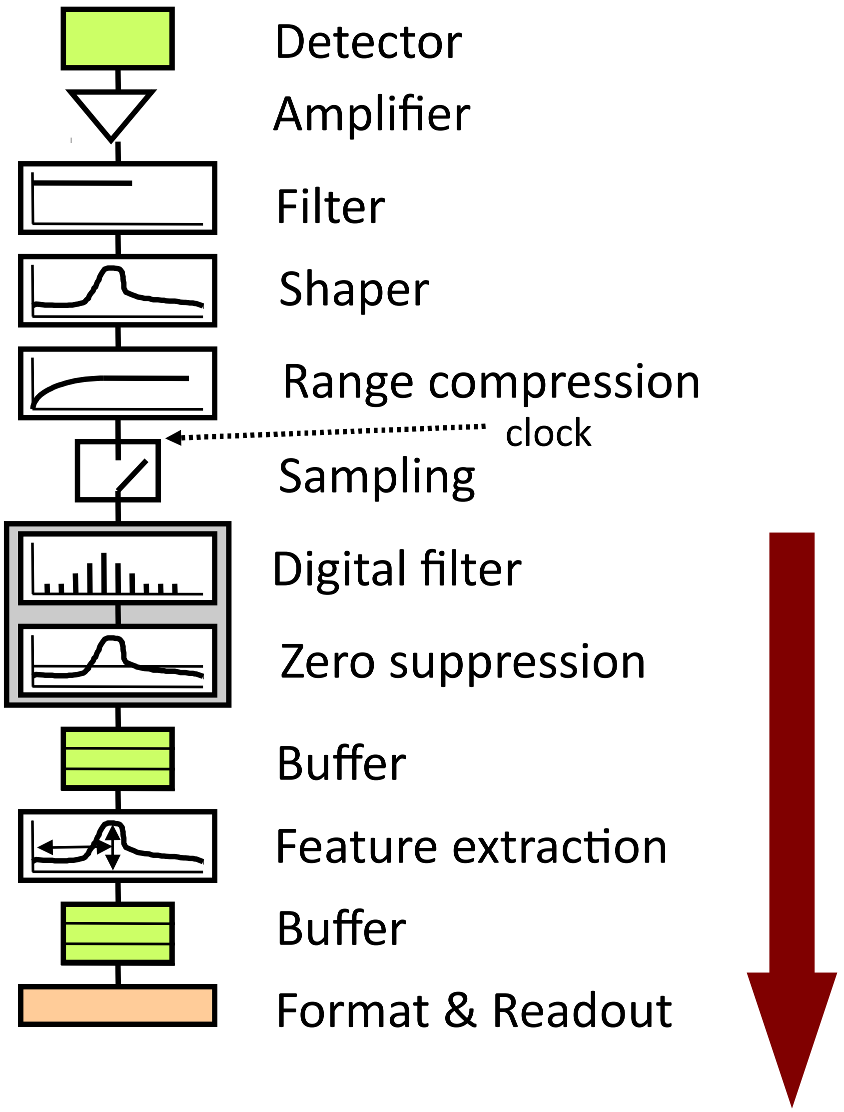
- Limit pulse width (high-pass filter) → avoid overlap of successive pulses
  - increase maximum signal rate at the cost of more noise



Shaping is often a compromise

CR-(RC)^n shaping is often a good compromise

Read-Out Chain



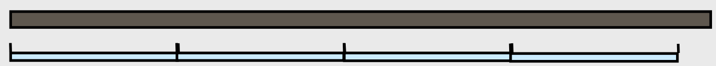
Analog-to-Digital Conversion Introduction

Digitization → encode analog information into a numerical (discrete) format

Why ? Much easier to handle and preserve

Which format ? Usually binary, sometimes BCD

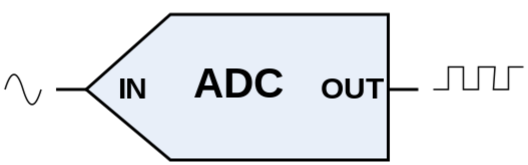
Entity to be measured



Ruler unit

Compare entity (→ count) with a ruler

Electrical Symbol:



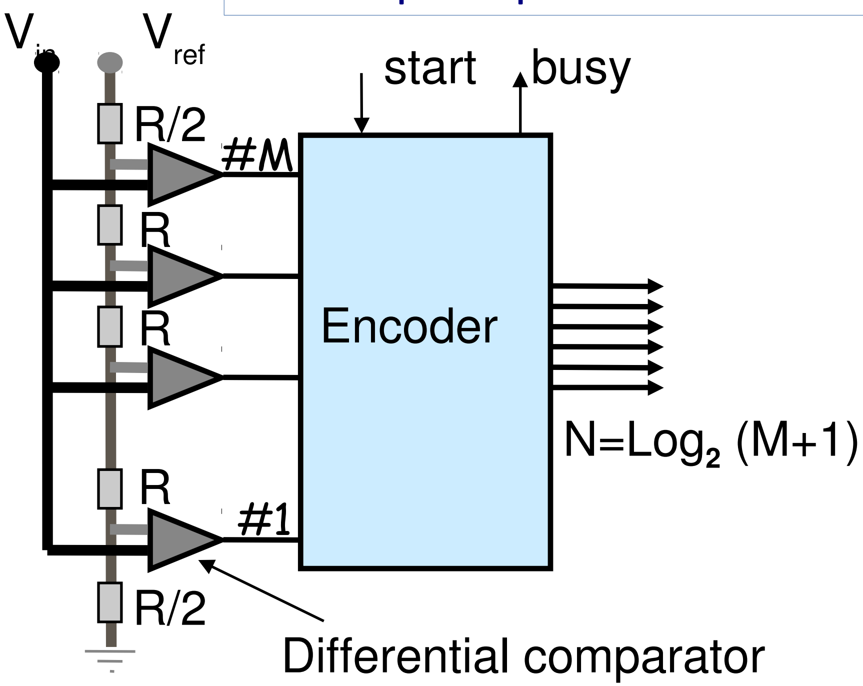
Allow further processing and storage in digital electronics and computers

Flash ADC

- Simplest and fastest implementation
- Performs M comparisons in parallel
  - input V compared with M fractions of a reference voltage:

    $0.5*V_{ref/}/M, 1.5*V_{ref/}/M, \dots (M-0.5)*V_{ref/}/M$

    in step of $V_{ref/}/M$
- Result encoded into compact N-bit binary value
- Sample input at fixed rate and fixed sample depth



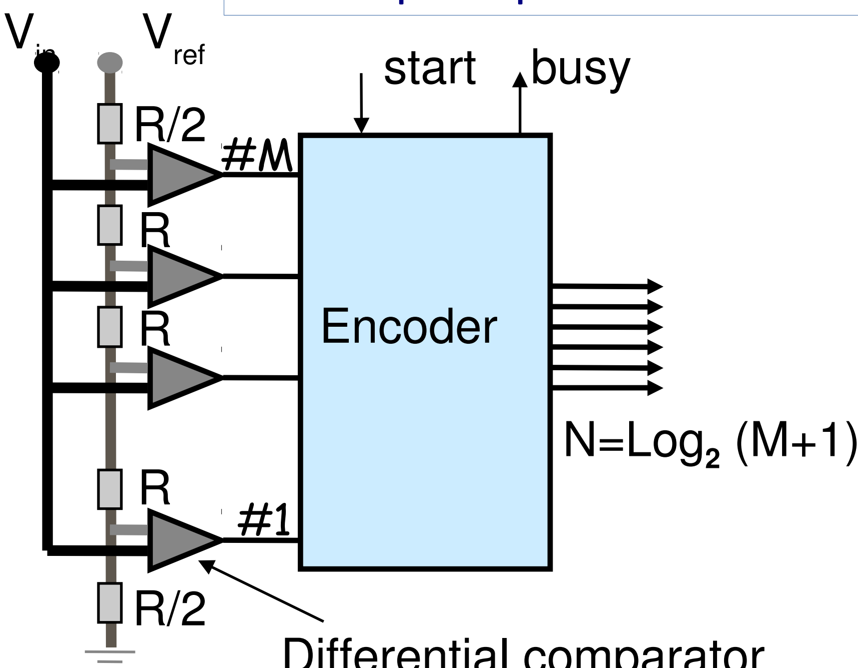
- Simple ? Yes
- Fast ? Yes
- Could be non-linear ? Yes
- Cheap ? Oopss ...

Flash ADC

- Simplest and fastest implementation
- Performs M comparisons in parallel
  - input V compared with M fractions of a reference voltage:

    $0.5*V_{ref/}/M, 1.5*V_{ref/}/M, \ldots (M-0.5)*V_{ref/}/M$

    in step of $V_{ref/}/M$
- Result encoded into compact N-bit binary value
- Sample input at fixed rate and fixed sample depth

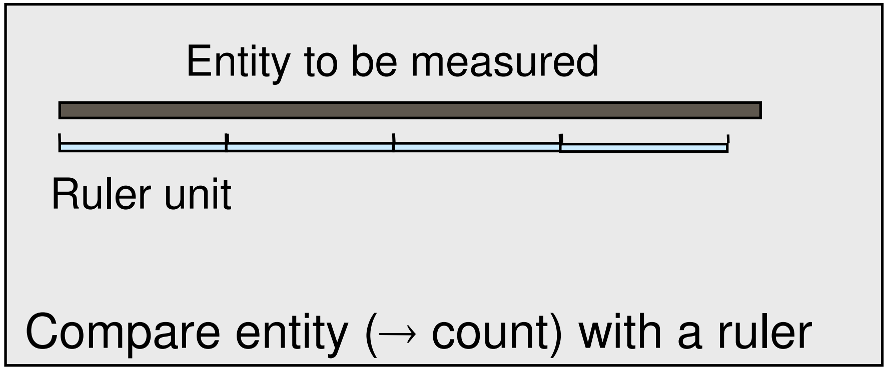


Example M=3 → N=2

V_{in}/V_{ref}	Comparison results	Encoded form
<1/6	000	00
1/6≤ <3/6	001	01
3/6≤ <5/6	011	10
5/6≤	111	11

ADC Characteristics

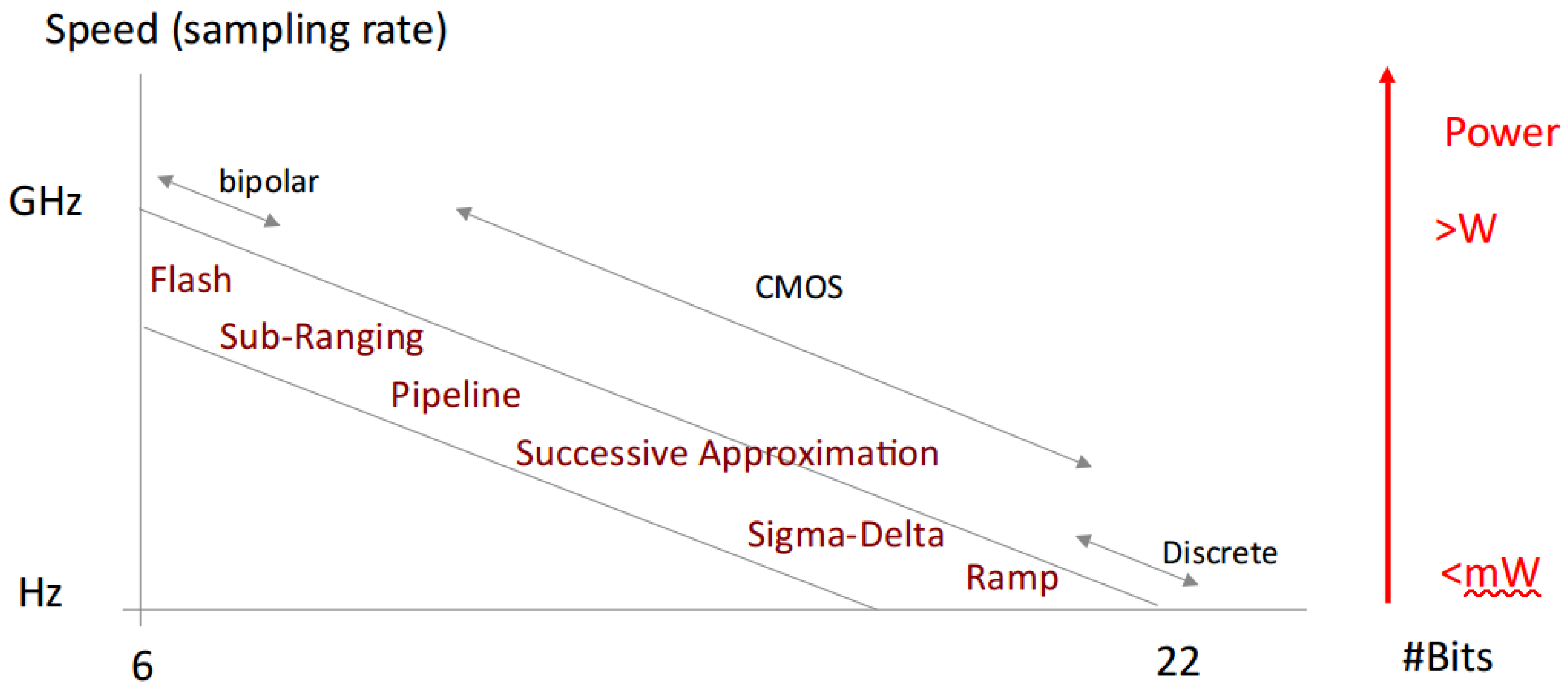
Digitization → encode analog information into a numerical (discrete) format



- Resolution (LSB), the ruler unit: $V_{max}/2^N$
  - 8bit, 1V → LSB=3.9mV
- Quantization error: ±LSB/2
- Dynamic range: V_{max}/LSB
  - N for linear ADC
  - >N for non-linear ADC; if logarithmic:
    constant relative resolution on the valid input range

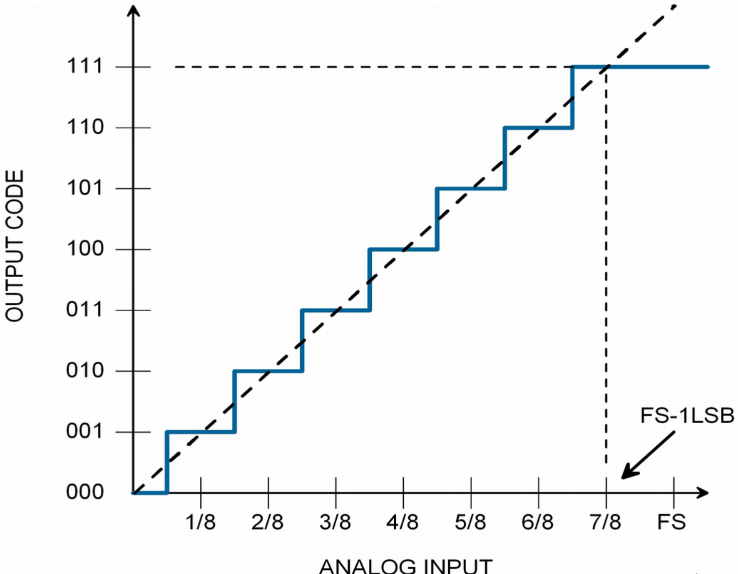
ADC Phase-Space

Many different ADC techniques exist, with different trade-offs between speed, resolution, power consumption, cost, ...

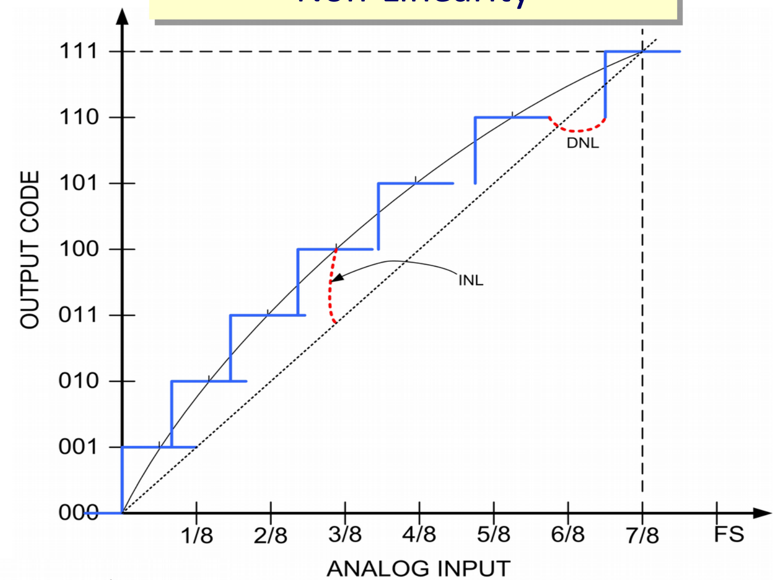


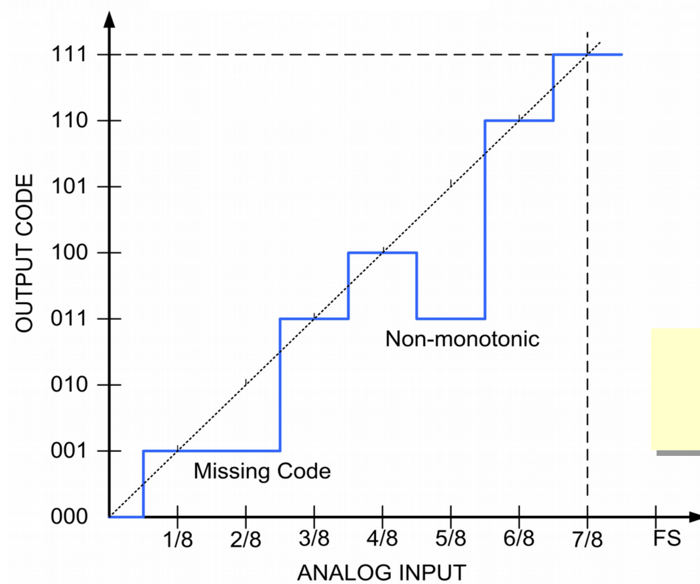
ADC (In)Accuracies

ADC Transfer function



Integral & Differential Non-Linearity

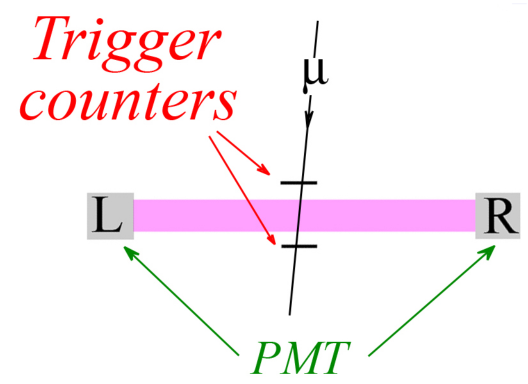


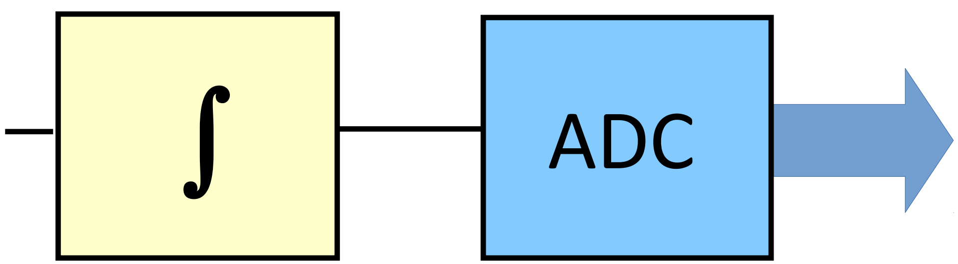


Extreme Differential Non-Linearity

Real ADC.s at Work

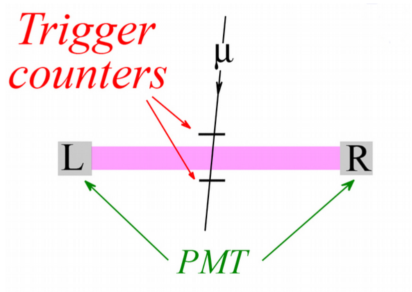
- Real data from a beam test @CERN
- $PbWO_4$ (scintillating) crystal equipped with two PMTs and exposed to e, μ and π beams
- QDC → (gated) charge integrator followed by ADC
  - → (fixed-duration) gate opened after trigger
  - → digital conversion started after gate closing
  - → integrator discharged after conversion

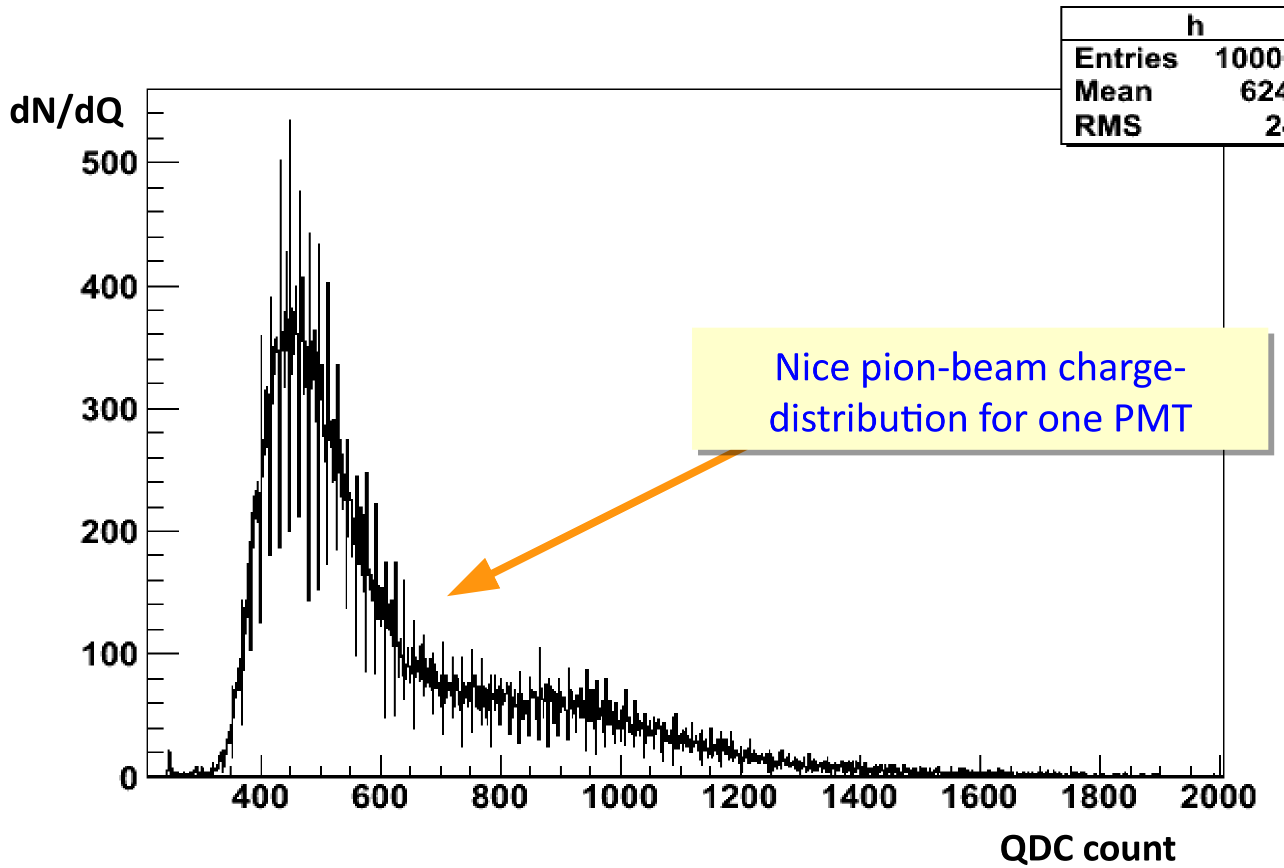




Real QDC.s at Work

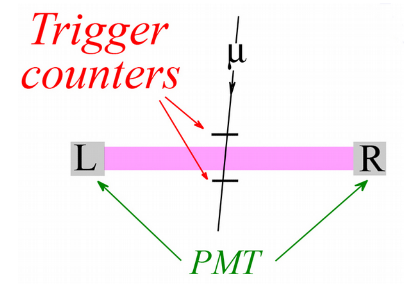
$PbWO_4$ crystal equipped with two PMTs and exposed to e, μ and π beams

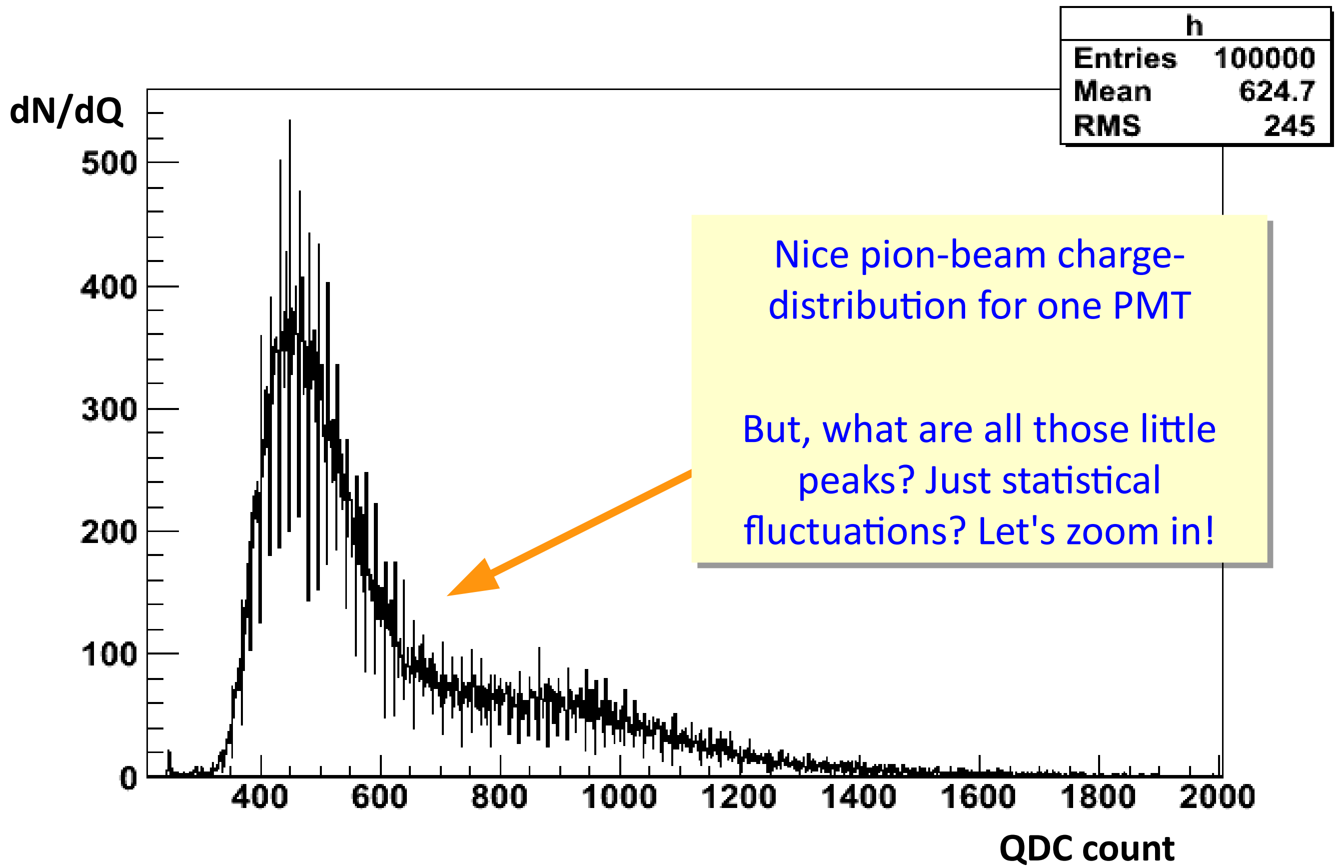




Real QDC.s at Work

$PbWO_4$ crystal equipped with two PMTs and exposed to e, μ and π beams

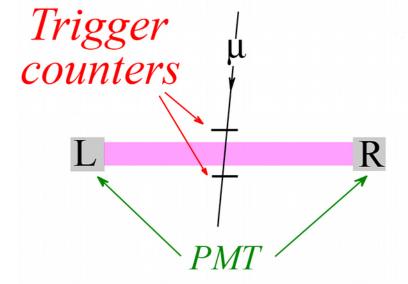


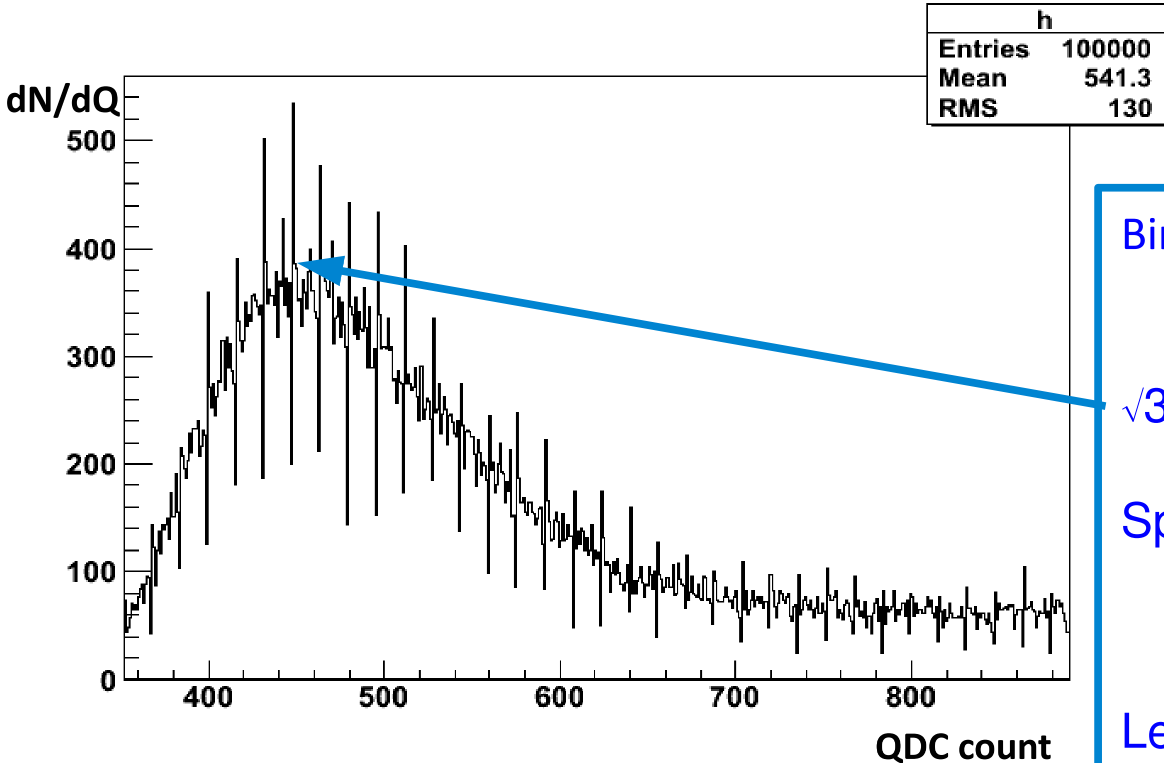


Nice pion-beam charge-distribution for one PMT

But, what are all those little peaks? Just statistical fluctuations? Let's zoom in!

Real QDC.s at Work





Bin with N entries shall fluctuate with:

- σ=√N

√360~19 → (540-360)/19~10

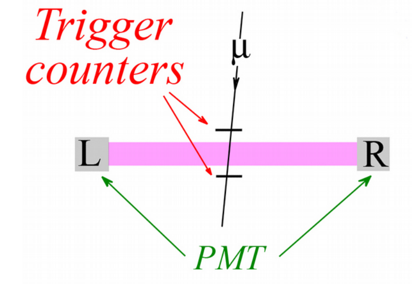
Spikes are regularly distributed

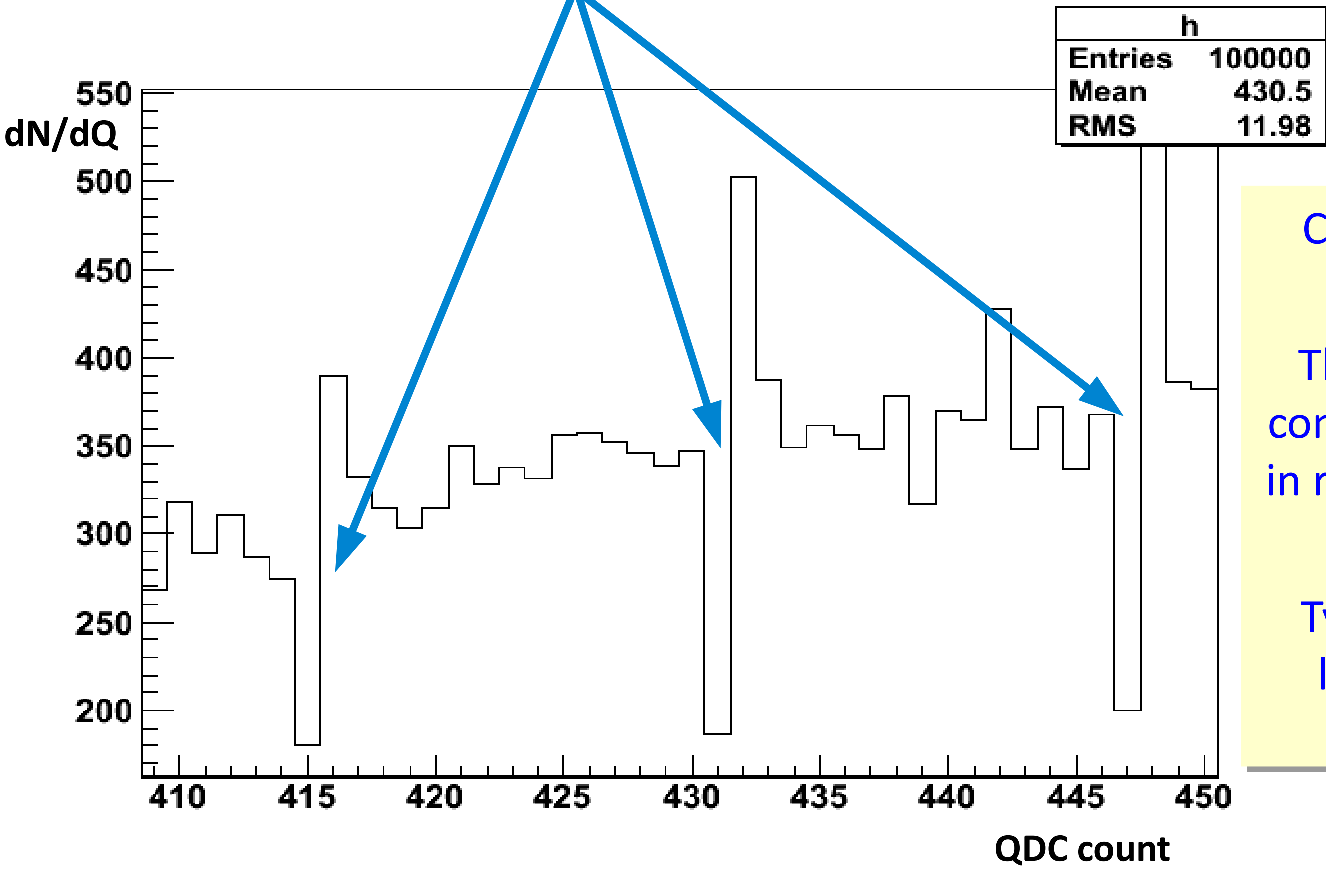
- some systematic effect is taking place

Let zoom in a bit more!

Real QDC.s at Work

415 & 416 → 0x19f & 0x1a0
431 & 432 → 0x1af & 0x1b0
447 & 448 → 0x1bf & 0x1c0





Can you see the effect?

The QDC prefers output configurations of type *xxx*0 in respect of those like *xxxf*

Typical differential non-linearity of successive approximation ADCs

Homework: can you find a simple way to fix this problem in the data? What the cost?

Some more … Peak-Sensing ADC

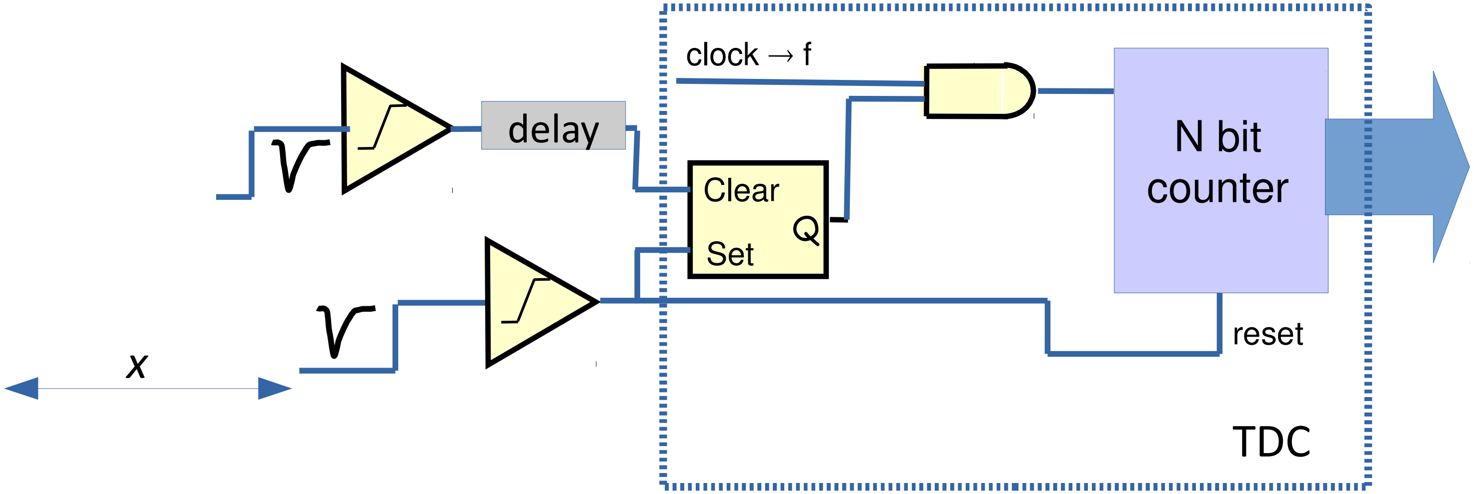
- QDC signals need to be fully integrated, gate need not to be too long

  → need precise and stable timing .vs. gate:
- high-rate unipolar pulses may suffer of baseline drift

→ to overcome such problems:

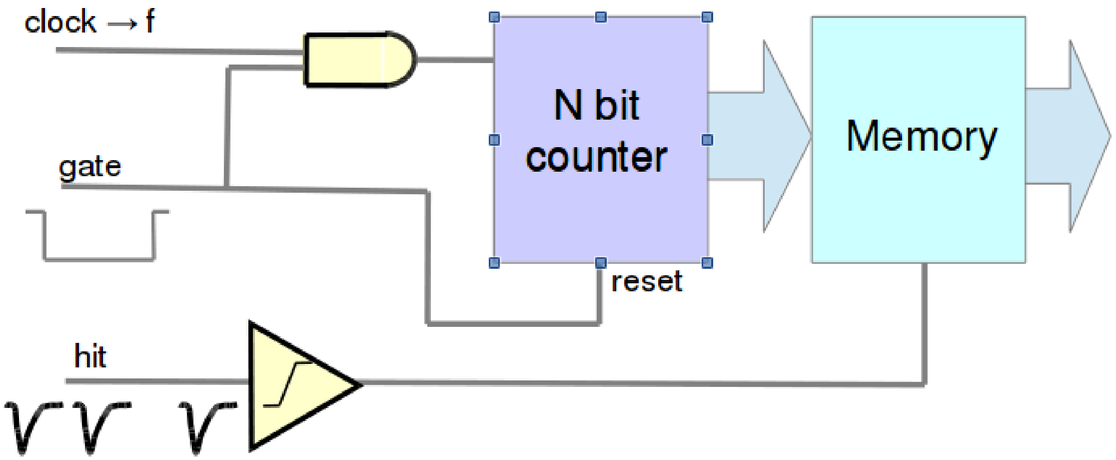
1) charge amplifier + shaper:
   - signal shape stable
   - peak value proportional to Q
2) peak-sensing ADC:
   - find Vmax within a gate (rise-time shouldn't be too fast)
   - at end-of-gate, convert

Time Measurements → TDC



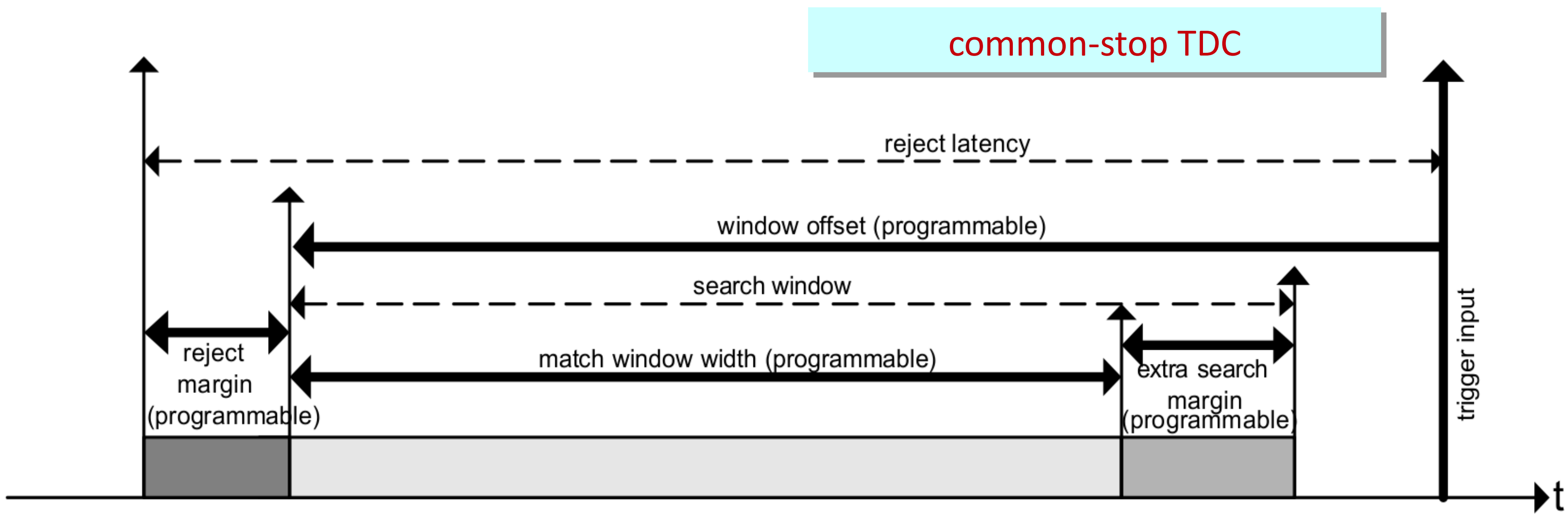
- Time-to-Digital Converter
- Resolution: 1/*f*
- Dynamic range: N
- Single-hit TDC:
  - e.g. noise spike arriving just before the signal → measure lost

Multi-Hit TDC



- Gate resets and starts counter. Also provides measurement period
- Gate duration <~ $2^N/f$
- Each “hit” (i.e. signal) forces memory (FIFO) to load current counter value, that's delay wrt. gate opening
  - in order to distinguish hits belonging to different gates, some additional logic needed to tag data (end/start-of-gate marker)
- Common-start configuration

Real TDC.s



- Real TDCs provide advanced functionalities for fine-tuning hit-trigger matching
  - internal programmable delays
  - internal generation of programmable gates
  - programmable rejection frames

Digital Converters – Summary

Speaking about measuring fast (short) pulses ...

- Flash ADC: high-speed sampling, measure V
- QDC: pulse integration, measure Q, pedestal* proportional to gate length
- Peak Sensing ADC: measure V(peak)
- TDC: measure time intervals

- conversion (dead) time of commercial VME boards $\sim$ few us

*pedestal = measurement of input noise (absence of signal) to be continued...