xTCA IG Meeting - CERN

RECENT DEVELOPMENTS CONCERNING IPMI IN THE ATLAS-TILECAL UPGRADE

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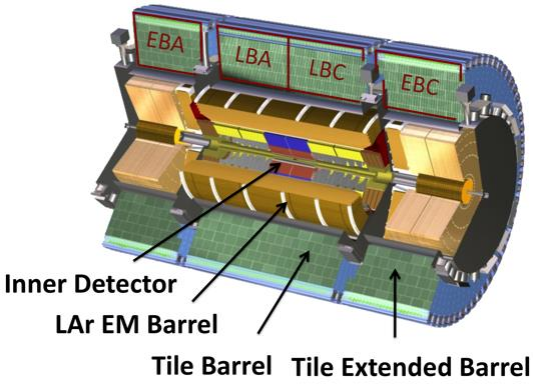
On behalf of the ATLAS Tile Calorimeter Group

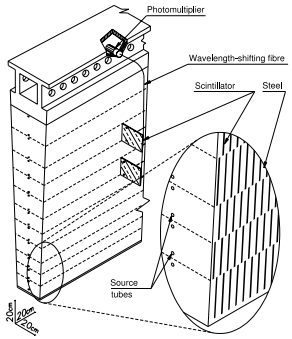
Outline

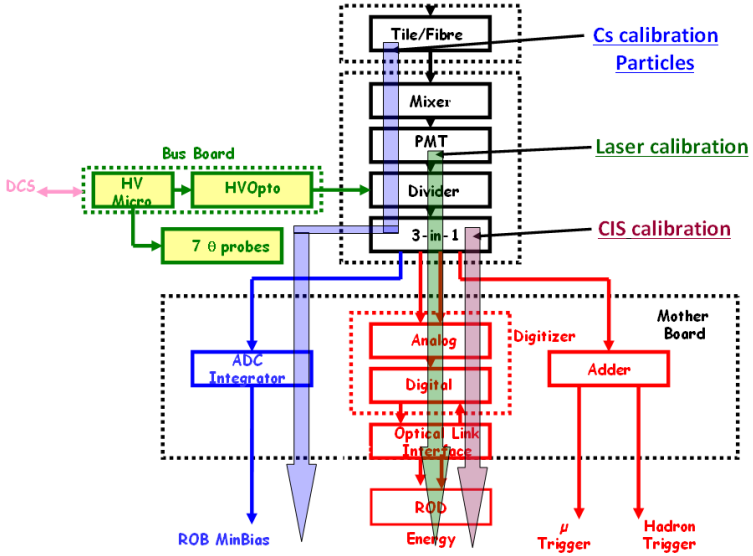
- ATLAS Tile Calorimeter
- Phase II Upgrade
- Tile Demonstrator Project
  - Back-end electronics
  - PPR Prototype
  - ATCA platform test-bench at IFIC (Valencia)
- IPMI-PICMG HW Management in the PPR prototype
- IFIC's ATCA HW Management Software Tool
- Next steps @IFIC for the ATLAS-TileCal upgrade R&D
- Summary

ATLAS Tile Calorimeter

- Segmented calorimeter made of steel plates and plastic scintillator which covers the most central region of the ATLAS experiment
  - Divided in 4 partitions: each one has 64 modules
    - One drawer hosts up to 48 Photo Multiplier Tubes (PMTs)
  - The front-end electronics digitize and store the signals coming from PMTs upon the reception of a Level-1 trigger accept, when they are transferred to the Read-Out Drivers (ROD) in the back-end electronics
  - More than 10,000 readout channels

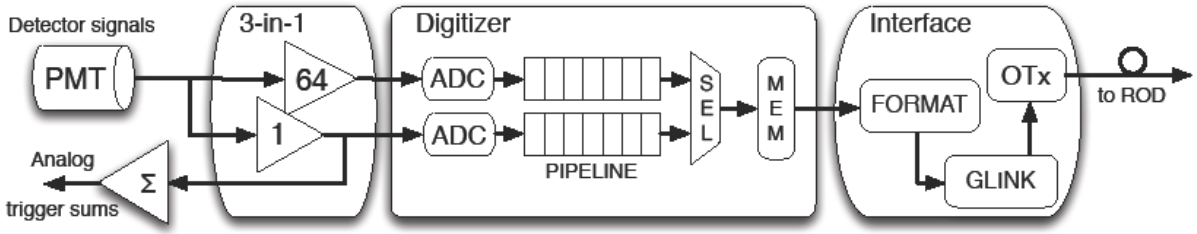




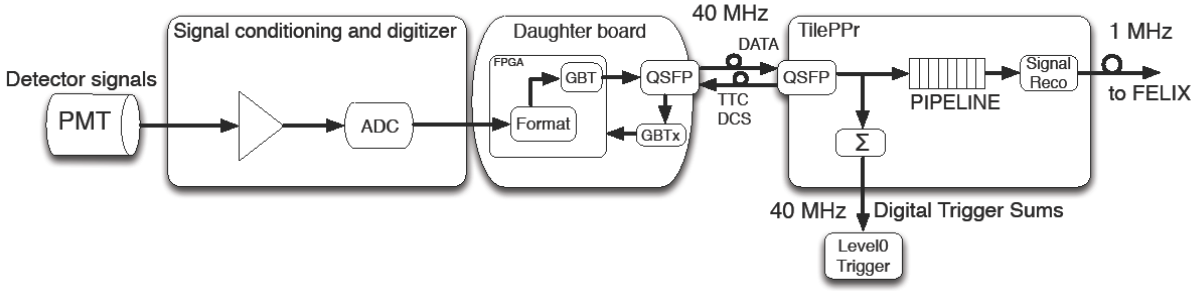


Tile Calorimeter Phase II Upgrade

- Large Hadron Collider plans to increase the instantaneous luminosity by a factor 7 around 2024 (High Luminosity LHC)
- Complete redesign of front-end (FE) and back-end (BE) electronics
  - Full **digital** Level-1 trigger
  - Higher reliability and robustness, higher radiation tolerance
    - Full redundant readout data links
    - Increased modularity in front-end and redundant low voltage power supplies



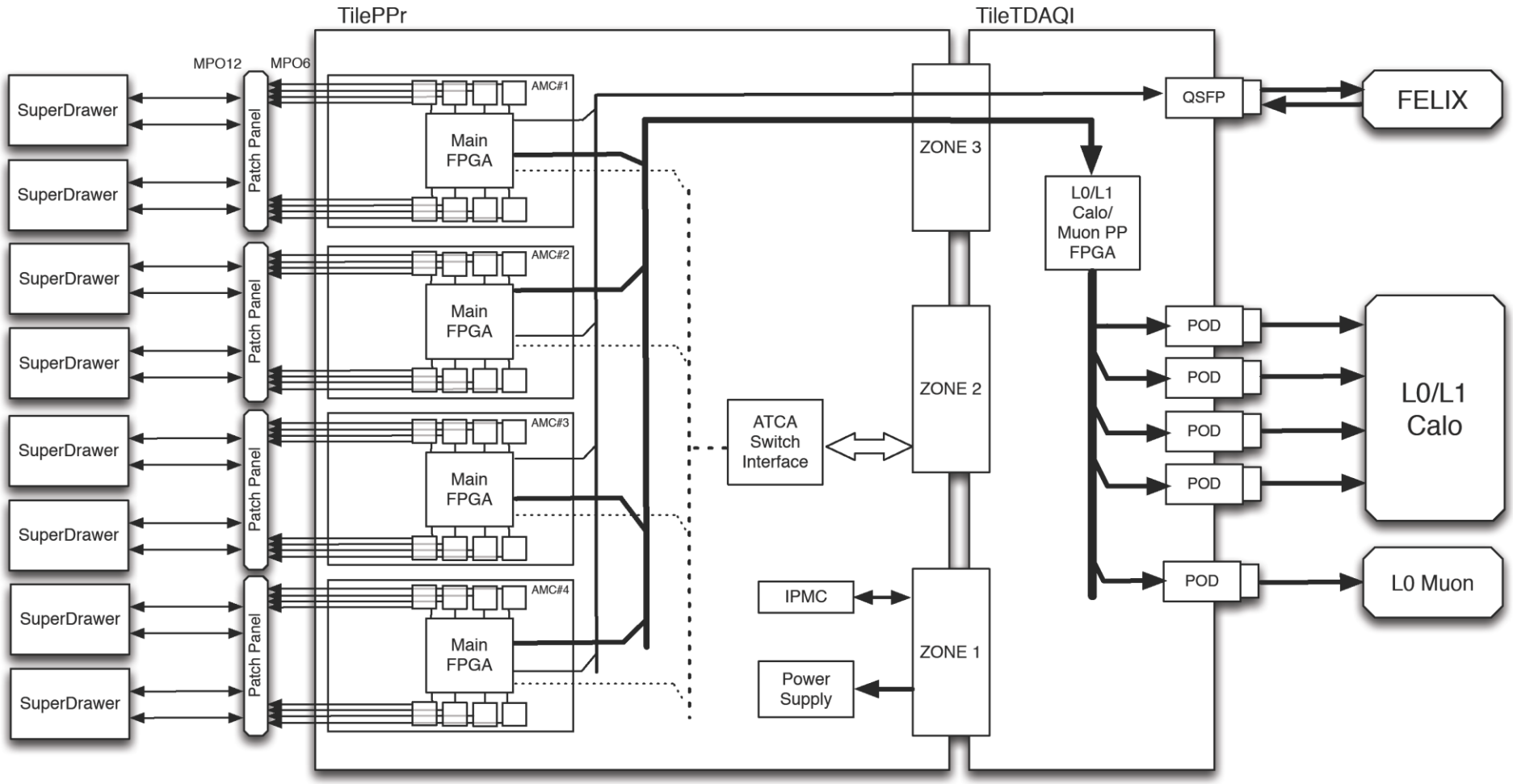
Current architecture



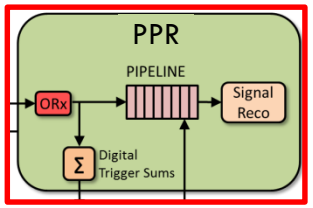
New architecture

	Present	Phase II
Total BW	~165 Gbps	**~40 Tbps (+40 Tbps)**
N. fibers	256	**4096 (+4096)**
BW/drawer	640 Mbps	**160 Gbps (+160 Gbps)**

Tile Calorimeter Phase II Upgrade



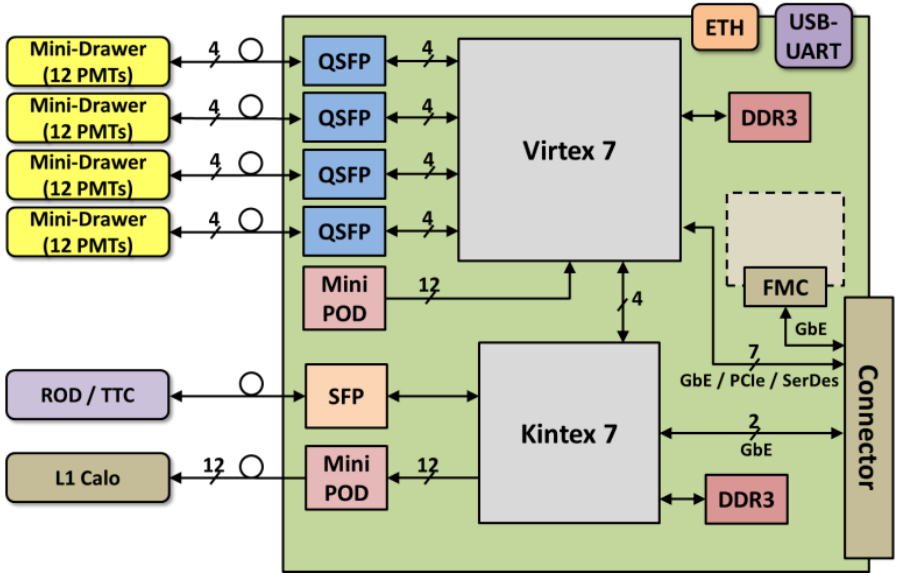
Back-End Electronics



- PrePRocessor prototype (IFIC-Valencia)
- *High speed interface with the front-end electronics*
  - Readout data coming from the detector
    - 4 Mini-Drawers
    - Up to 48 PMTs
  - Timing Trigger and Control (TTC) distribution to the FE
    - Clock distribution for synchronization
    - Control and configuration commands

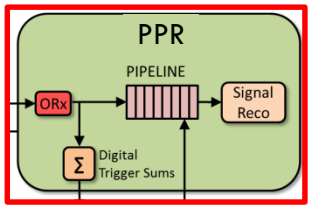
BW: 4 x 40 Gbps

- Real time data processing
  - Reconstruction algorithms: energy, time and quality factor
- Communication with the Level-1 Trigger system
  - Sending preprocessed data for L1 trigger decision
- Keeps backward compatibility with the present DAQ system



Schema of the PPR prototype

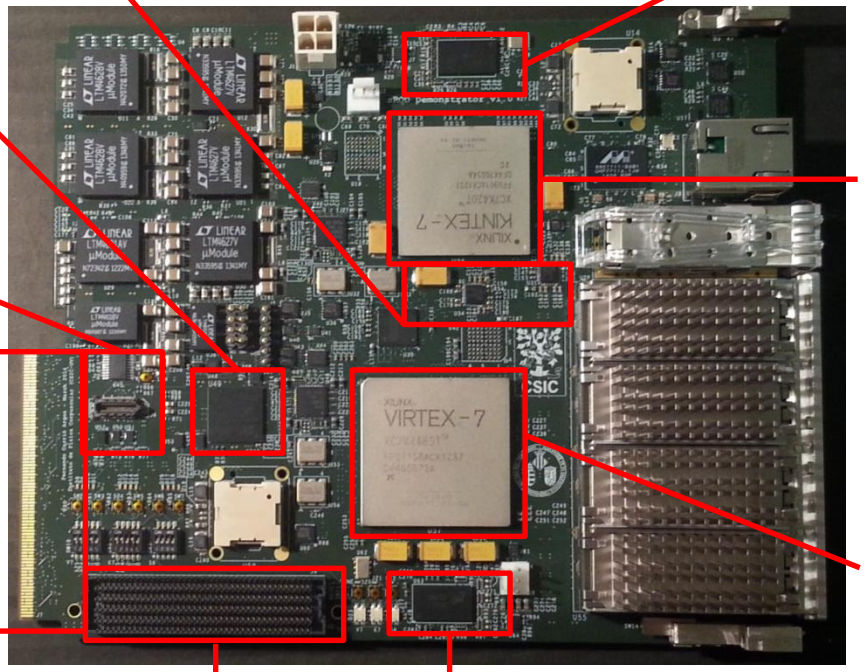
PPR prototype



Xilinx Spartan 6
- Slow control capabilities (Clock management)
- Read back status of the system(IPMI port)

2 x CDR IC
- ADN2814
- Clock/data from TTC

DDR3 512MB



Xilinx Kintex 7 FPGA
- XC7K420T
- 28 GTX transceiver @ 10 Gbps
- Data preprocessing
- Communication with Level 1 trigger system

Module Management Controller (MMC)
- Power connection management
- IPMI protocol

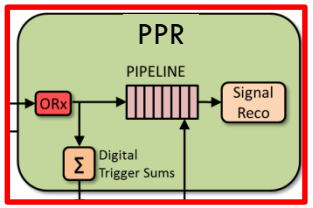
Xilinx Virtex 7 FPGA
- XC7VX485T
- 48 GTX transceiver @ 10 Gbps
- Communication with FE electronics
- Data processing

AMC connector
- 12 V power connection
- Slow control path
- High-speed communication path with the carrier board / µTCA crate (GbE, PCIE, custom protocols)

FMC connector
- Expansion funcionalities: ADC boards, test boards, ...

DDR3 512MB

PPR prototype



TOP
BOTTOM

Power Modules
- Linear Technologies
- Low noise

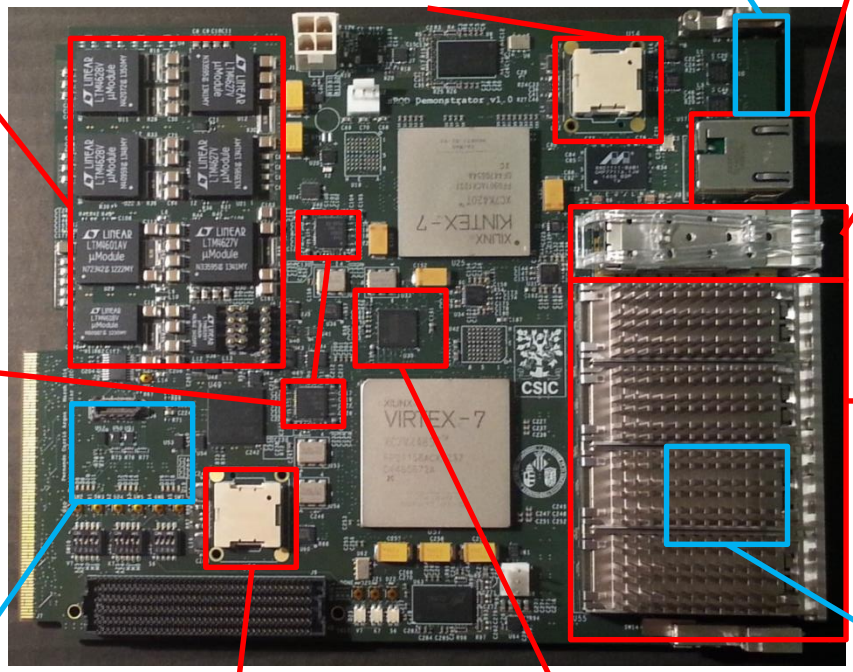
Jitter cleaners
- TI CDCE62005
- Low jitter (< 1ps)
- Clean recovery clocks for GTX
- Unify clock domains

Power supervisory IC
- LT LTC2977
- Power sequencing
- Protection
- Current, voltage, temp.

MiniPOD TX
- 12 x 10 Gbps
- L1 trigger communication

UART-USB ports

Ethernet port
- 10/100/1000 Mpbs
- PC communication



SFP module
- TTC reception
- Communication with current DAQ system

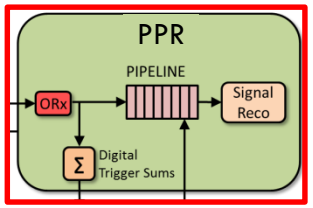
4 x QSFP modules
- FE communication
- Each module at 40 Gbps
- Total max. BW: 160 Gbps

MiniPOD RX
- 12 x 10 Gbps
- Test purposes

Clock generator
- LMK03806B
- 10 diff outputs
- Low jitter

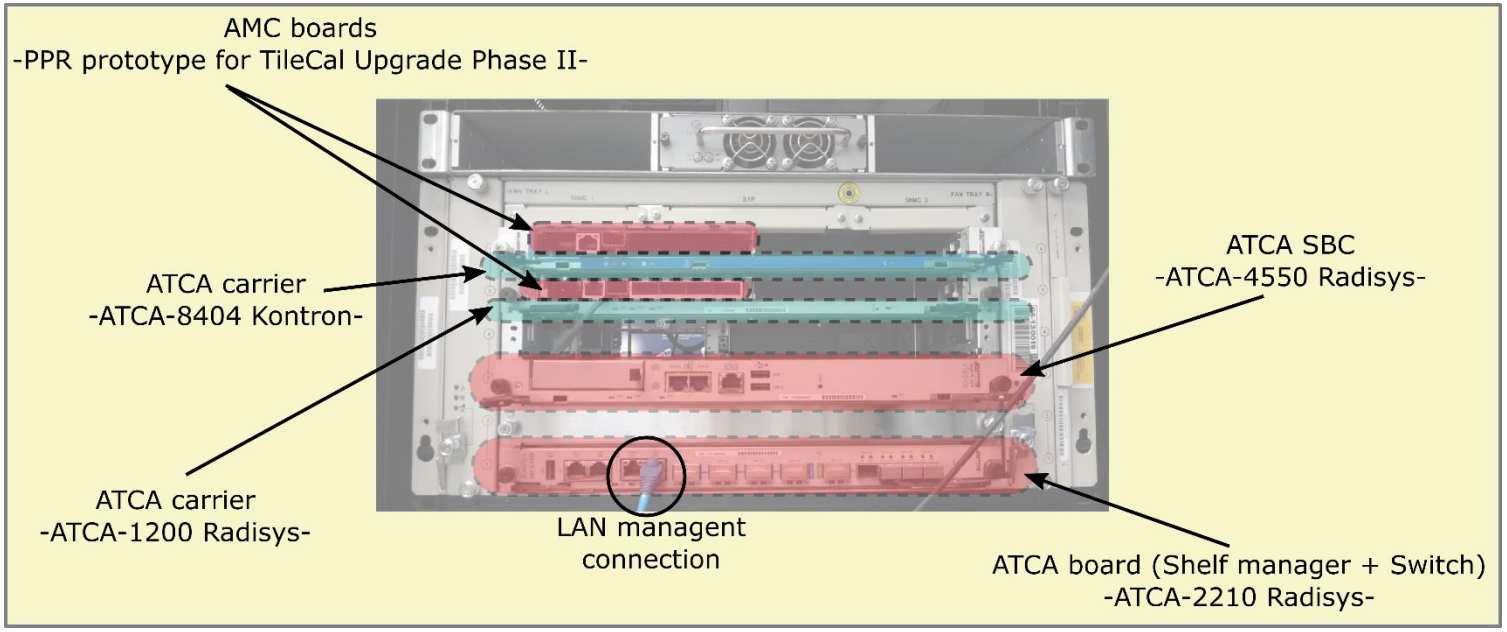
JTAG programmer

ATCA platform test-bench at IFIC (Valencia)



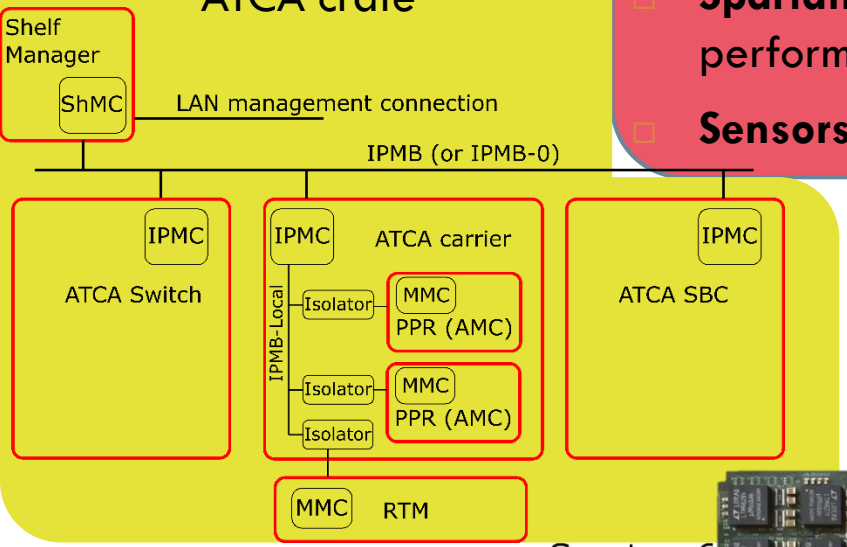
- Adopted by ATLAS as VME replacement
- Double mid-size AMC form factor
  - 180.6 mm x 148.5 mm
  - µTCA crates/ATCA carrier boards + ATCA crate

- Complete ATCA test-bench
  - ELMA chassis
  - ATCA 4550 Single Board Computer (SBC)
  - ATCA-1200 carrier (Radisys)
  - ATCA-8404 carrier (Kontron)
  - ATCA-2210 board (Shelf manager + Switch)



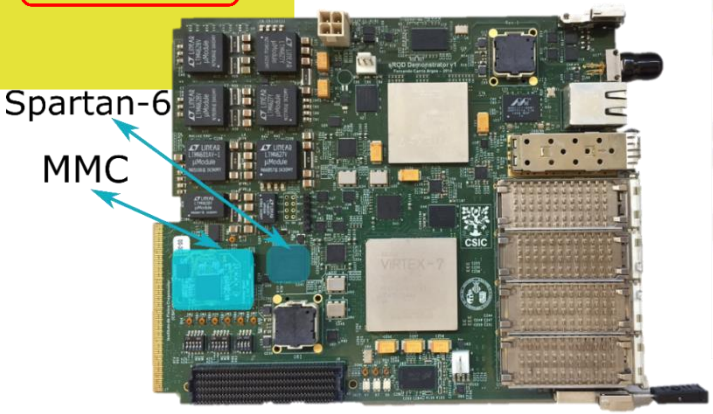
IPMI-PICMG HW Management in the PPR prototype

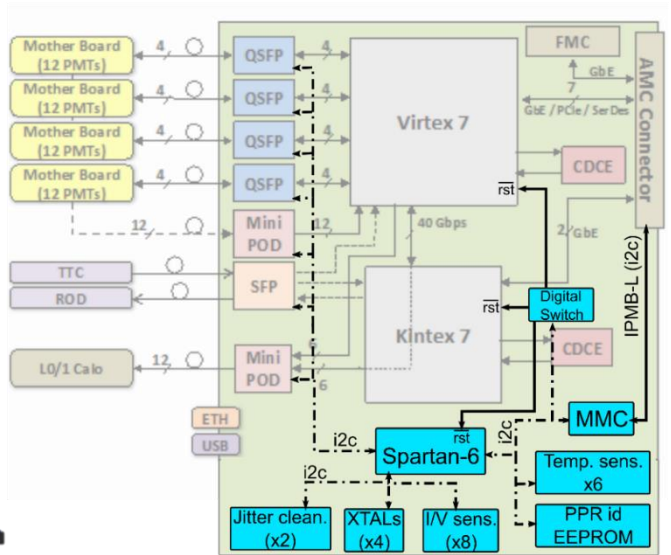
General scheme of the HW Management Infrastructure of an ATCA crate



IPMI-PICMG HW mgmt. inside the PPR prototype:

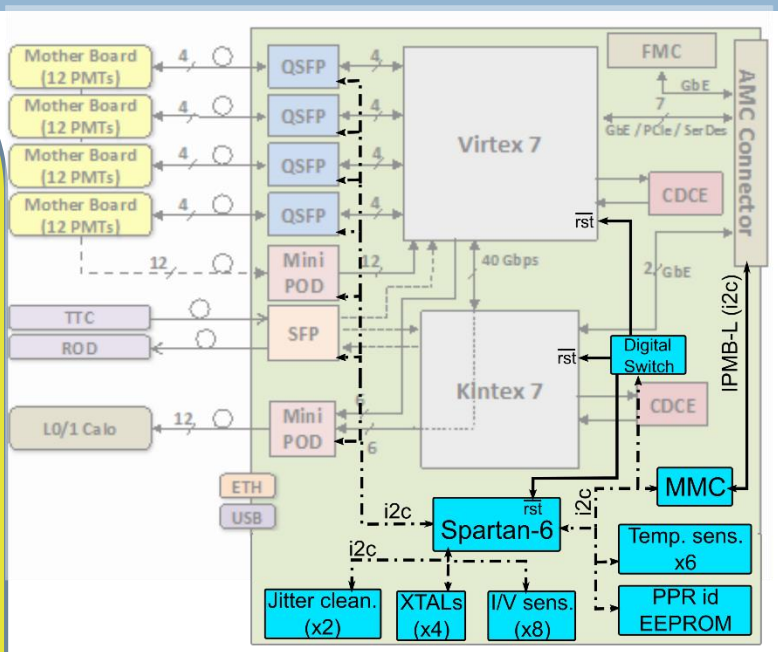
- **MMC**: collects the sensor readings and delivers them to the carrier's IPMC via the IPMB-L.
- **Spartan-6 FPGA**: assists the MMC reading sensors values, and performs other tasks, such as initialization of the PPR's XTALs.
- **Sensors**: (details in next slide).

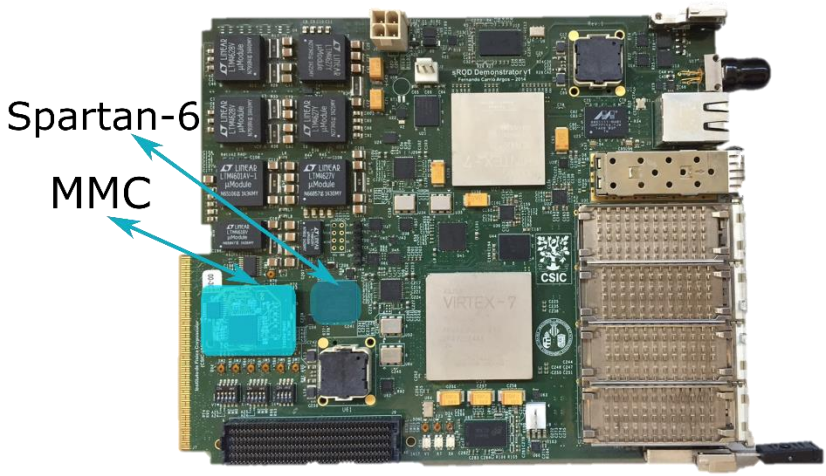




IPMI-PICMG HW Management in the PPR prototype

Device	N.devices x N.registers per device
Supply voltage	8x1 (sensor, r)
Supply Current	8x1 (sensor, r)
QSFP (link on/off state)	(4x4) links x1 (control, r/w)
QSFP (link optic. pwr)	(4x4) links x1 (sensor, r)
SFP (on/off state)	1x1 (control, r/w)
SFP (optical power)	1x1 (sensor, r)
MiniPOD (on/off state)	2x12 (control, r/w)
MiniPOD (optical power)	2x12 (sensor, r)
Temperature Sensor	6x1(sensor, r)
XTALs config.registers	4x4 (control, r/w)
Jitter cleaners	2x2 (control, r/w)
FPGAs remote reset	3x1 (control, w)
TOTAL OF 'read' BYTES	125
TOTAL OF 'write' BYTES	65





IFIC's ATCA HW Management Software Tool

- 1st version: Qt-C++ GUI based on OpenIPMI libraries.
  - *"An IPMI-compliant control system for the ATLAS TileCal Phase-II Upgrade PreProcessor module", P. Zuccarello et al., IEEE NSS-2016.*
- 2nd version: IFIC's own set of C++ functions
  - Goals in mind:
    - To have more control and in-depth knowledge about the HW management IPMI-PICMG messages/commands being issued.
    - To have more control on the HW management communication with the PPR.
  - Two threads:
    - 1: UDP socket to tx/rx IPMI-PICMG hw management messages/commands
    - 2: Qt-C++ GUI and other tasks such as tx buffer data preparation, mysql db connection, etc.
  - Incorporates connectivity with mysql data-base to register sensor values during experiments such as testbeams

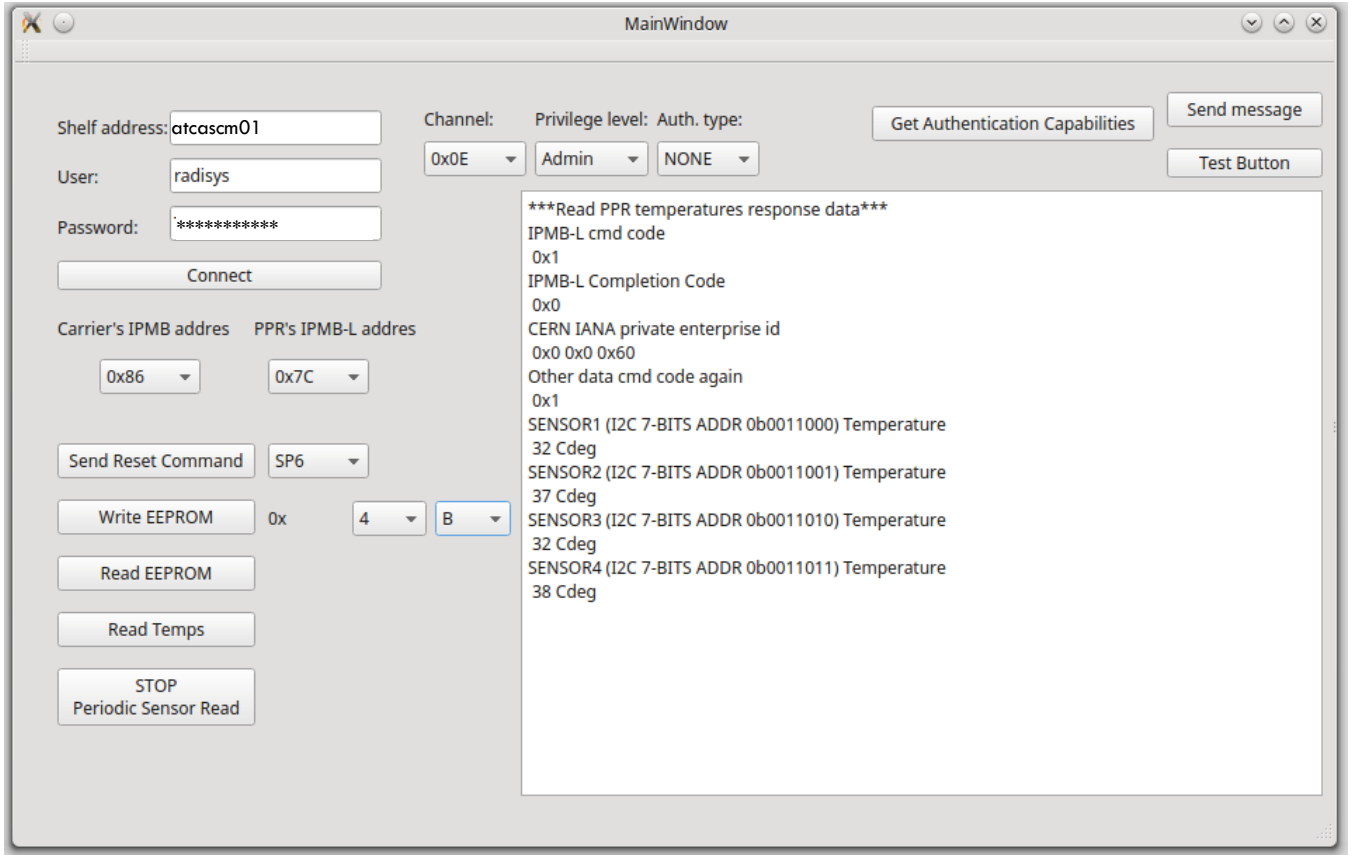
IFIC's ATCA HW Management Software Tool

- UDP tx/rx thread
  - Based on POSIX pthread. Communication with the ATCA crate is done via LAN management connector in the crate.
  - *run* threaded loop based on *sendto*, *select* (non-blocking), *recvfrom*
  - Decodes rx buffers (RMCP header, IPMI header and data)
- GUI thread
  - Qt-C++ GUI
  - Prepares data buffers (RMCP header, IPMI header and data) for tx
  - Handles the tx message queue
  - Handles the connection with the mysql-db
- Communication between threads
  - Qt signals/slots functionality using *emit* function.

IFIC's ATCA HW Management Software Tool

- Currently implemented features:
  - IPMI session activation
    - Get Channel Authentication Capabilities, Get Session Challenge, Activate Session IPMI commands (IPMI-v1.5-Rev.1.1)
  - Explicit message bridging
    - IPMI commands delivered to PPR's MMC via IPMB-L using Send Message Command (PICMG AMC.0 Spec. Rev.2.0, Sect.3.13).
  - PPR HW management commands for sensor reading and configuration are implemented using IPMI OEM Network Function codes (0x2E/2F) under CERN's IANA code (0x000060).

IFIC's ATCA HW Management Software Tool



Next steps @IFIC for the ATLAS-TileCal upgrade R&D

- Next steps in the **Back-end HW design:**
  - Final version of the PPR
  - **Design of an in-house ATCA-carrier to hold the PPRs**
- Next steps for the **ATCA HW Management Software Tool:**
  - Implement more IPMI-PICMG commands
  - Implement IPMI Event reading
  - Read all the sensors connected to the Spartan-6 of the PPR prototype (under development).
  - Use it in Sept.2017 testbeam

Summary

- IFIC participation in the R&D tasks for the Tile Calorimeter Phase II Upgrade
  - In-house design of the PPR
    - the central device in the back-end electronics of the upgraded ATLAS-TileCal
    - double-mid size AMC form factor (AMC.0 Rev.2.0 standard)
    - Follows IPMI-PICMG hw management standards
  - **In-house design** of the **ATCA-carrier** to hold the PPRs (**future work-2018**).
  - Hardware management software tool for ATCA crates
    - Uses UDP packets that encapsulates RMCP/IPMI commands.
    - Allows bridged communication, through the IPMC of the ATCA-carrier, with the MMC of the PPR
    - Stores historical sensor values in mysql db: data can be post-processed and analized off-line.