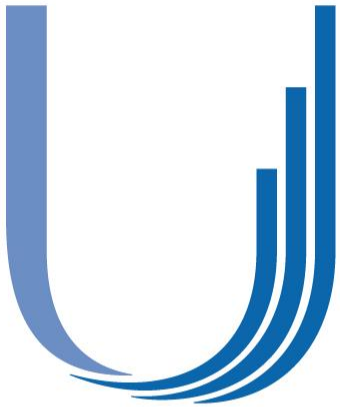


LHC Injectors Upgrade

LHC Injectors Upgrade

uTCA for SPS 200MHz Low Level RF Upgrade

12th xTCA Interest Group Meeting

P. Baudrenghien, **J. Galindo***,
G. Hagmann, G. Kotzian, L. Schmid, A. Spierer
CERN BE-RF

Today's presentation…

-LOW LEVEL RF

-CERN LLRF PLATFORMS

-uTCA @ CERN-BE

-PROOF OF CONCEPT

LOW LEVEL RF

Javier Galindo

uTCA for SPS 200MHz Low Level RF Upgrade

WHAT LOW LEVEL RF MEANS …

-LLRF

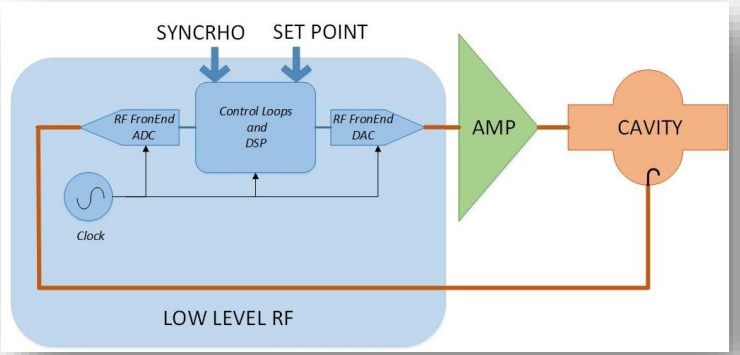
-PLATFORMS

-uTCA @ BE

-uTCA PoC

RF sub-system responsible of

Stable accelerator operation and performance

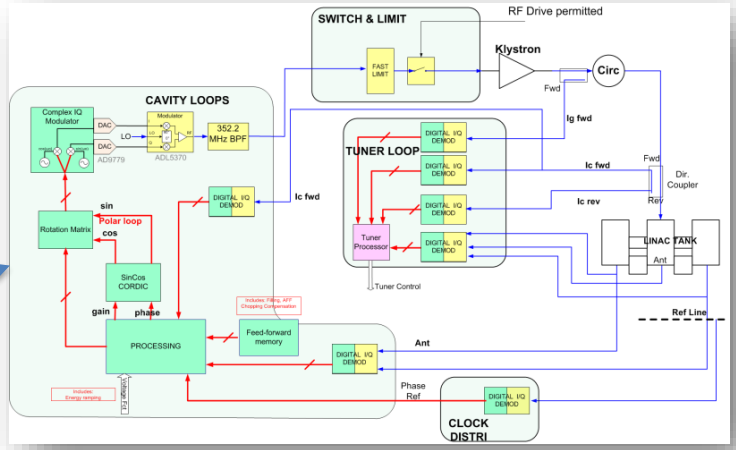


Generation of RF voltages

correct *phase and frequency* in the longitudinal plane

Several controllers

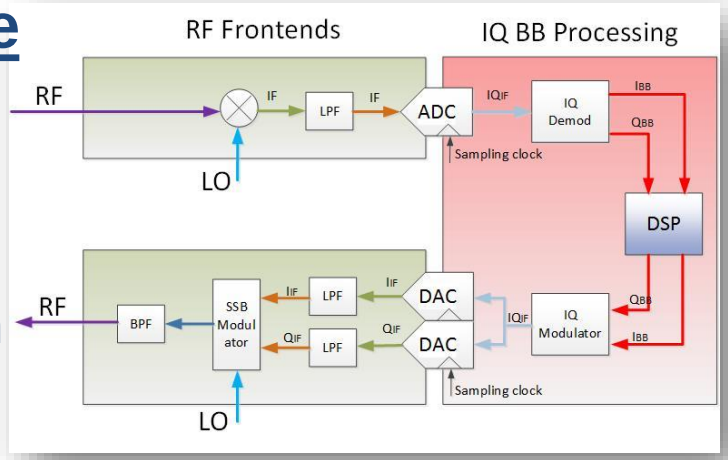
Beam Controllers
Cavity Controllers
Bunch by Bunch Dampers
Synchronization systems



LLRF HARDWARE USUALLY COMPOSES…

Crate or Pizza Box architecture

CERN uses *Crate* architecture



RF Frontends

Clock and *RF* signal generation/distribution

Specific *voltages*

Data observation

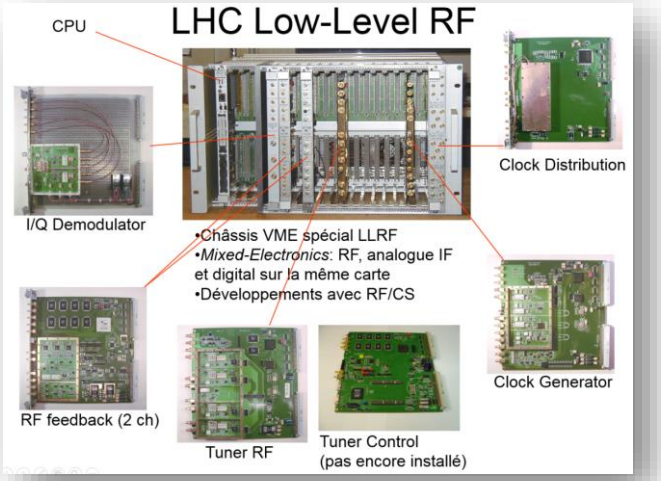
DSP Platform for Control

Feedback / Feedforward Loops

Requires *Synchronization* signals

Latency, bandwidth

Processing power



CERN LLRF PLATFORMS

Javier Galindo

CERN LOW LEVEL RF PLATFORM(S)…

-LLRF

-PLATFORMS

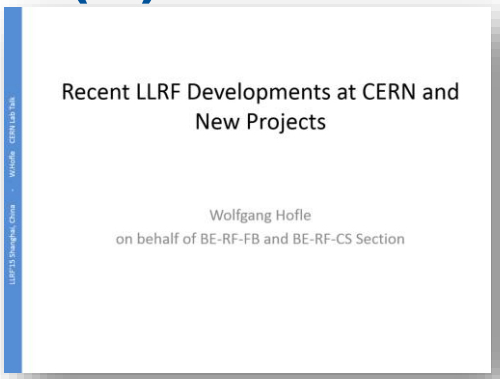
-uTCA @ BE

-uTCA PoC

Past and Present Solutions;

- NIM

  SPS 200 MHz and others)



- VME

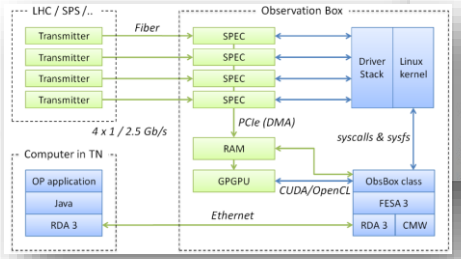
  Linac4, HiIsolde, SPS 800 MHz, LHC long and ADT, part of PS upgrade

- VXS

  PSB, LEIR, ELENA

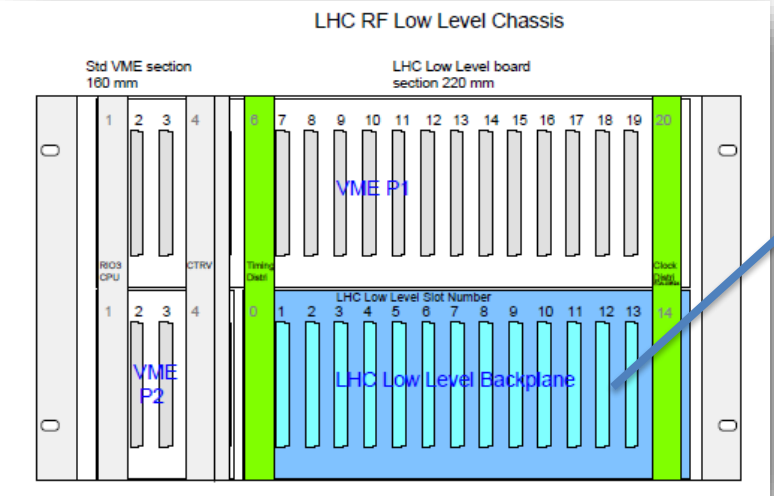
- ObsBox

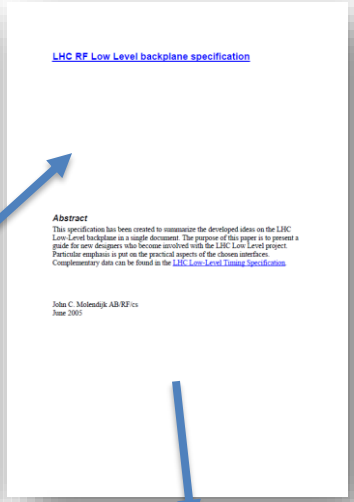
  LHC PizzaBox



LHC LOW LEVEL RF BACKPLANE…

- -LLRF
- **-PLATFORMS**
- -uTCA @ BE
- -uTCA PoC

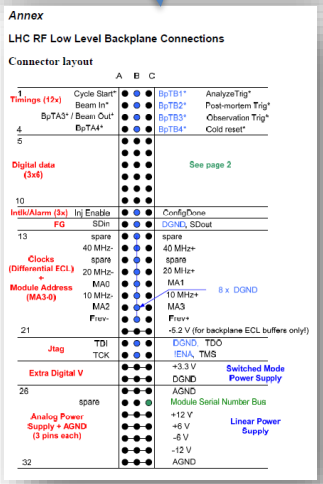



LHC RF Low Level backplane specification

Abstract

This specification has been created to summarize the developed ideas on the LHC Low-Level backplane in a single document. The purpose of this paper is to present a guide for new designers who become involved with the LHC Low Level project. Particular emphasis is put on the practical aspects of the chosen interfaces. Complementary data can be found in the LHC Low-Level Timing Specification.

John C. Molendijk AB/RFcs
June 2005


Annex

LHC RF Low Level Backplane Connections

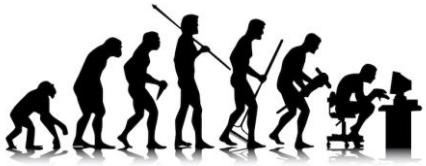
Connector layout

A B C

Timings (12x) — Cycle Start* / Beam In* / BpTA3* / Beam Out* / BpTA4*
BpTB1* AnalyzeTrig* / BpTB2* Post-mortem Trig* / BpTB3* Observation Trig* / BpTB4* Cold reset*
Digital data (3x6) — See page 2
Intlk/Alarm (3x) — Inj Enable
FG — SDin
ConfigDone / DGND, SDout
Clocks (Differential ECL) + Module Address (MA3-0) — spare / 40 MHz- / spare / 20 MHz- / MA0 / 10 MHz- / MA2 / Frev-
spare / 40 MHz+ / spare / 20 MHz+ / MA1 / 10 MHz+ / MA3 / Frev+ (8 x DGND)
-5.2 V (for backplane ECL buffers only!)
Jtag — TDI / TCK
DGND, TDO / IENA, TMS
Extra Digital V — +3.3 V / DGND (Switched Mode Power Supply)
AGND / Module Serial Number Bus / spare
Analog Power Supply + AGND (3 pins each) — +12 V / +6 V / -6 V / -12 V / AGND (Linear Power Supply)

"Power distribution, Clock distribution, Timing distribution, Function Generator Data distribution, Interlocks / Alarms, Inter-module LVDS digital data, Crate Centralized Reconfiguration JTAG, Module Serial Number bus, Automatic Slot Addressing…"

LLRF PLATFORM / BACKPLANE EVOLUTION…



Technical and non technical reason to look for a new platform…

- LLRF mainly based in VME, already a legacy standard
  - Obsolescence problems
  - VME has a low bandwidth
  - Limitation on acquisitions data
  - Limited fast links on the backplane, non standard
  - Limited card to card communication
  - No RF clock distribution on backplane → LLRF backplane
  - All RF custom-designed, no COTS / off-the-shelve modules
  - Power hungry platforms, 6 power supplies, no redundancy

    (5V, 3.3V, ±12V, ±6V)

LLRF PLATFORM / BACKPLANE EVOLUTION…

Technical and non technical reason to look for a new platform…

- Standardization
  - Within CERN; RF, CO, experiments…
  - Other labs DESY, SLAC, ESS…
  - New platforms available uTCA, VPX, PXIe…
  - Commercial solutions available
  - Focus on firmware and not re-designing the same HW again
  - Avoid support to custom systems
  - Collaboration with other people, Open Hardware
  - Re-use of designs, FMC, mezzanines…

uTCA @ CERN-BE

Javier Galindo

uTCA LLRF ONGOING ACTIVITIES @ BE…

Joint effort between BE-CO and BE-RF

BE-CO moving away from VME

(part of CO3 project, BE-CO)

uTCA being evaluated

uTCA4.1 has LLRF flavor

Proof of Concept

in SPS upgrade 200 MHz system

No surprise as much design comes from the Desy Linac RF requirements; off-the-shelf modules

uTCA 4.1 PRELIMINARY WINNER…

Why MTCA.4 and PXIe?

7

After a requirements survey involving BE-CO and the equipment groups (2016), MTCA.4 and PXIe are clear winners:

- Gigabit inter-board communication and timing in the backplane
- Standard means of management and monitoring (AMT, IPMI)
- Both based on PCI Express: simplified driver model
- Support for RTMs and RF applications (MTCA.4)
- Established community at CERN and multitude of hardware vendors (PXIe)
- Significant investment in MTCA.4 (DESY) and growing number of applications (not only in accelerator/physics market)

uTCA PoC JOINT EFFORT @ BE…

-LLRF

-PLATFORMS

-uTCA @ BE

-uTCA PoC

MTCA.4 PoC

Deliverables

BE-CO:

- OS support (drivers, remote management)
- Basic FPGA framework (PCIe, DDR4, DMA)
- White Rabbit support for Kintex Ultrascale FPGA family
- MMC firmware:
  - A microcontroller taking care of management of a MTCA.4 card
  - In collaboration with EP-ESE

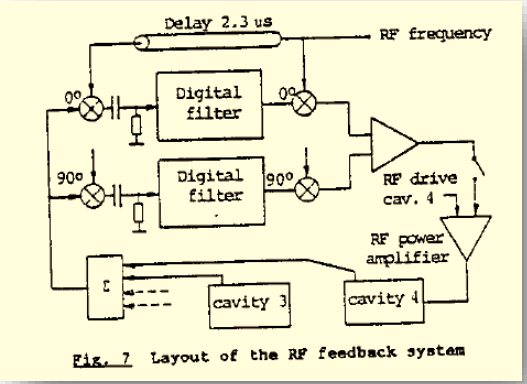
BE-RF:

- Feedback loop design
- Customization of the vector modulator/downconverter/ADC hardware for particular SPS requirements

uTCA PoC, NEW CERN LLRF PARADIGMS…

Avoid sweeping clocks (bunch synchronous);

- Processing/ Sampling clocks are *multiple* of f_{rev}
- *CERN De-facto* since 1983, OTFB
- Go for *fixed clock*
- Modules → COTS



1st Digital One Turn Feedback (OTFB) Boussard, 1983

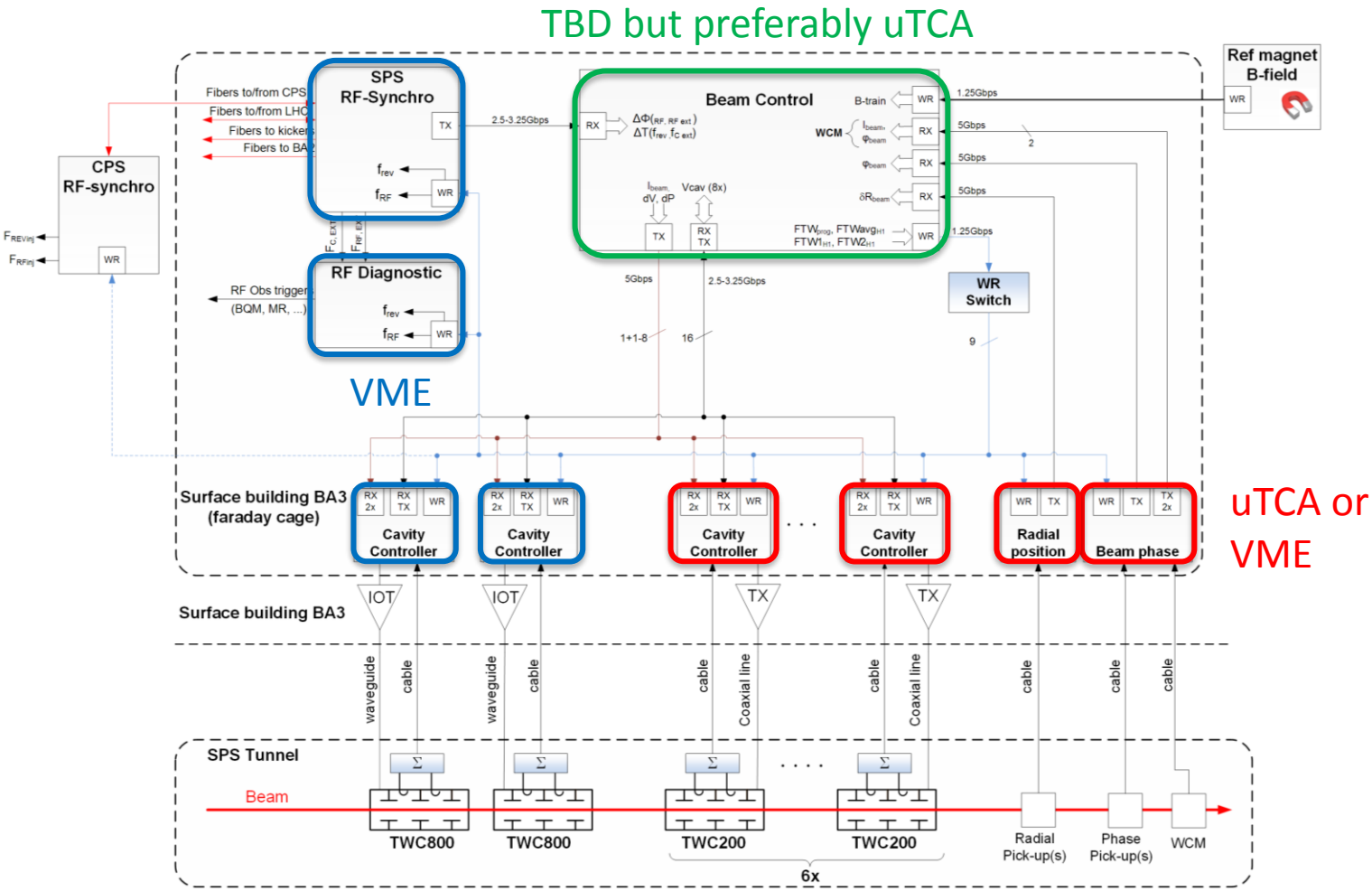
Avoid Master-Slave distribution of RF and clocks;

- Custom *point-to-point* links to all cavities (stations)
- Go for *distributed deterministic* architecture
- Use of *White Rabbit* (deterministic link)
- Broadcast RF *Frequency Tuning Word*
- Reference *Clock extracted* from data (on-going)

PROOF OF CONCEPT

SPS 200Mhz LLRF PRELIMINARY ARCHITECTURE…

- -LLRF
- -PLATFORMS
- -uTCA @ BE
- **-uTCA PoC**



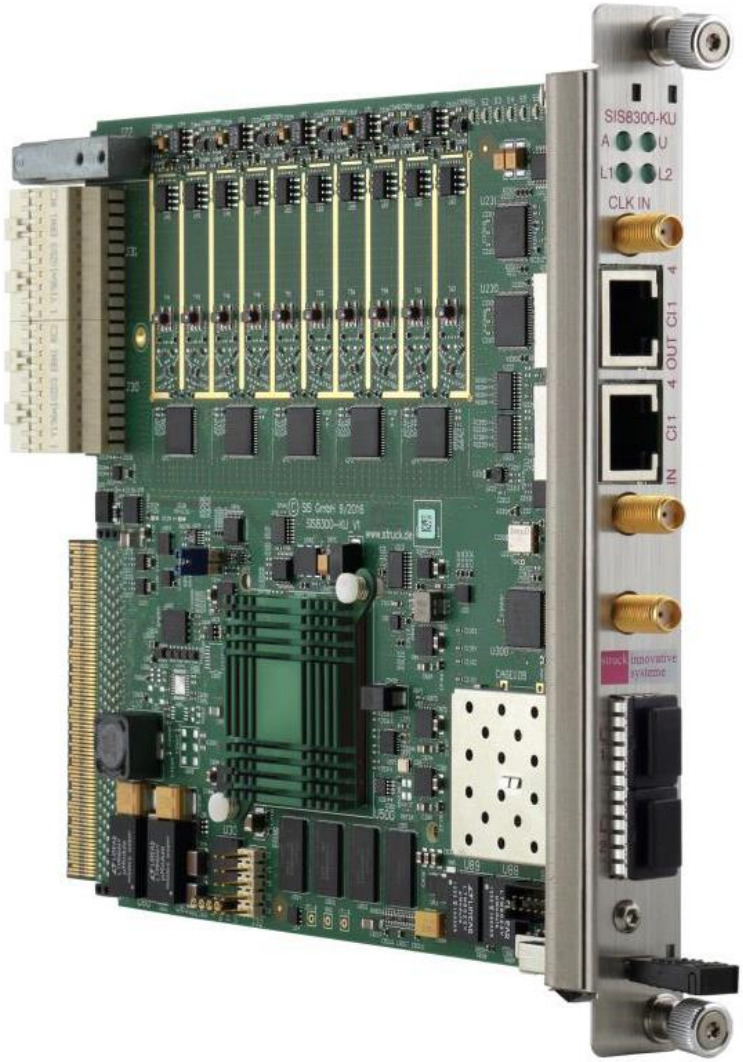
SELECTED uTCA HARDWARE COTS…

Item	Remarks
uTCA.4.1 crate	NAT NATIVE_R9 9U, 12 slots AMC
Power module	NAT-PM-AC600D 600W, 12V
MCH	NAT-MCH-PHYS
CPU	NAT-MCH-RTM & CPU module
Timing module carrier	NAMC-PMC NAMC-PMC-T261 (double width)
AMC extender	NAMC-EXT-RTM-F-PS (uTCA.4)
RTM extender	NAMC-EXT-RTM-R (uTCA.4)
AMC – SIS8300-KU	8AC, 2DC, DAC & Interlock to zone3, White-rabbit option
DRTM – DWC8VM1 } RF	RTM with down-converter, Vector modulator
DRTM – DS8VM1 } Frontend?	RTM for direct-sampling, Vector modulator

LLRF DIGITIZER…

SIS8300-KU (AMC)

- 10 ADC channel 125 MS/s, 16 bits
- 2 DAC channel 250 MS/s , 16 bits
- Kintex ultra-scale KU040
- Dual SFP+
- White Rabbit Option
- 4 x 4Gbit DDR4
- External clock and trigger Inputs
- 4 Lanes PCI Express gen 3



LLRF RF FRONTEND, HETERODYNE…

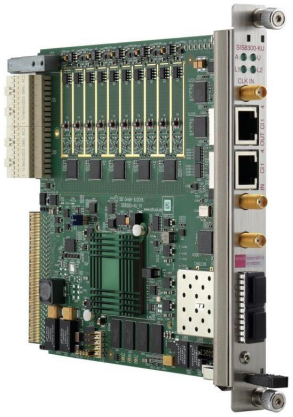
DWC8VM1 (RTM)

- 8 Channels down-converter
  - 700MHz to 4.0GHz
  - 352MHz version for ESS
- 1 channel vector-modulator
  - 700MHz to 4.0GHz
- RF switch
  - at the up-converter output
  - Interlock from AMC or frontpanel

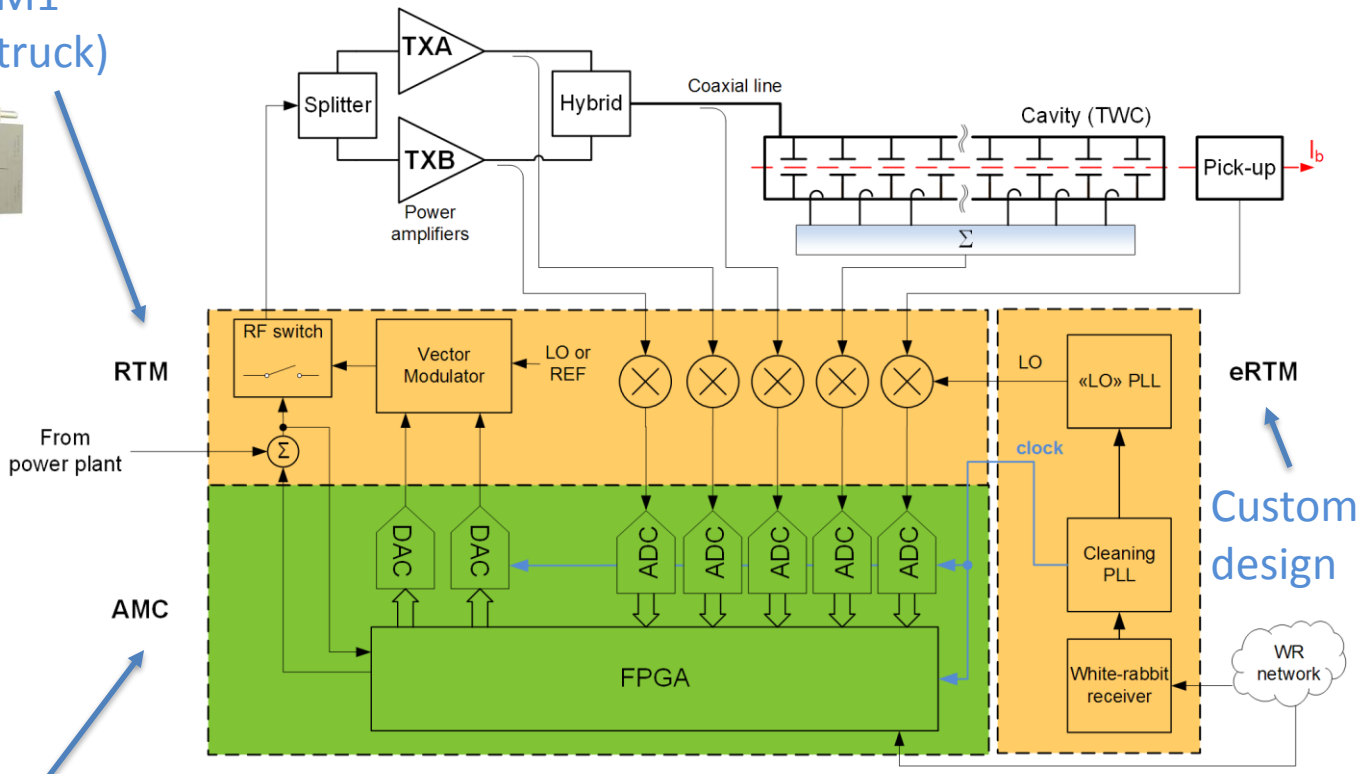
LLRF uTCA CAVITY CONTROLLER, HETERODYNE…

- -LLRF
- -PLATFORMS
- -uTCA @ BE
- **-uTCA PoC**

DWC8VM1
(Desy/Struck)



SIS8300-KU
(Desy/Struck)



LLRF RF FRONTEND, DIRECT SAMPLING…

DS8VM1 (RTM)

8 channels direct-sampling

- 5MHz to 400MHz

2 channels direct-sampling

- DC to 400MHz

1 channel vector-modulator

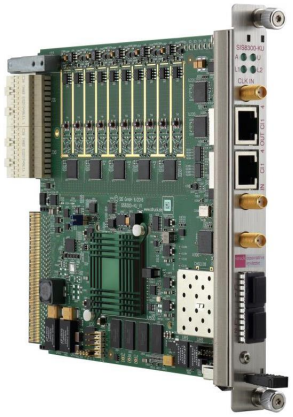
- 50MHz to 6.0GHz
- BW from DC to 50MHz

RF switch at the up-converter output

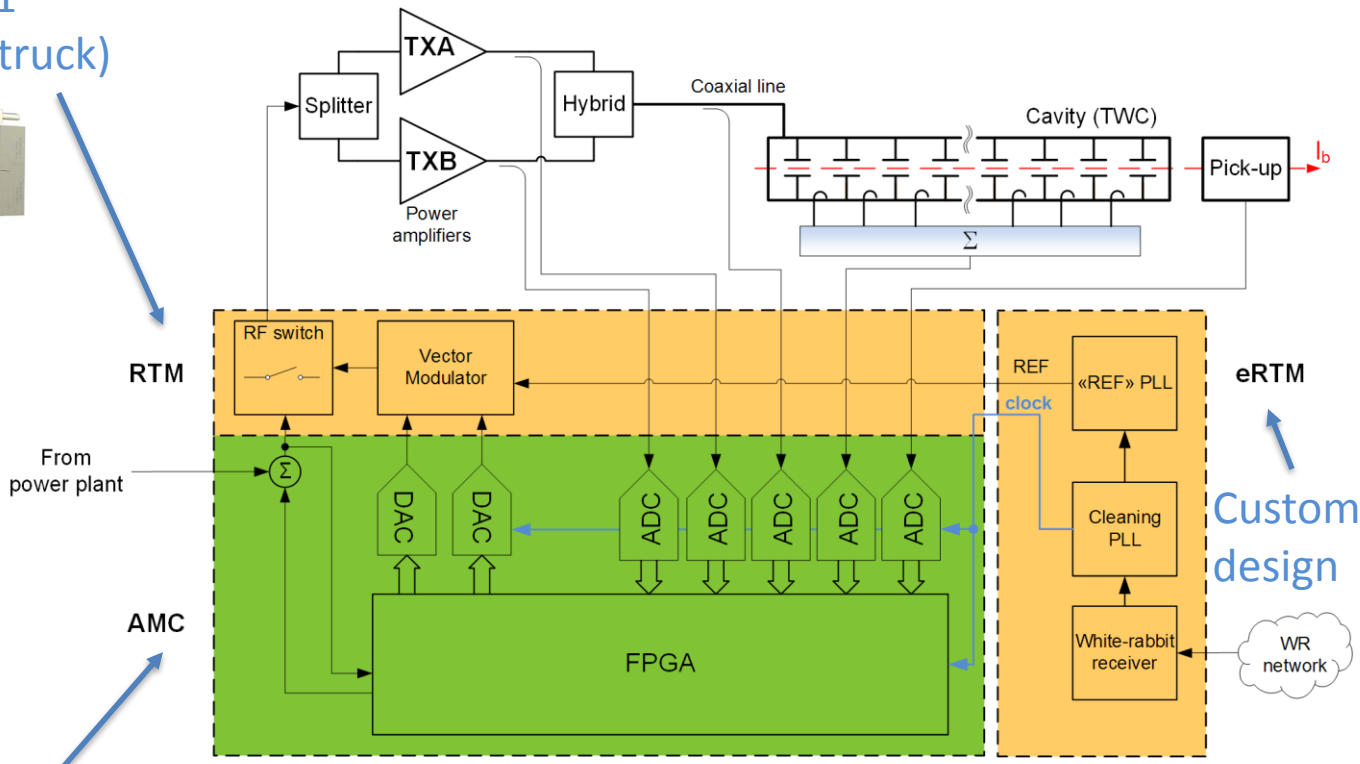
LLRF uTCA CAVITY CONTROLLER, DIRECT SAMPLING…

- -LLRF
- -PLATFORMS
- -uTCA @ BE
- **-uTCA PoC**

DS8VM1
(Desy/Struck)



SIS8300-KU
(Desy/Struck)



Thank you!

Your Time…

BACK UP SLIDES

FIXED CLOCK…

	Bunch Synchronous Clock	Fixed Clock
STABILITY OF THE FEEDBACK LOOPS	Variable sampling clock → Variable loop delay Compromise in Regulation Bandwidth and Feedback Stability	Fixed sampling clock → Fixed loop delay Optimal Regulation Bandwidth and Feedback Stability
PHASE JUMPS	RF as harmonic of clock → multiplexing required to cover wide RF range (PSB) Phase Jumps when multiplexing	Simple DDS implementation can cover a wider range without interruption
ADC AND DAC	Complex analogue reconstruction filter Coherent signals fall in swept range Non optimal integrated noise	Fixed analogue reconstruction filters Coherent signals at fixed digital frequencies Optimized integrated noise
UP AND DOWN MIXING	Sweeping LO -> Lower spectral purity of clock → DDS and IQ sensitive to jitter → Problem for heterodyne architectures	Non IQ sampling and Direct down conversion easier
TECHNOLOGY LIMITATIONS	PLLs tracking and locking Max dF/dt for DCM in FPGAs Clock domain synchronization Serial interfaces FIFOs	PLLs and DCM readily usable Ease clock domain synchronization Ease use of serial interfaces and modern technologies

FIXED CLOCK…

	Bunch Synchronous Clock	Fixed Clock
CLOCK INTERRUPTION BETWEEN CYCLES (ppm operation)	Periodic resynchronizations require RF interruptions, which induce clock interruption in electronics	Dedicated clock can independently handle RF generation and DSP processing
SPECTRAL PURITY OF THE CLOCK	Beam Phase Loop continuously modulates RF on top of sweep Cleaning PLL architectures at varying frequencies -> spectral purity of reconstructed clock not optimal	Dedicated cleaning architecture for clock Optimal spectral purity
RF GYMNASTICS	Fast or abrupt modifications of the phase or frequency of the RF complicated as it affects the ADC-DAC-FPGA clocking Slip stacking merging bunches in the phase space will be difficult.	Dedicated clock for DDS enables Digital RF regeneration Instantaneous modifications of RF phase and frequency driven by data, not by clocks Any type of RF gymnastics

OTFB…

Swept DSP Clock
Ramped Synchrotron

$$H_{comb} = G\frac{b_0 + b_1 \cdot Z^{-N}}{1 + a_0 \cdot Z^{-N} + a_1 \cdot Z^{-2N}}$$

$f_{RF} + kf_{rev}$ Transient Beam Loading

$f_{RF} + kf_{rev} \pm f_s$ Stability dipolar mode

$f_{RF} + kf_{rev} \pm f_s \pm 2f_s$ Stability quadripolar mode