Track Triggers

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Future of collider searches for Dark Matter at the LPC
July 27-28, 2017

Outline

- What is a "track trigger"?
  - Physics motivations for track triggers
- Current generation of track trigger in ATLAS: FTK
  - System design and performance
- Track triggers for the High-Lumi LHC (Phase-II upgrade)
  - Upgrade design goals and current concepts

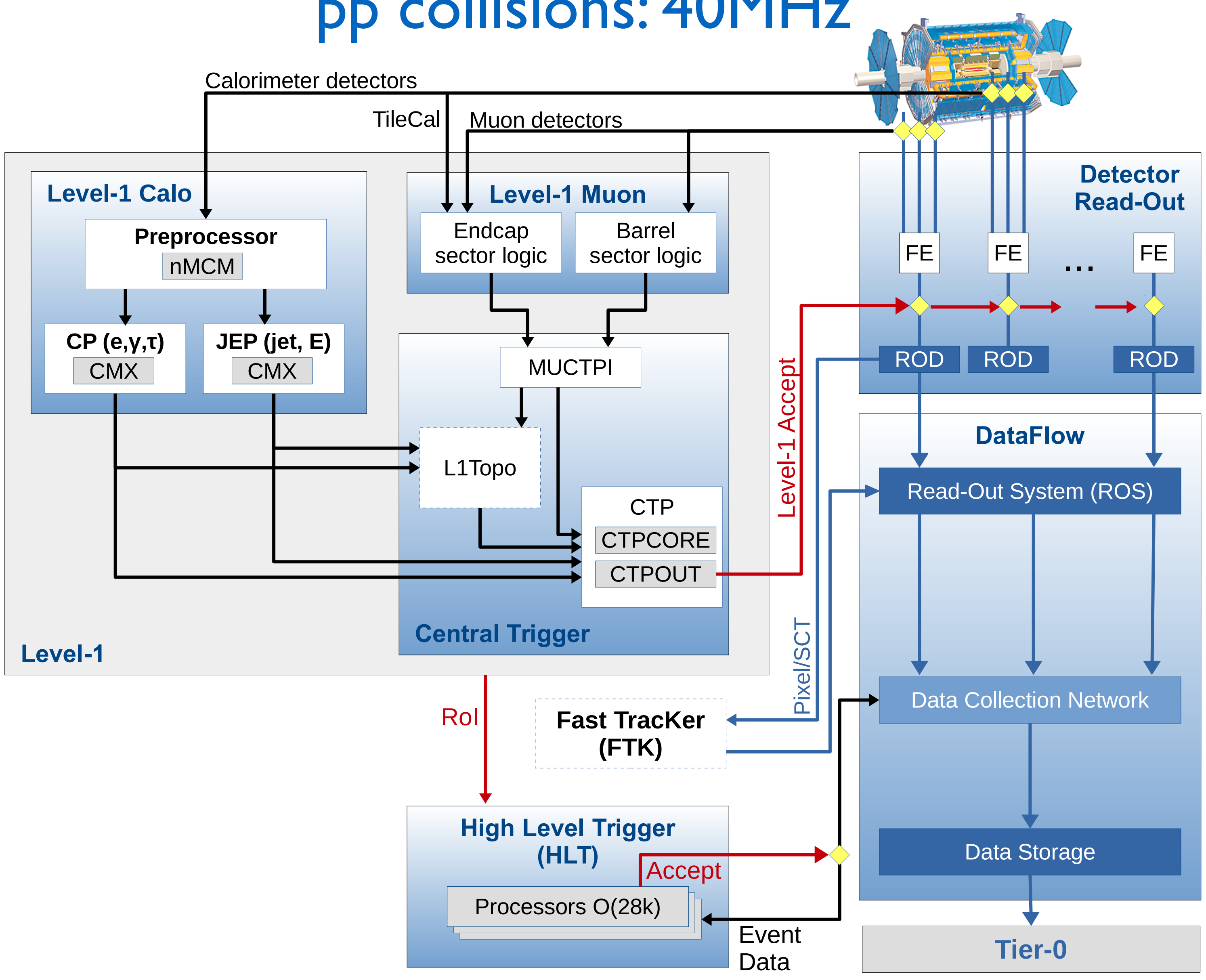
What is a "track trigger"?

Consider current layout of the ATLAS trigger (a 2-level system)

pp collisions: 40MHz

Level 1:
implemented in hardware
reduces rate to 100kHz
(L1calo & L1muon)

High-level Trigger (HLT):
implemented in CPUs
steps to final rate ~1kHz



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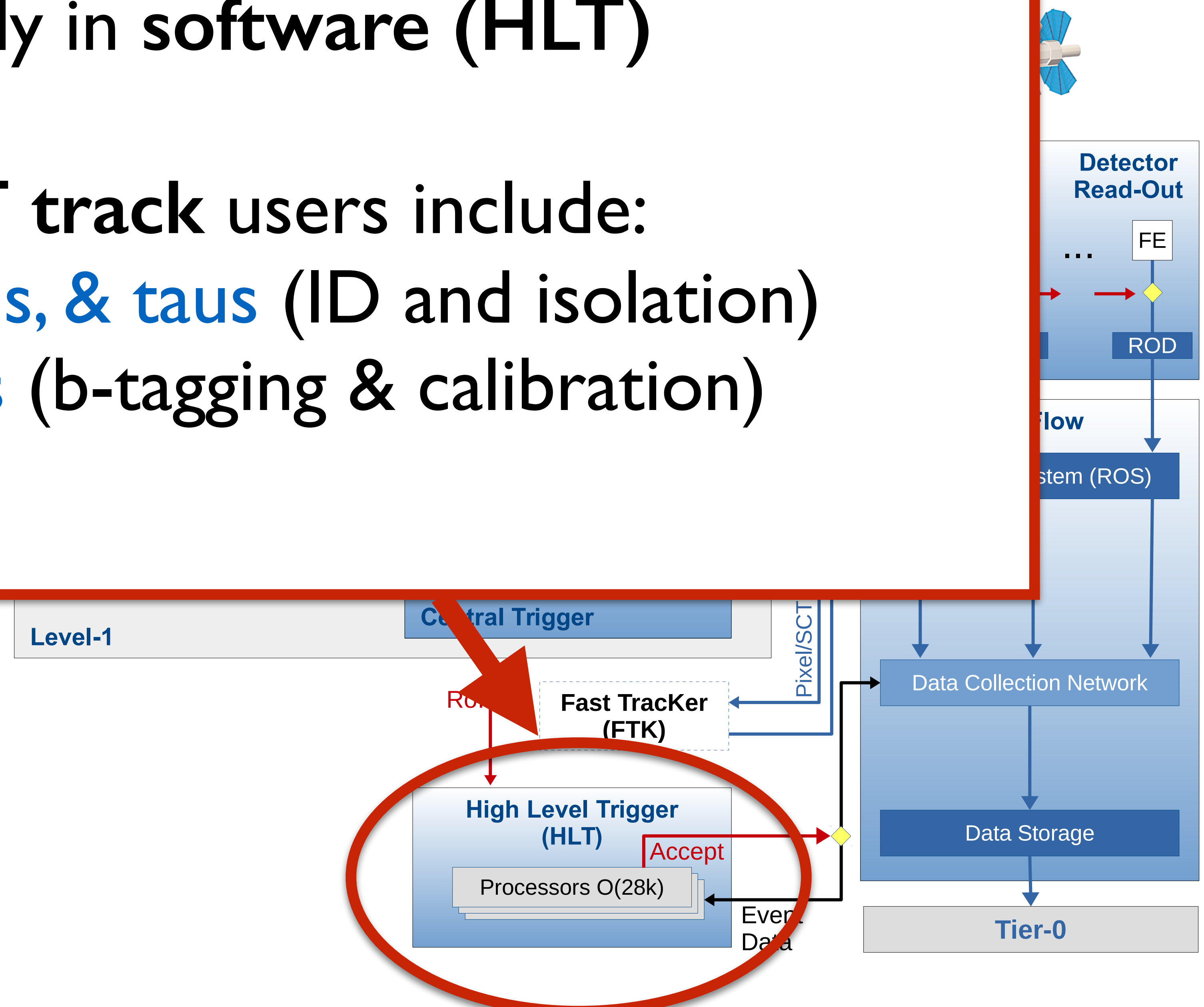
Software tracking

Co… …em)

imple…
redu…
(L…

We currently use tracks in the trigger,
though only in **software (HLT)**

Many **HLT track** users include:
electrons, muons, & taus (ID and isolation)
as well as jets (b-tagging & calibration)



High-level Trigger (HLT):
implemented in CPUs
steps to final rate ~1kHz

Drawbacks

Co em)

imple
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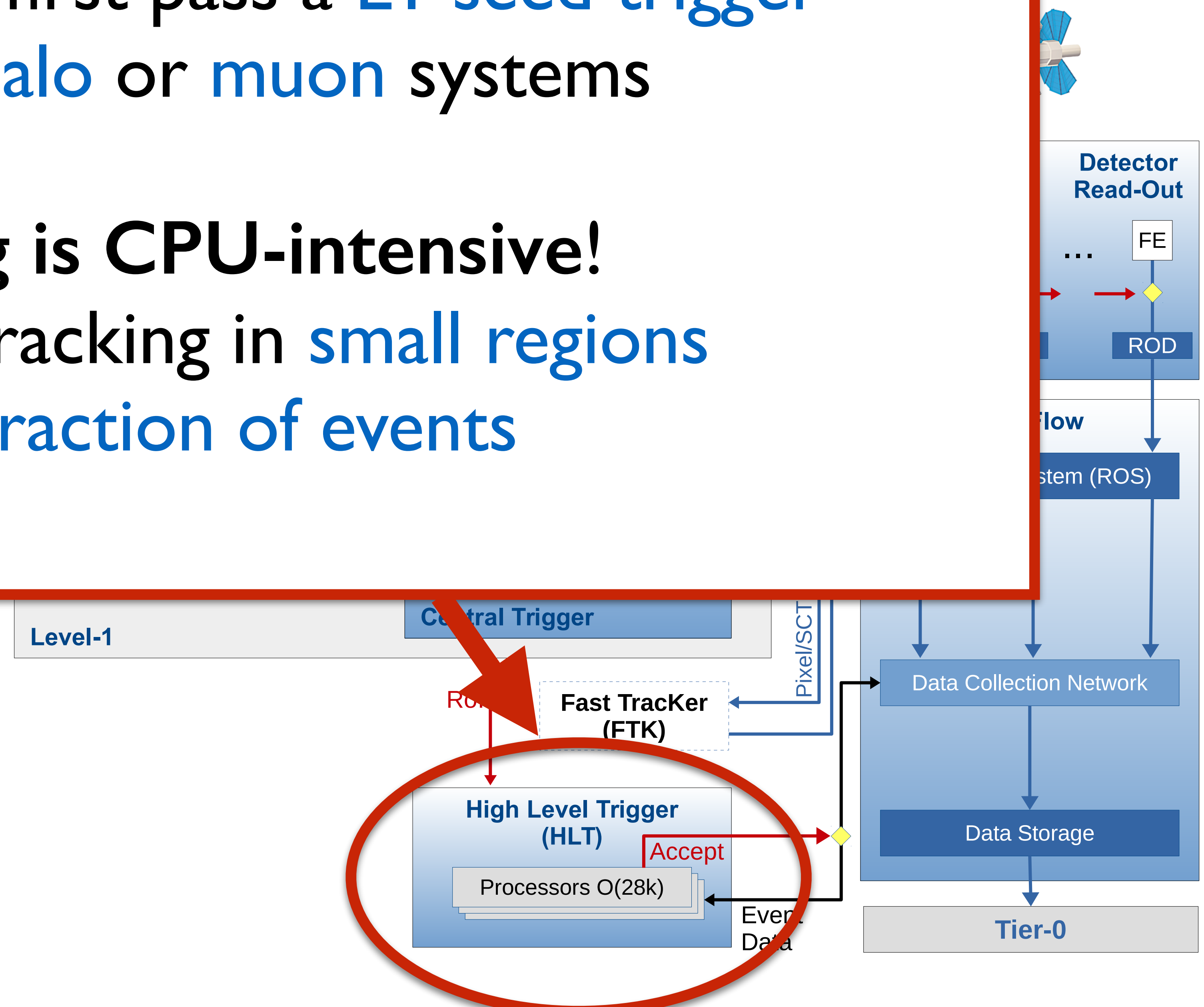
Limited to the HLT rate

All events must first pass a L1 seed trigger from the calo or muon systems

Tracking is CPU-intensive!

Limited to tracking in small regions for a fraction of events

High-level Trigger (HLT): implemented in CPUs steps to final rate ~1kHz



Track trigger

Co… …em)

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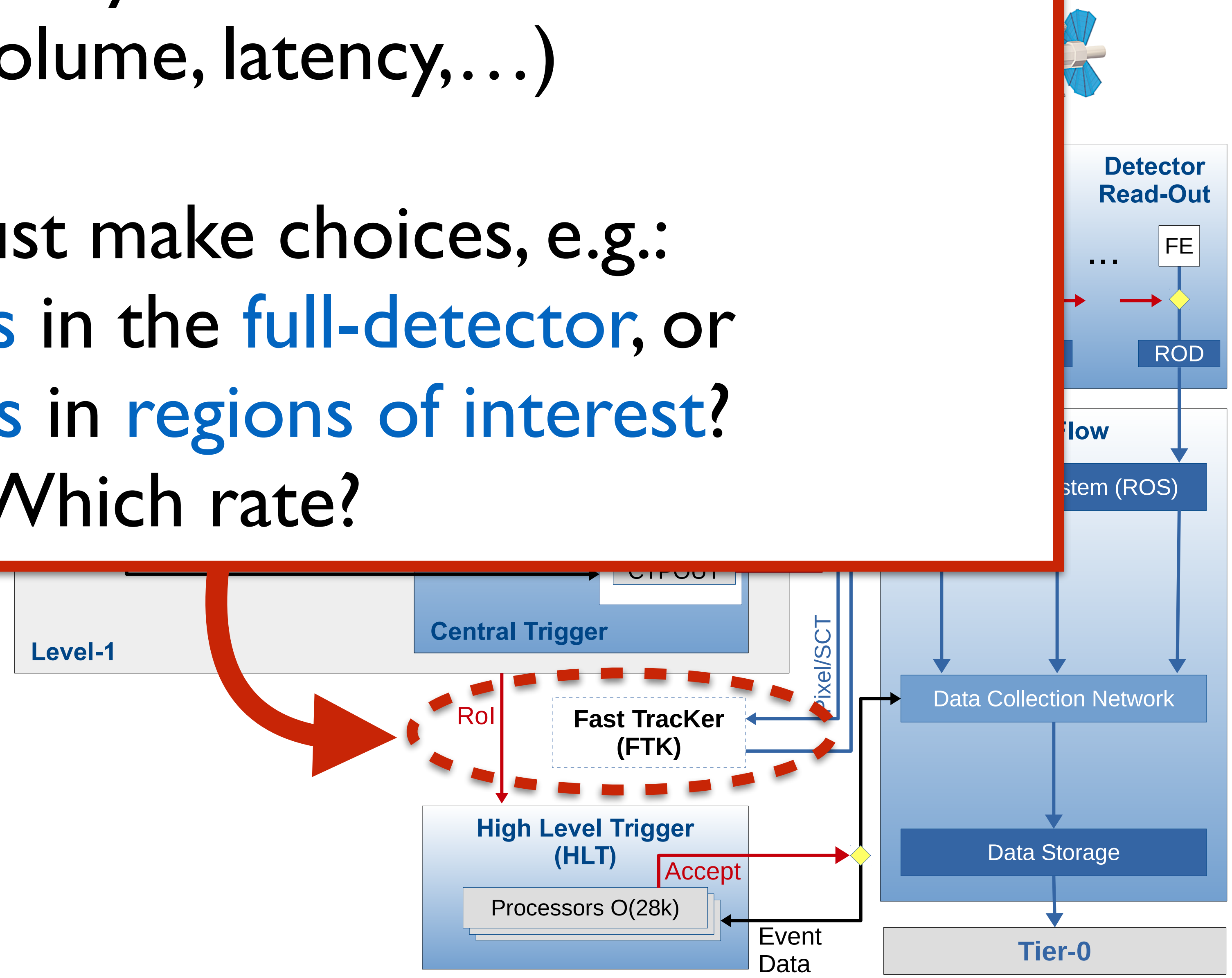
Partially solve problems w/ **hardware track trigger**

But still face system constraints
(data volume, latency,…)

So one must make choices, e.g.:
4 GeV tracks in the full-detector, or
1 GeV tracks in regions of interest?
Which rate?



High-level Trigger (HLT):
implemented in CPUs
steps to final rate ~1kHz

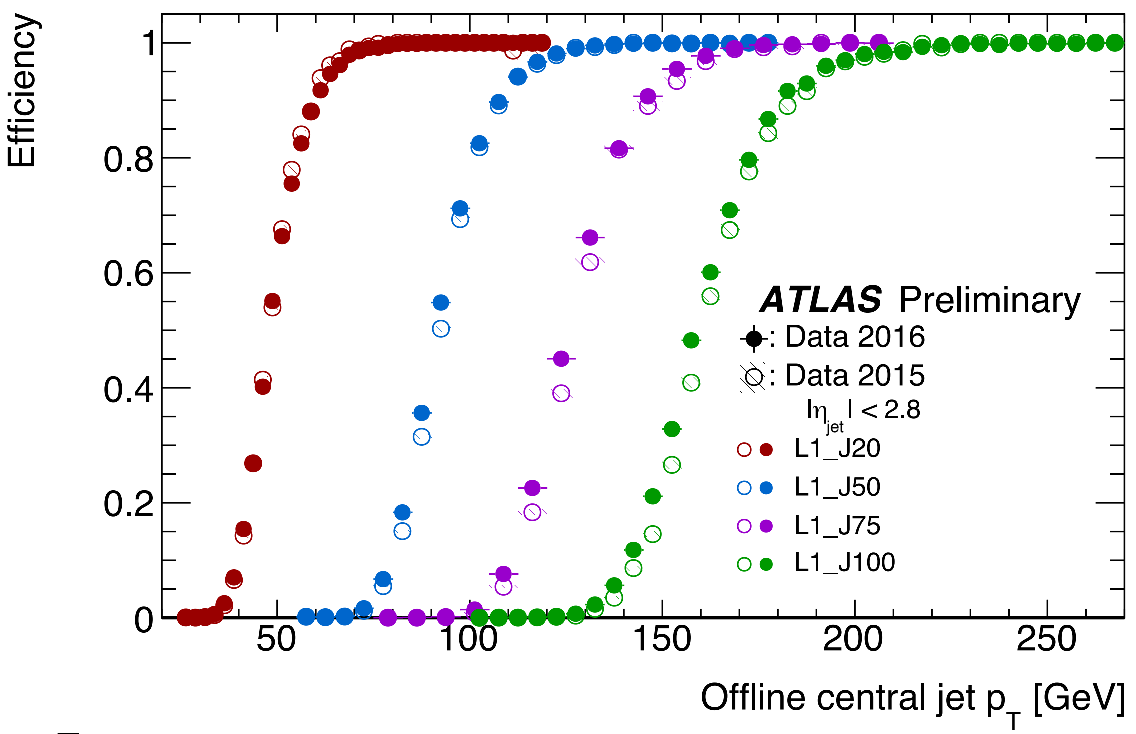
Physics motivations for track triggers

- b-tagging

Crucial for many signatures:
hh→4b, h→bb (VBF), etc.

2017 4-jet thresholds:
35 GeV w/ b-tag
120 GeV w/o b-tag

With b-tagging, trigger is CPU-limited, using 15% of HLT resources!



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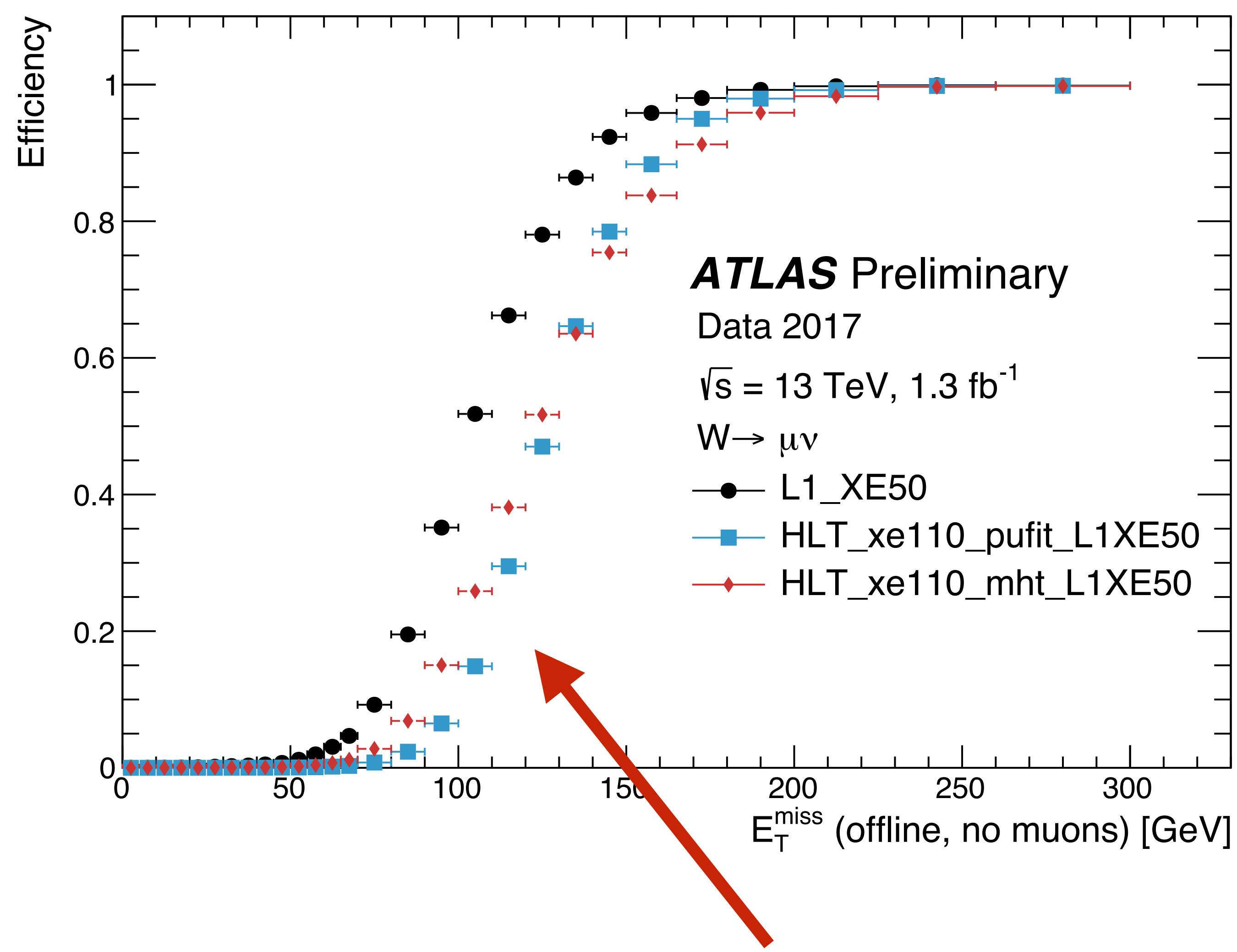
Physics motivations for track triggers

- b-tagging
- MET (soft term)

MET very difficult in the trigger,
must get calculate energy over entire detector

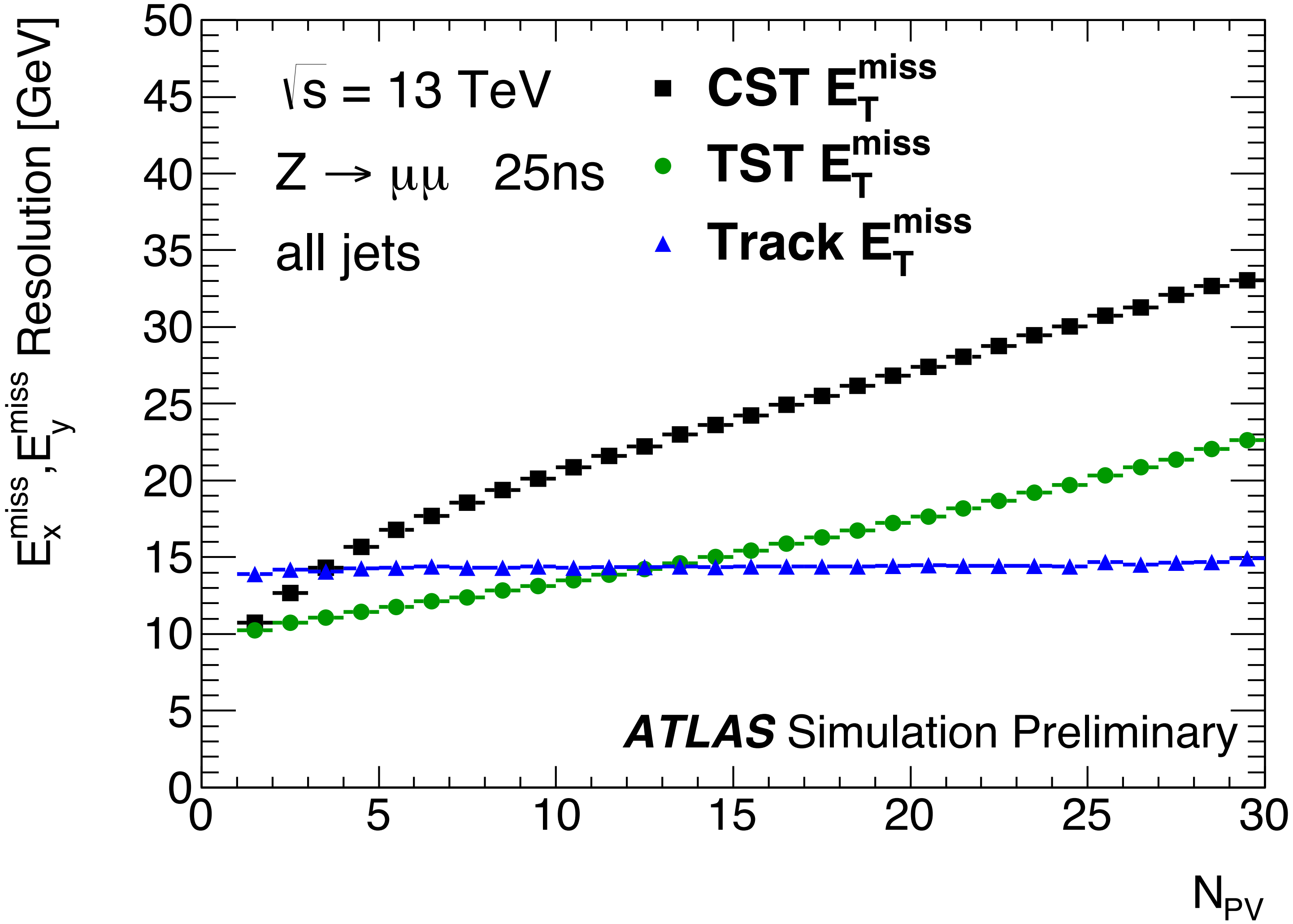


poor resolution = "wasted" rate

Physics motivations for track triggers

- b-tagging
- MET (soft term)

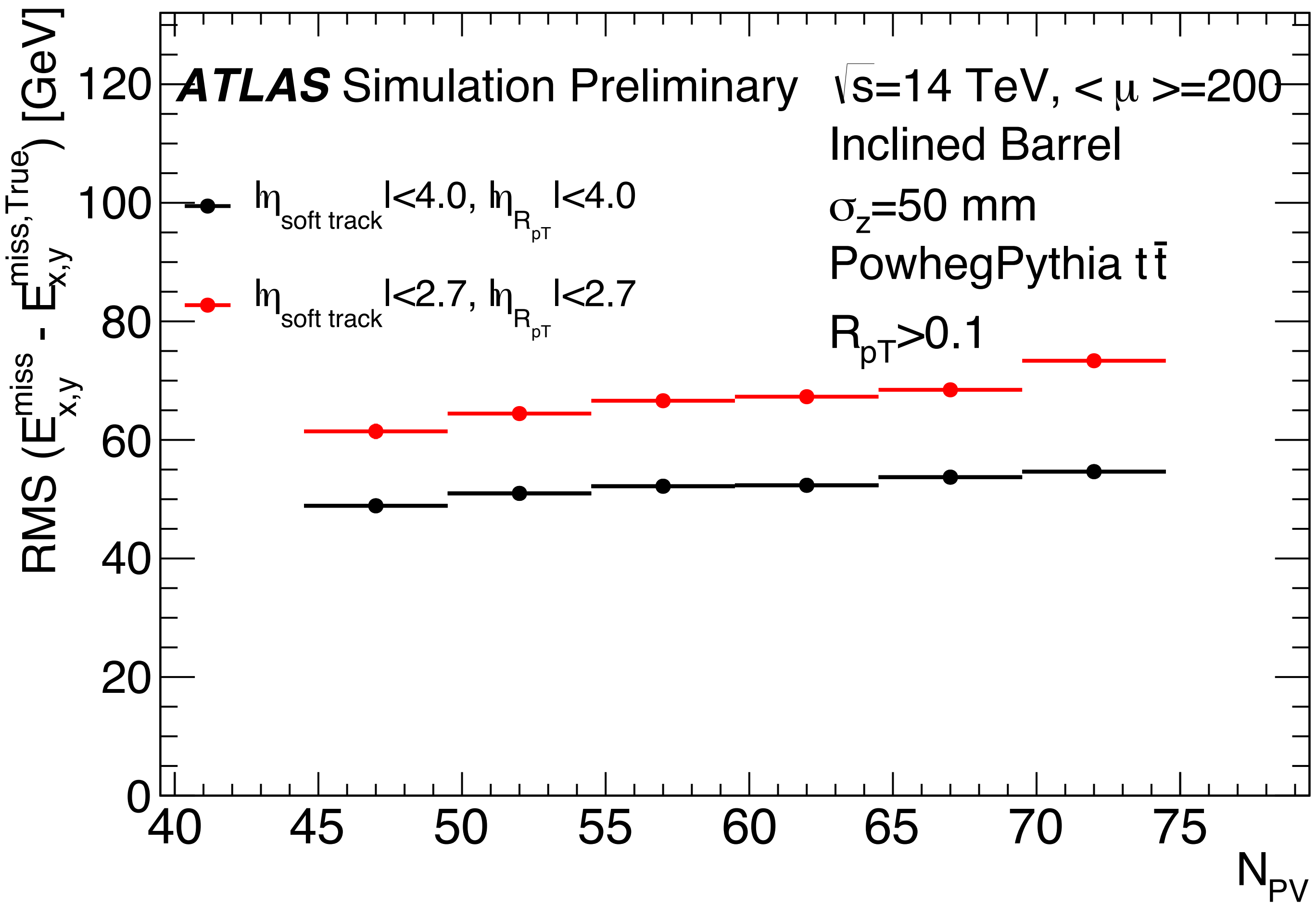
track-based soft term can significantly improve resolution



tracks can also help ID hard objects coming from the primary vertex

Physics motivations for track triggers

- b-tagging
- MET (soft term)



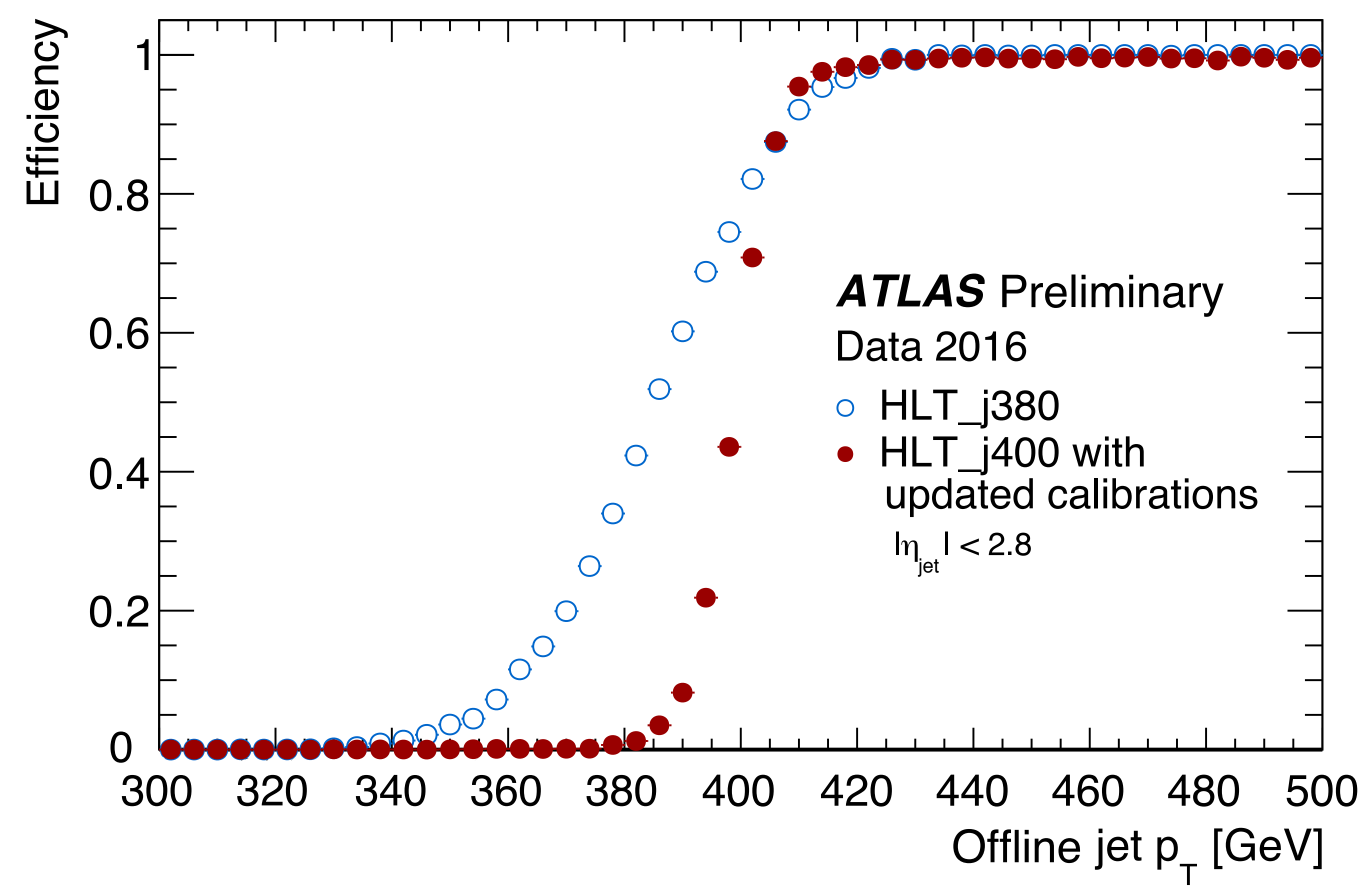
forward tracking brings substantial improvement

Physics motivations for track triggers

Calorimeter response varies w/shower shape

Track-based corrections reduce wasted rate

- b-tagging
- MET (soft term)
- jet energy calibration



Common theme for hadronic triggers!

Physics motivations for track triggers

- b-tagging
- MET (soft term)
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Calorimeter response varies w/shower shape

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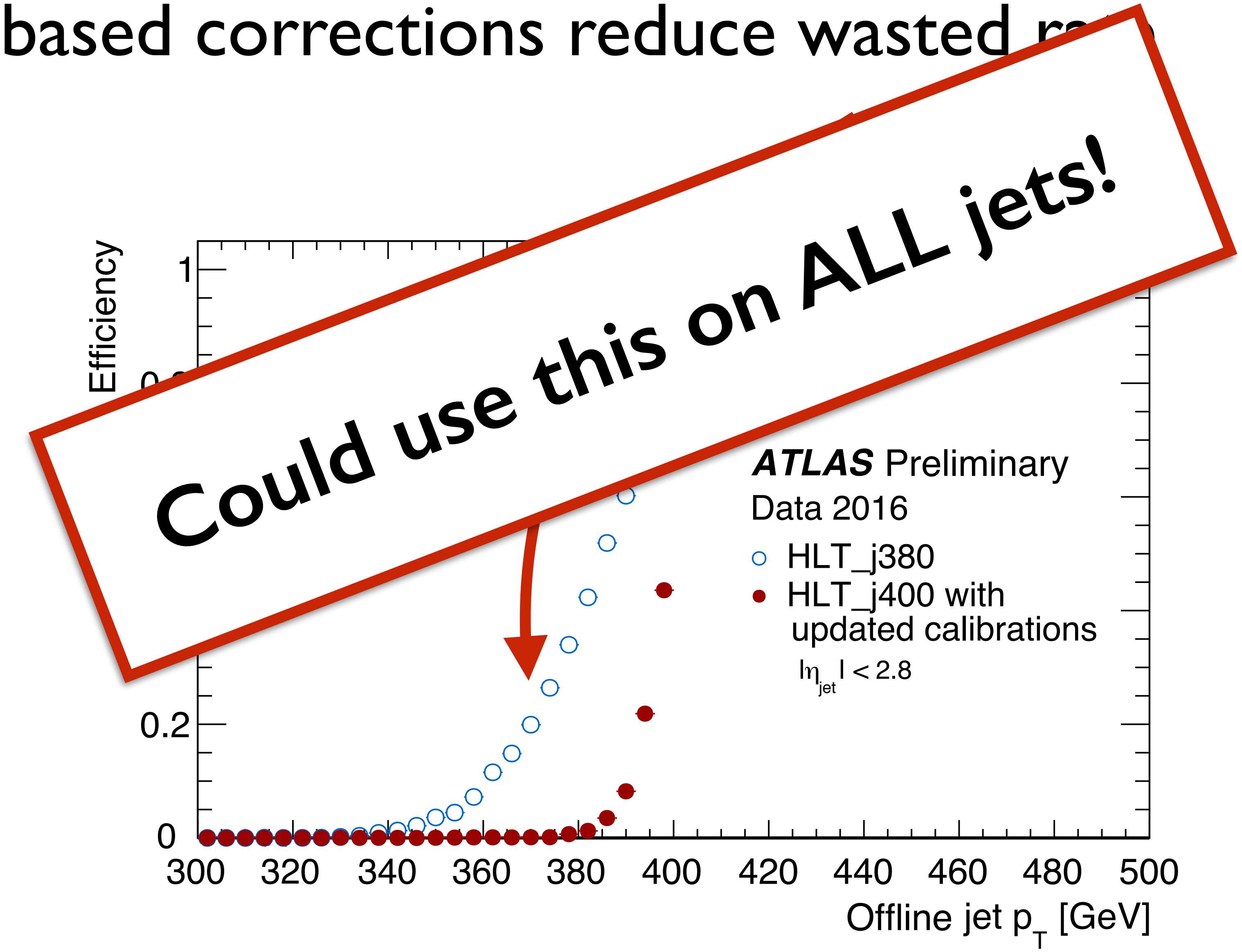
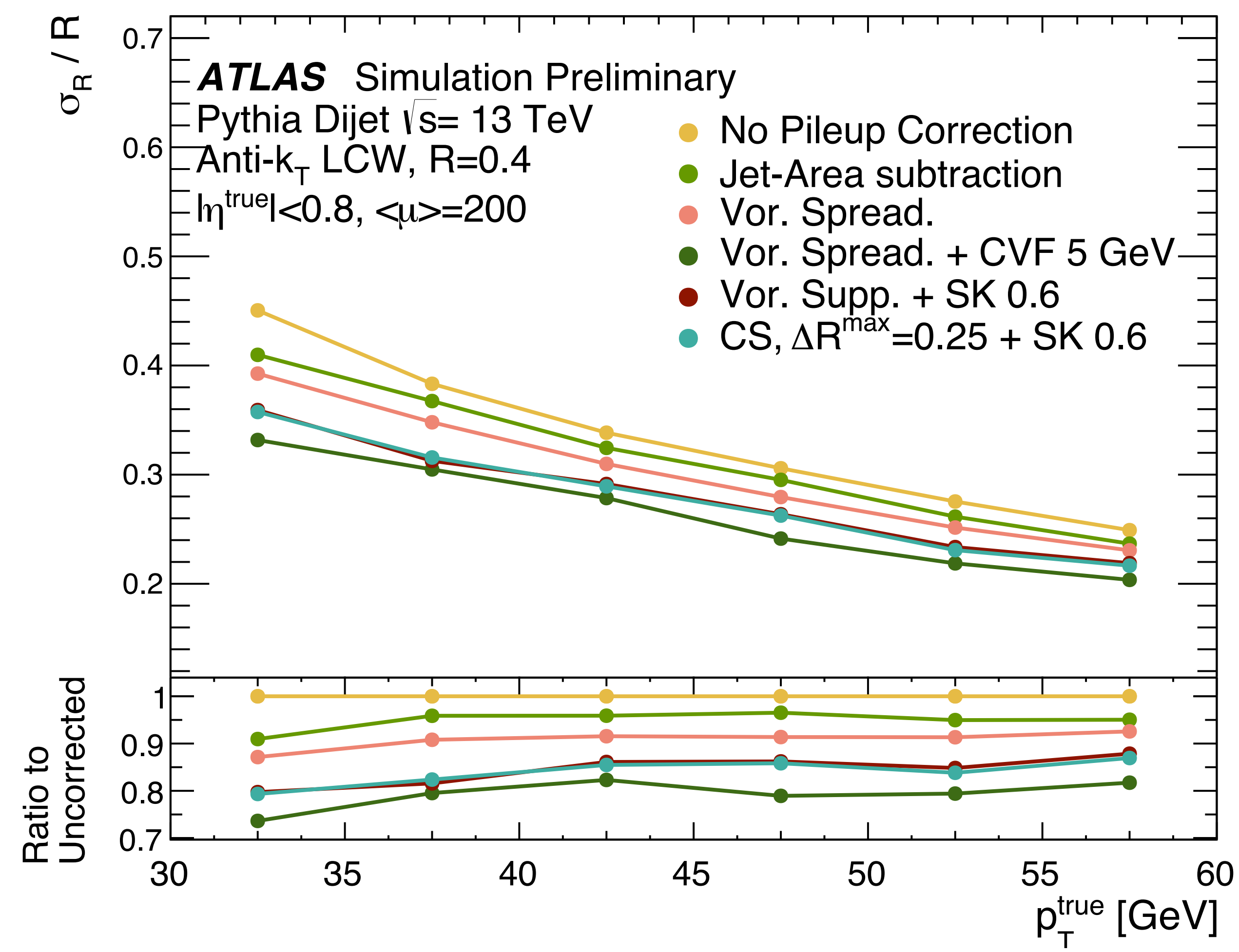


Common theme for hadronic triggers!

Physics motivations for track triggers

- b-tagging
- MET (soft term)
- jet energy calibration
- pileup subtraction

pileup increasingly important



constituent-level pileup suppression improves jet energy resolution

Physics motivations for track triggers

- b-tagging
- MET (soft term)
- jet energy calibration
- pileup subtraction
- Much more!

hadronic taus

$h \rightarrow \tau\tau$, $hh \rightarrow \tau\tau bb$

SUSY: direct staus

VBF triggers
w/ quark-tagging?

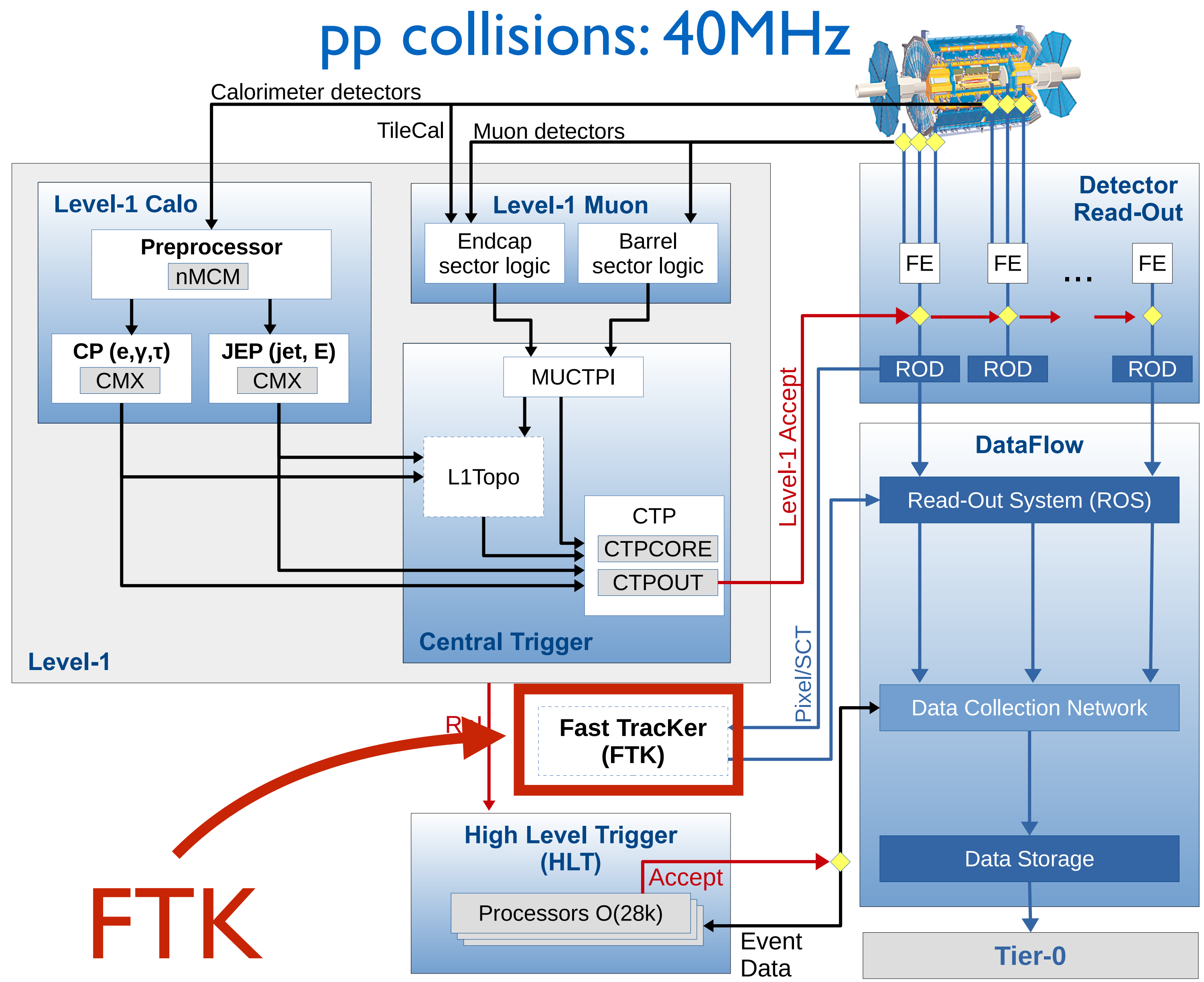
novel signatures?

trigger-level
analyses

**Your new ideas from
DM@LPC workshop???**

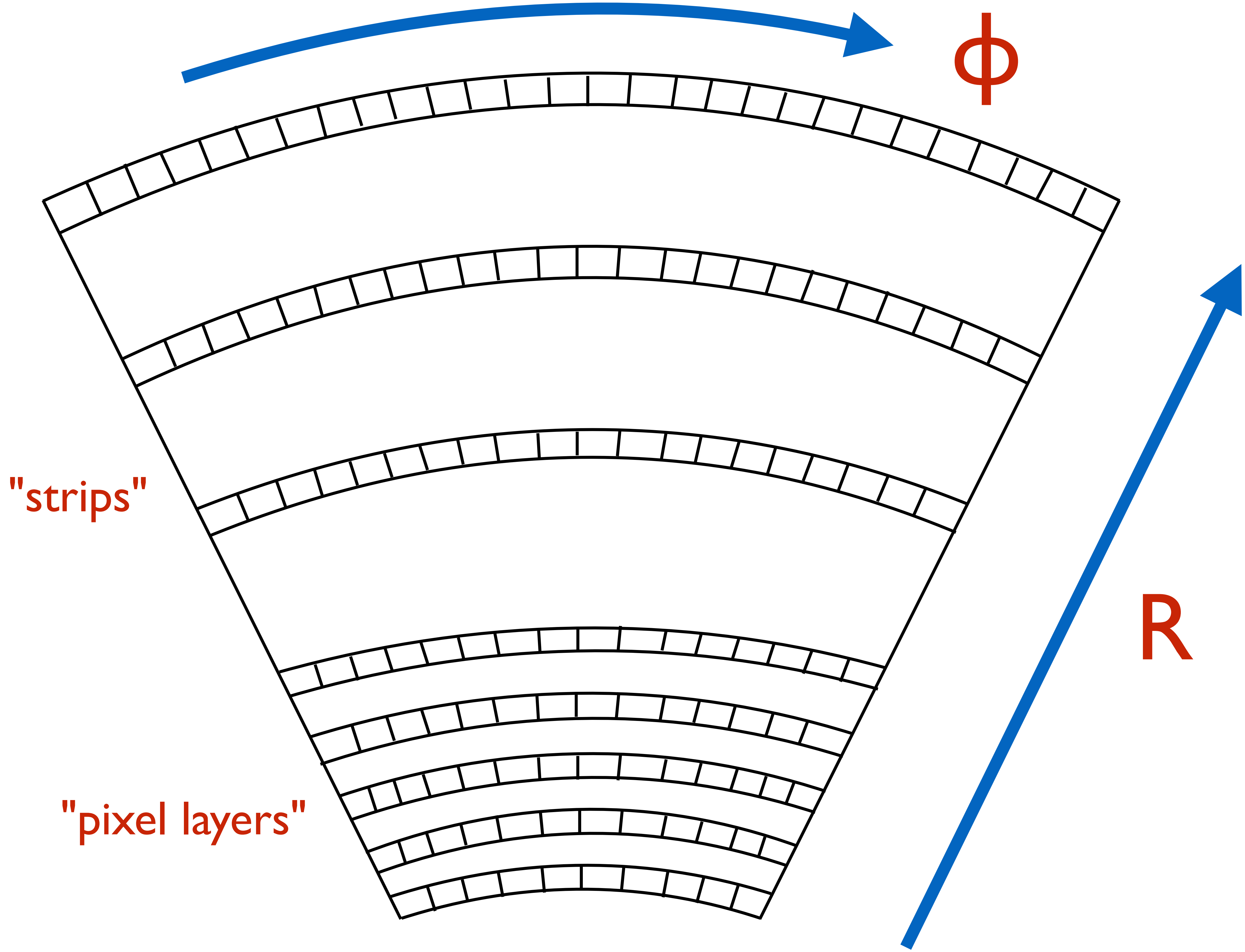
Track triggers in 2017

- ATLAS has already built the Fast TracKer (FTK) system
- Running in "commissioning mode" for 2017
- Designed with associative memory (AM) technology
- Built to deliver tracks (1 GeV, full-scan) at 100 kHz, up to lumi of 3×10^{34} $cm^{-2}s^{-1}$
- Full tracking available to all HLT algorithms

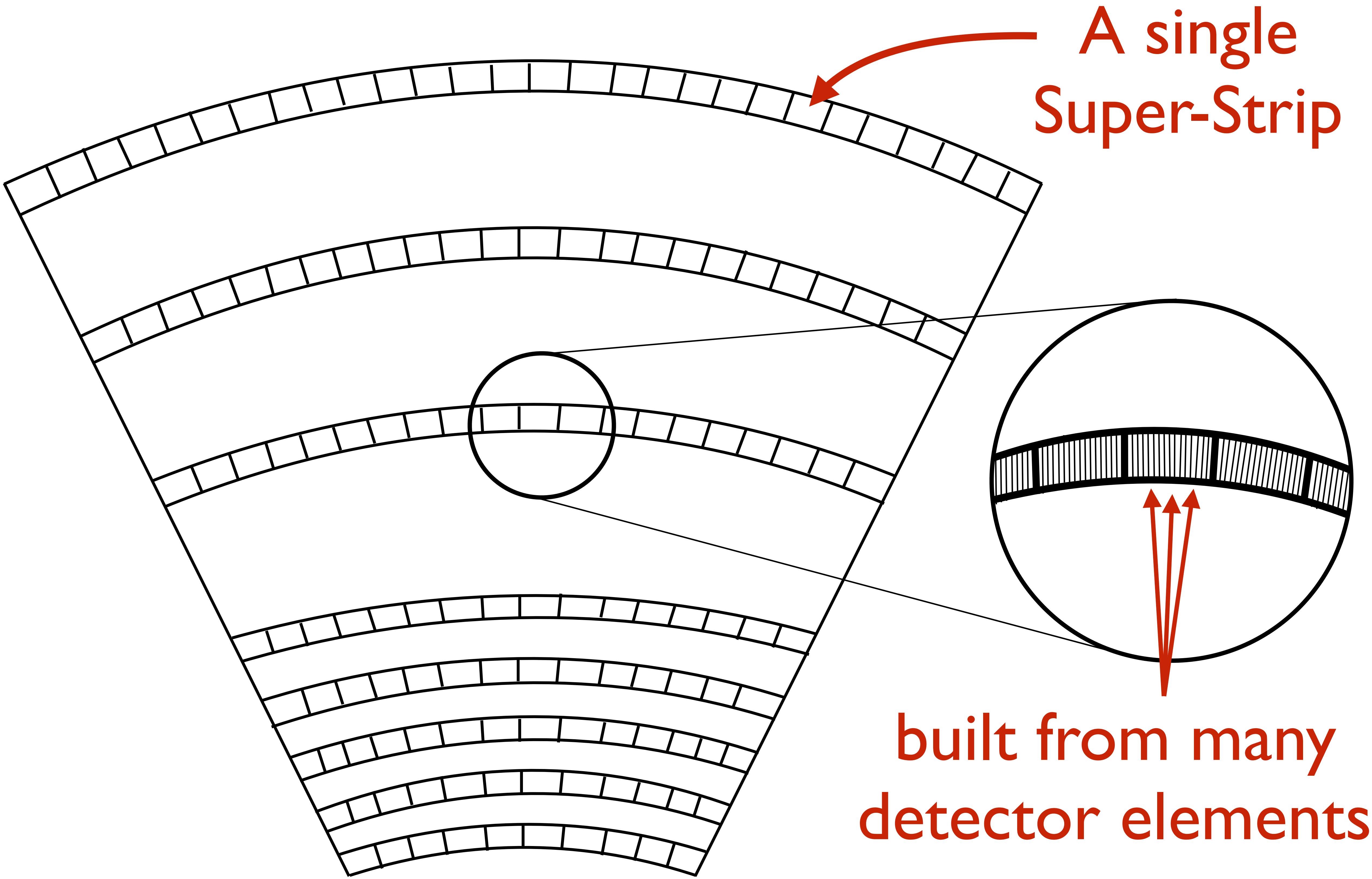


AM track trigger concept

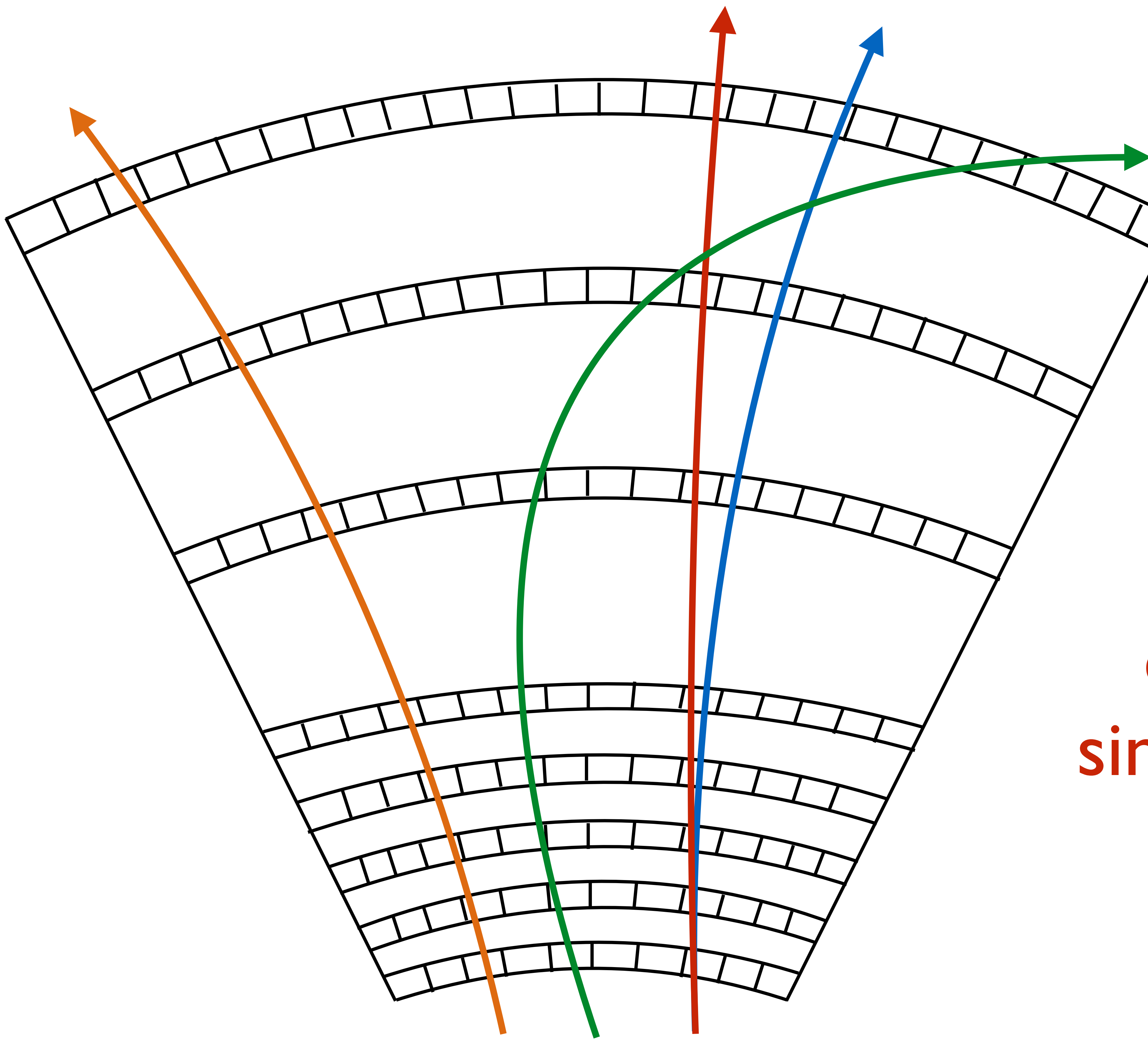
- No real time track-finding, instead pre-store coarse tracks and lookup based on silicon hits
  - Coarse tracks seed more precise "track-fitting" step
- Full procedure consists of two essential parts
  - **Pattern matching**
    - Group detector elements into super-strips
    - Build patterns out of the super-strips
  - **Track fitting**
    - Read all detector elements hits from matched patterns
    - Perform a linear fit from $\{x_i\} \rightarrow \{p_T, eta, phi, d_0, z_0\}$



Consider a toy model slice of a detector

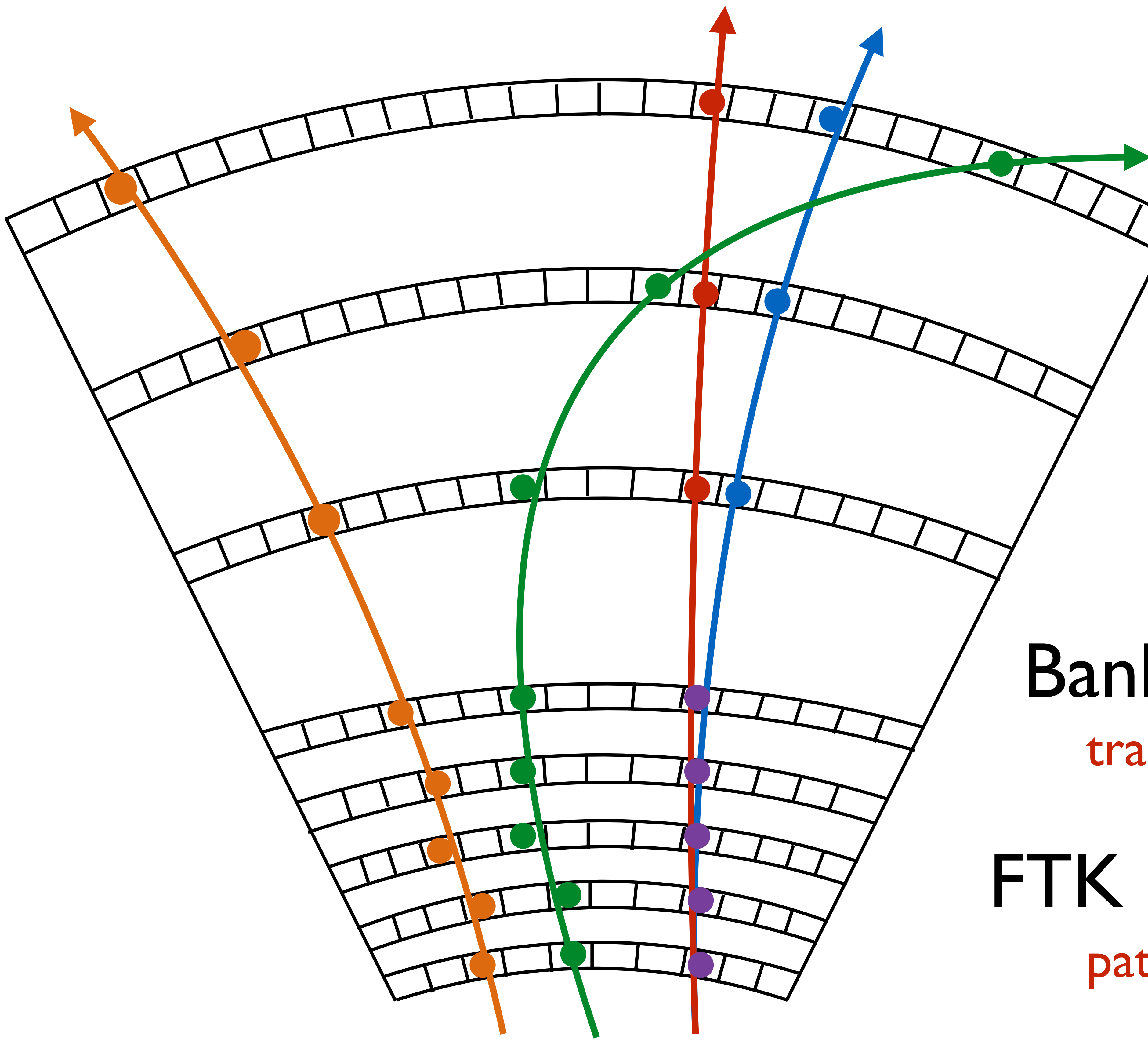


Detector elements are grouped into super-strips



consider
single muons

Tracks impinge the detector, leaving hits in the super-strips



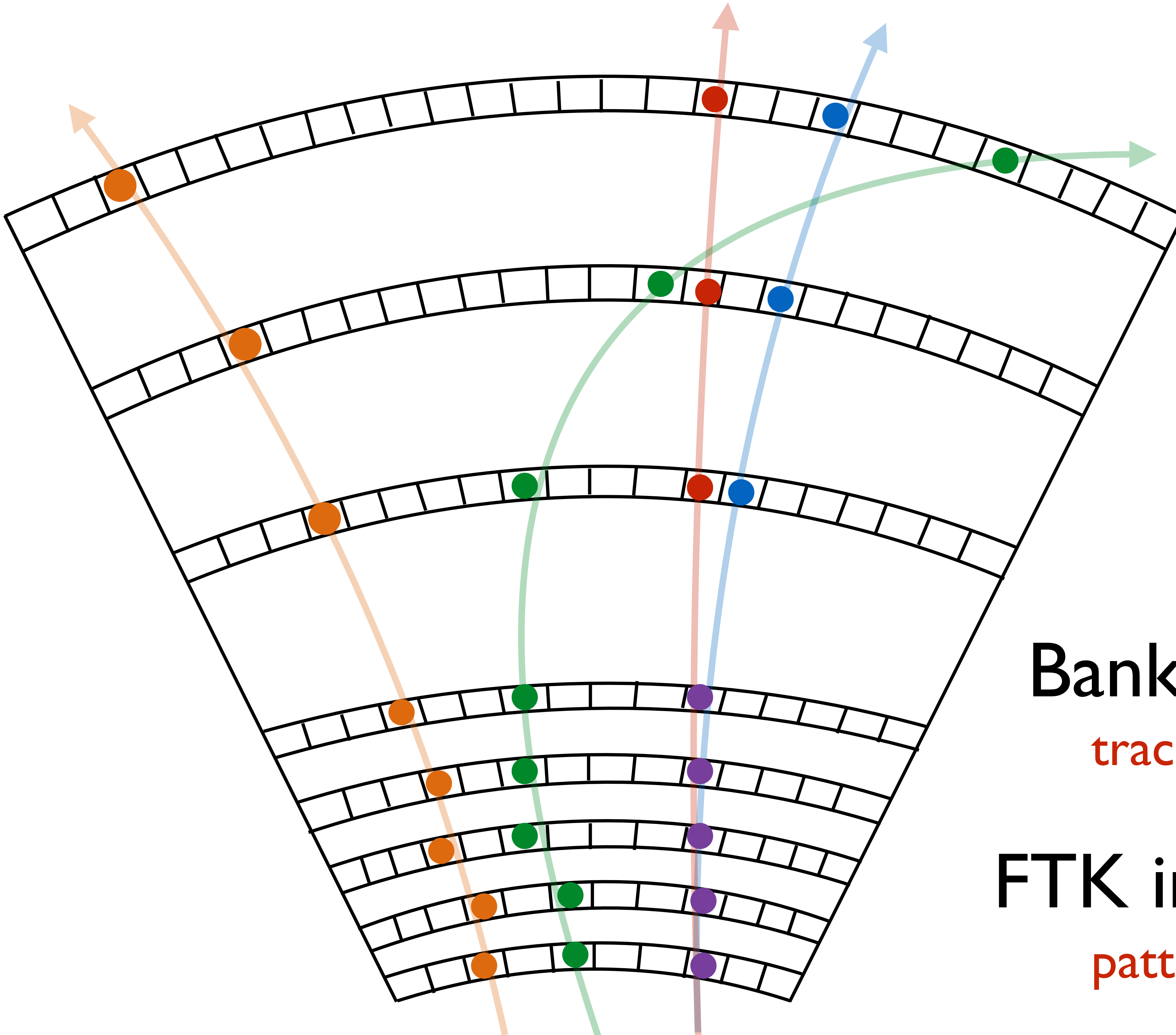
Bank generation

tracks → patterns

FTK in data-taking

patterns → tracks

A set of super-strips (1 per layer) defines a pattern



Bank generation

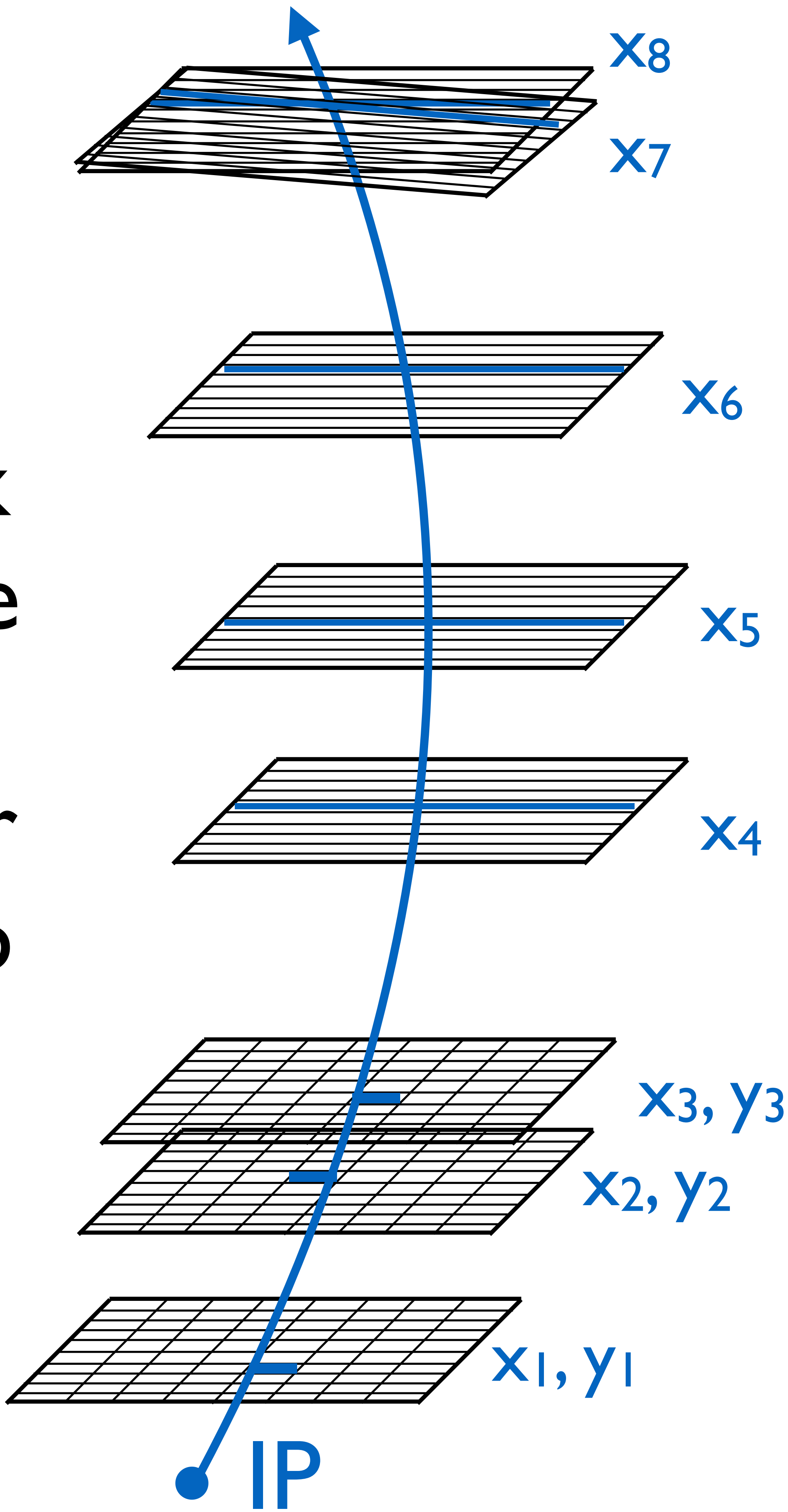
tracks → patterns

FTK in data-taking

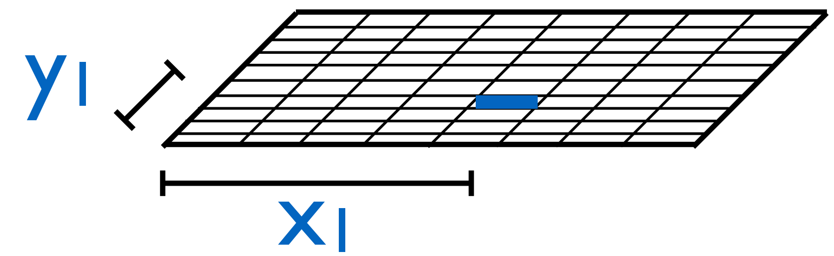
patterns → tracks

Generate billions of muons to create a bank of patterns

Look inside each super-strip



Each hit gives 1 or 2 coordinates



Perform linear fit

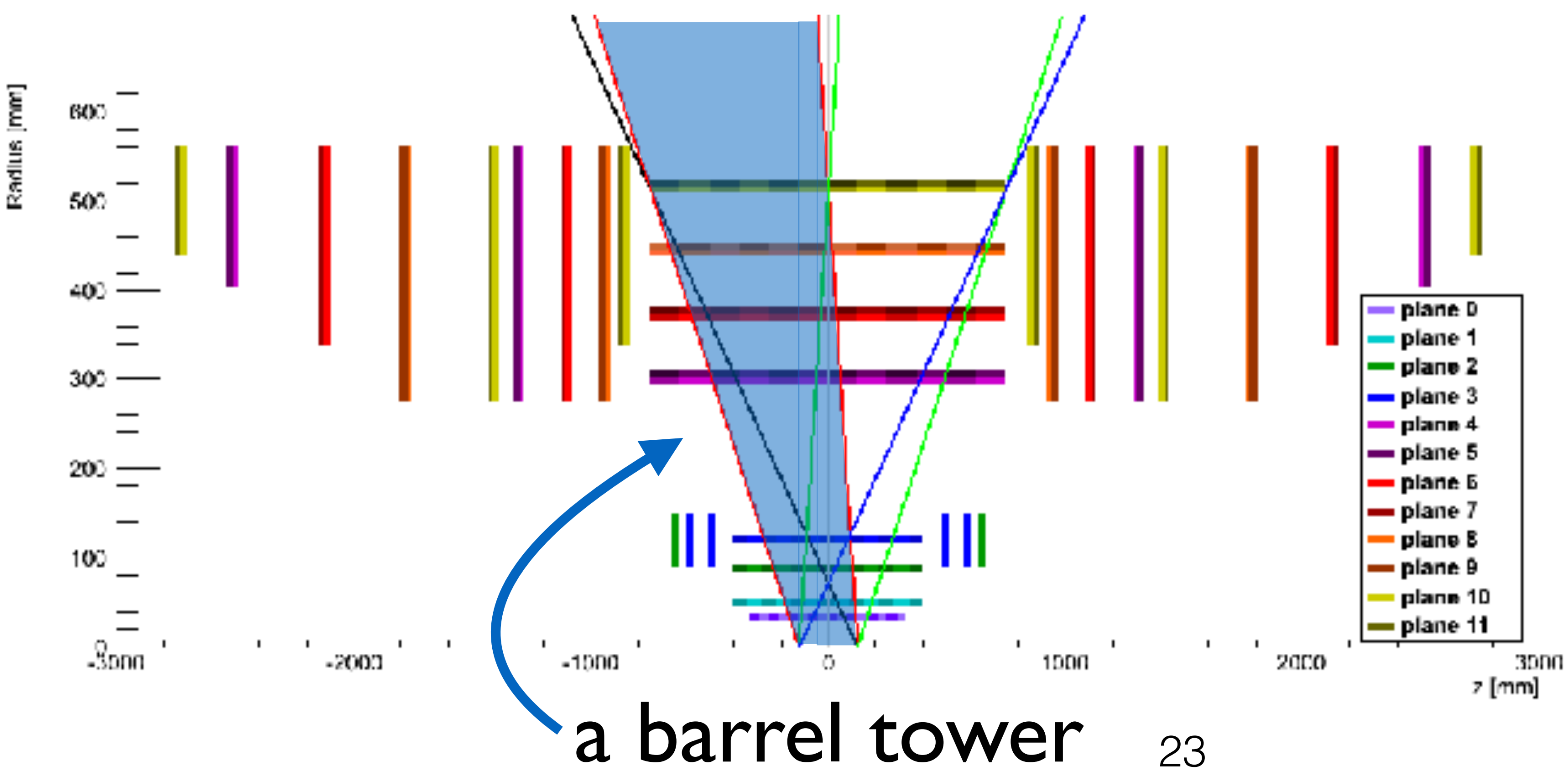
$\{x_i\} \rightarrow \{q_i\} = \{p_T, eta, phi, d_0, z_0\}$

$$q_i = C_{ij}x_j + q^0_i$$

Locally defined fit constants

FTK details

- FTK designed to operate in two stages,
  - Pattern+fits using 8-layers (IBL+2pix+5strips) w/ ≥ 7 hit
  - Roads extrapolated to full 12 layers (req 3 of 4 add'l layers hit) and second track fit performed
- Parallelization: detector divided into 64 "towers" working independently on different detector regions



per tower:
16.8M patterns
16k roads max
80k fits max

in total:
a billion patterns!

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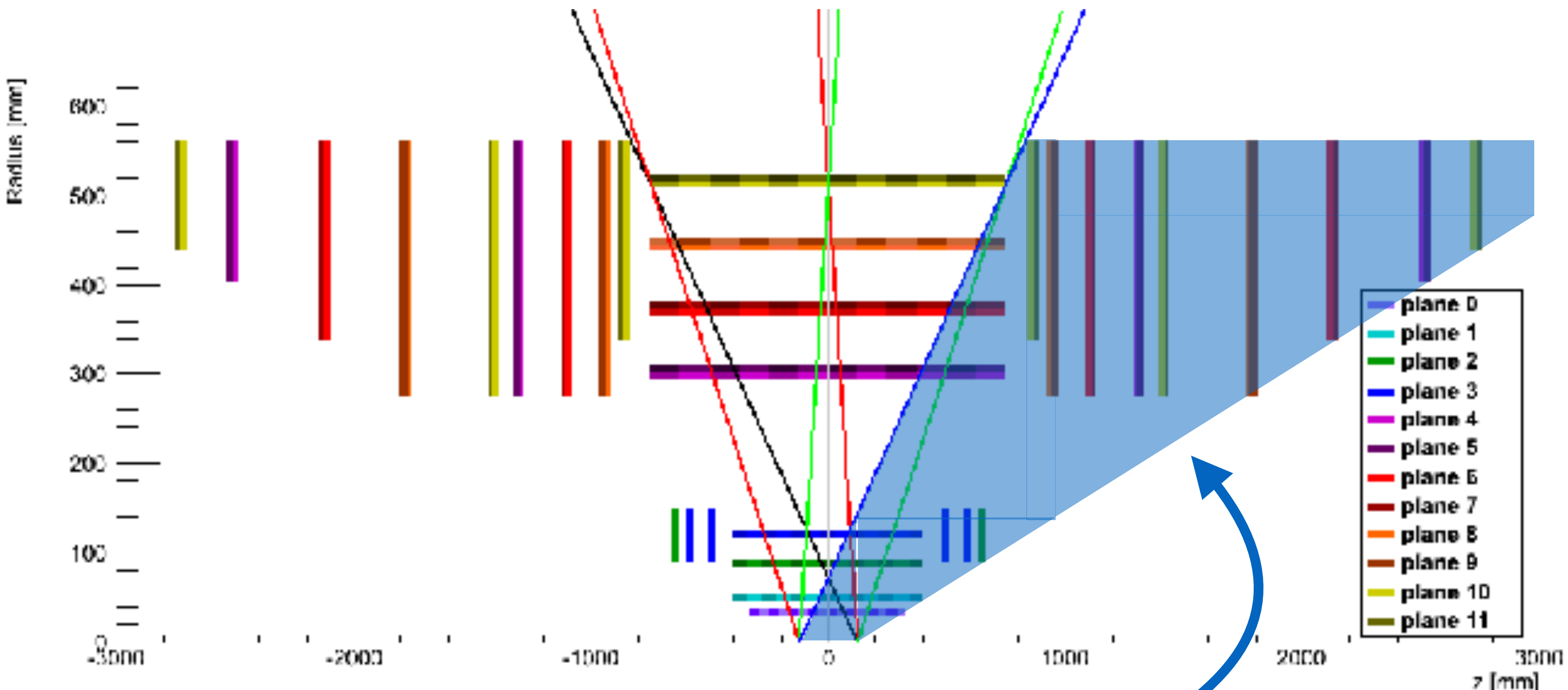

an endcap tower

per tower:
16.8M patterns
16k roads max
80k fits max

in total:
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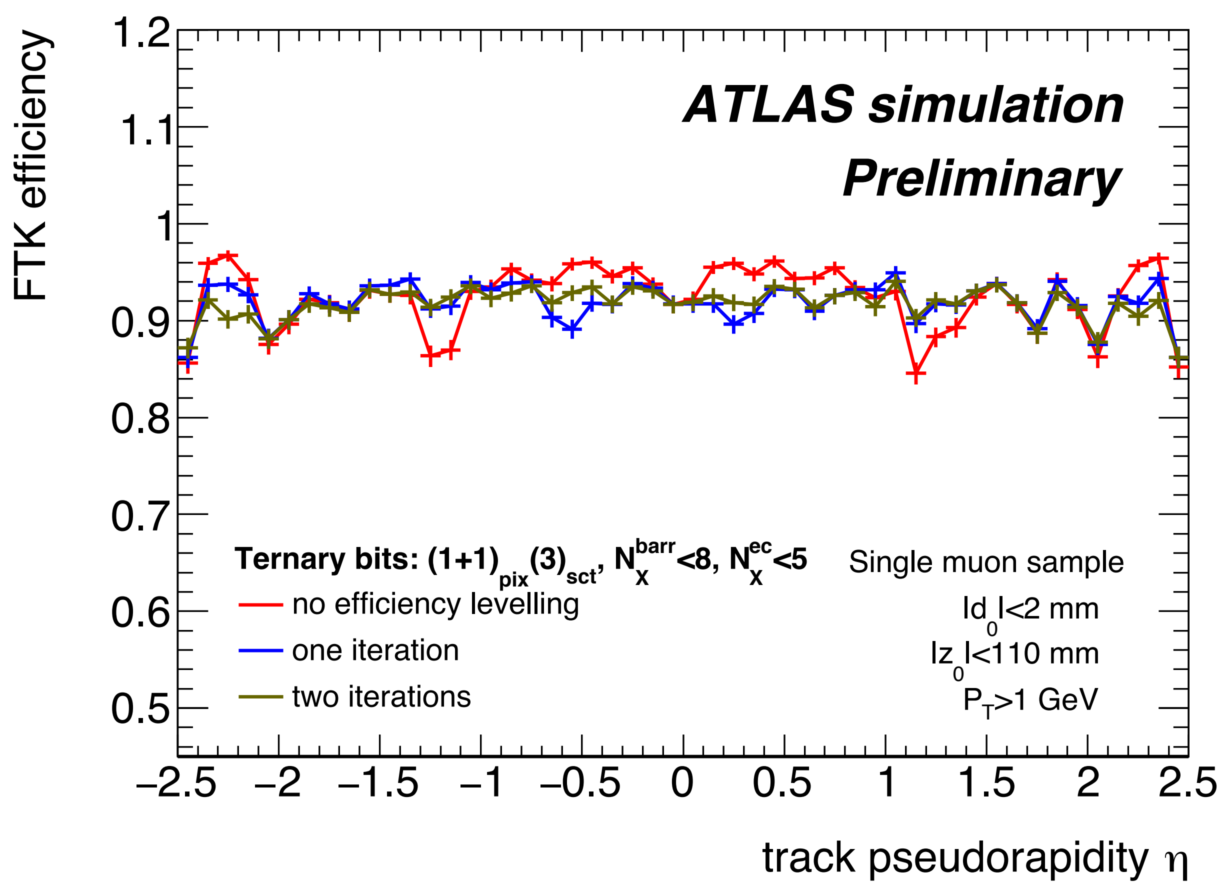
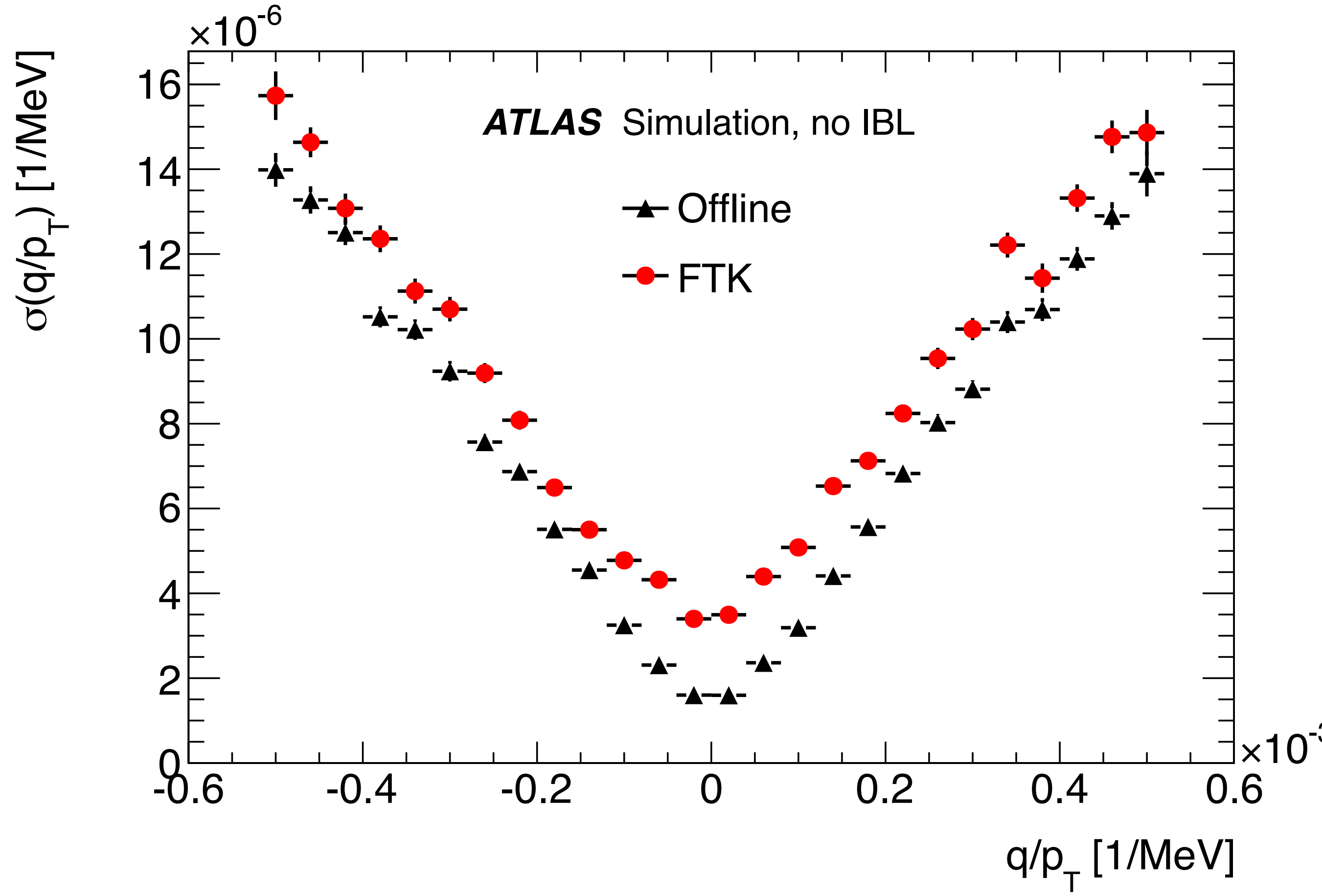
Towards physics goals w/ FTK

Develop banks and algorithms to meet physics goals, while respecting hardware constraints



FTK reaches near-offline efficiency (>90%) across the detector



Precise p_T measurement key for single leptons, MET soft term, all

Towards physics goals w/ FTK

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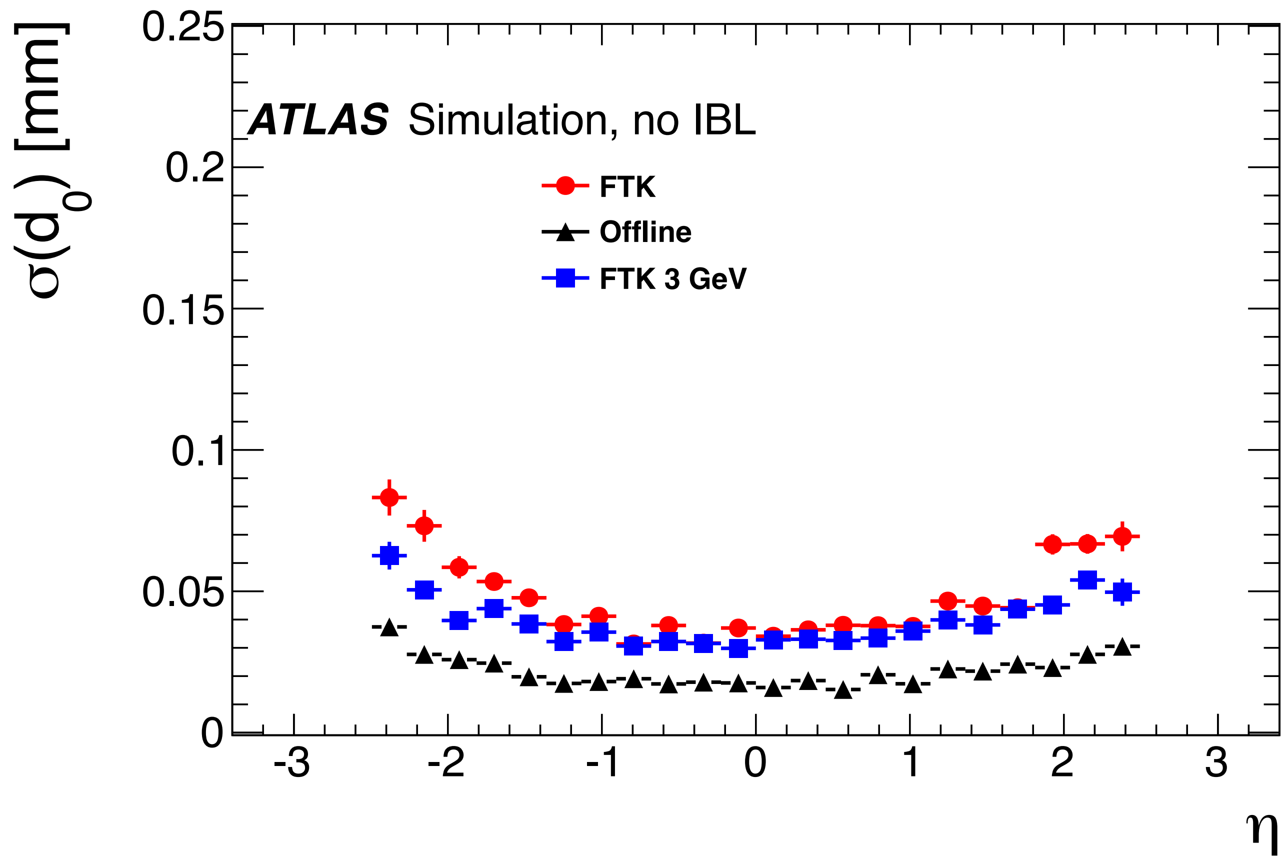

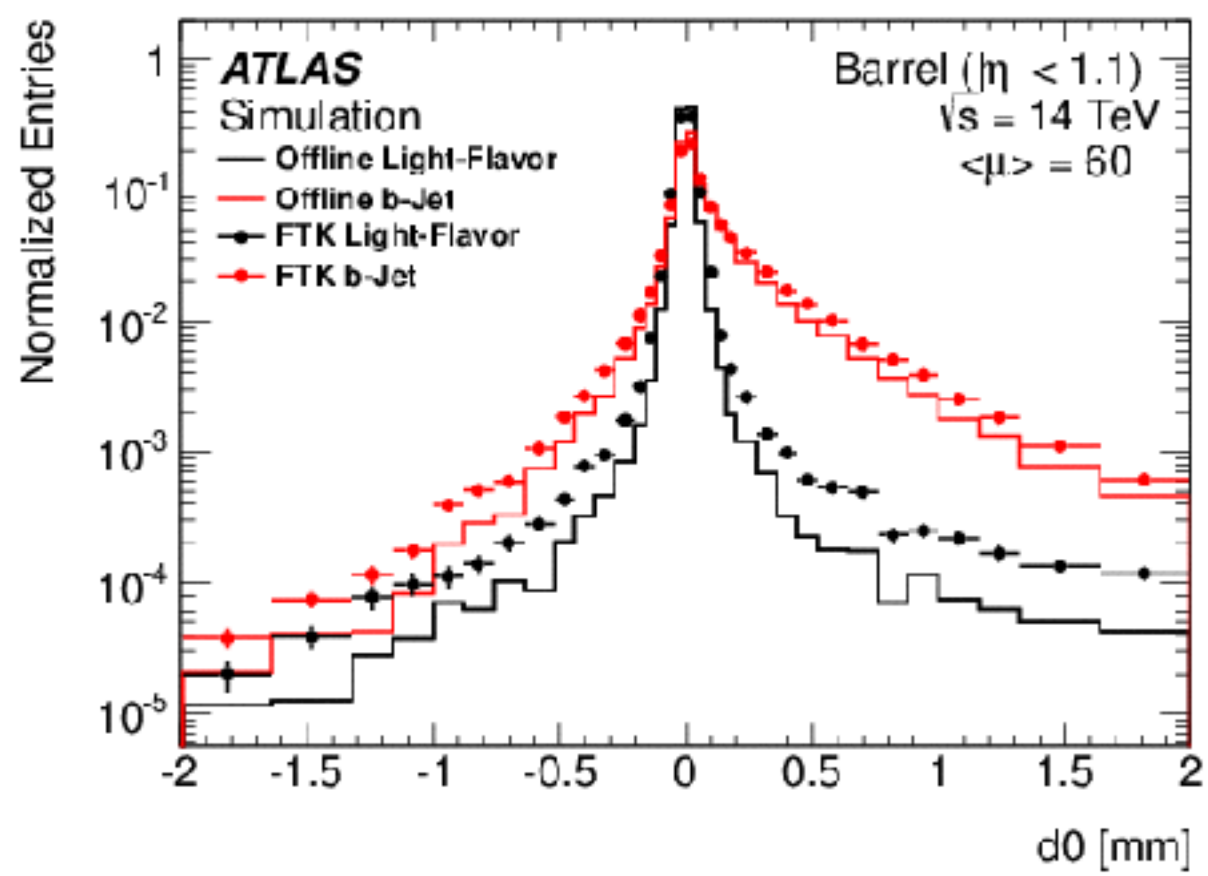

z_0, d_0 impact parameters critical for track-vertex association (MET, multijets) and displaced vertex ID

precise d_0 measurement crucial for b-tagging

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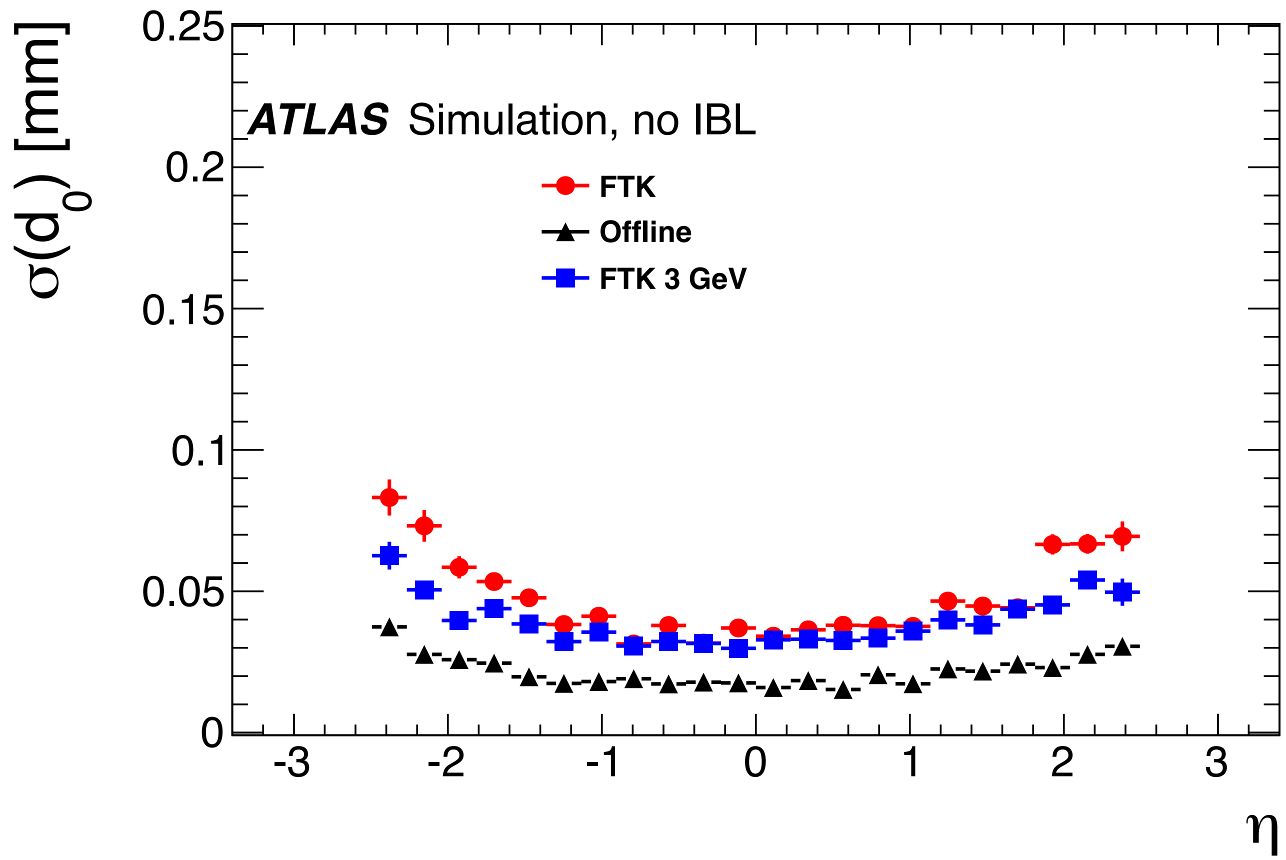

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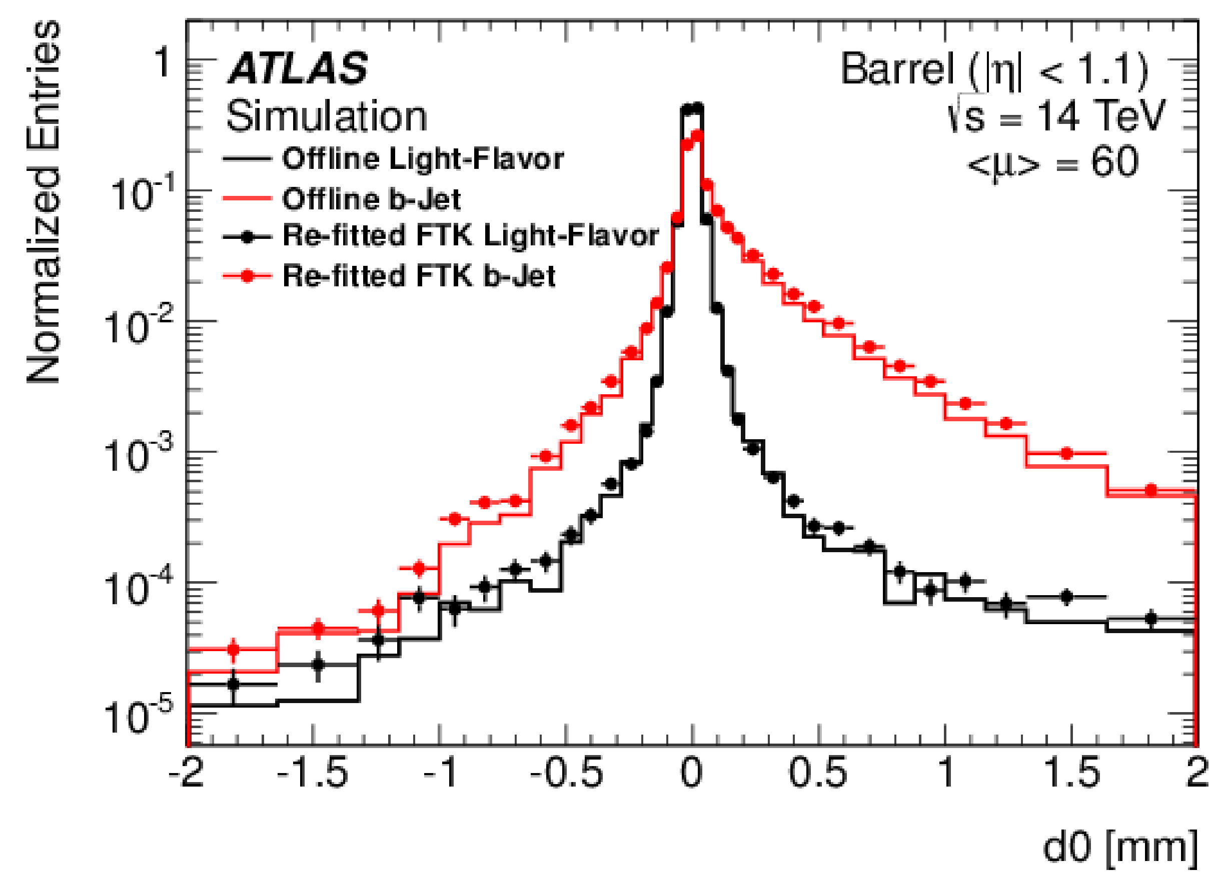
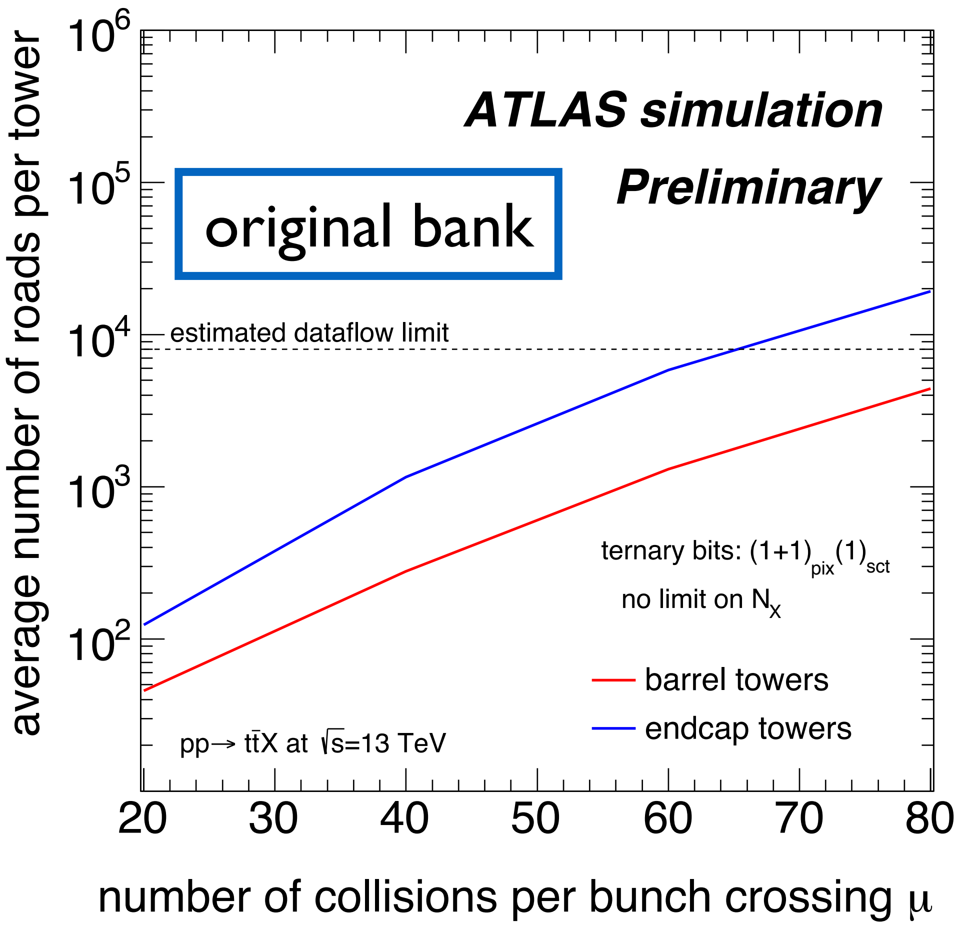
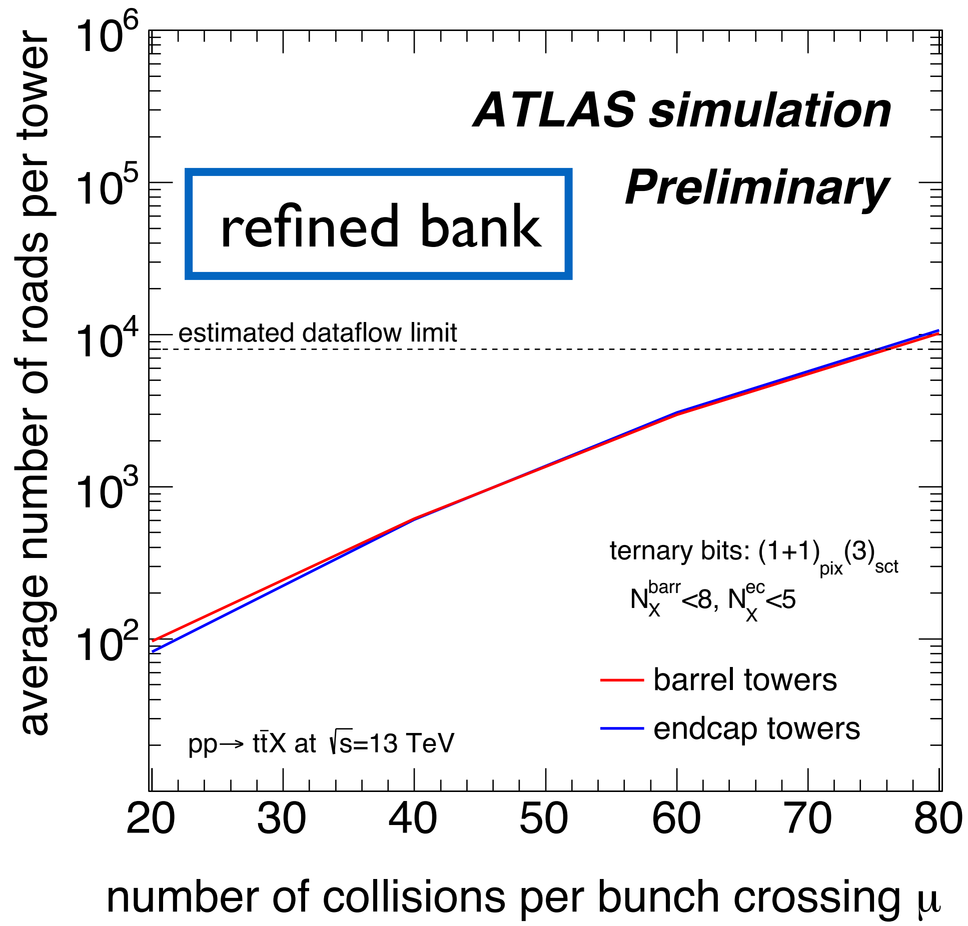


precise d_0 measurement crucial for b-tagging

can refit tracks if desired

Adapting to high-pileup environment





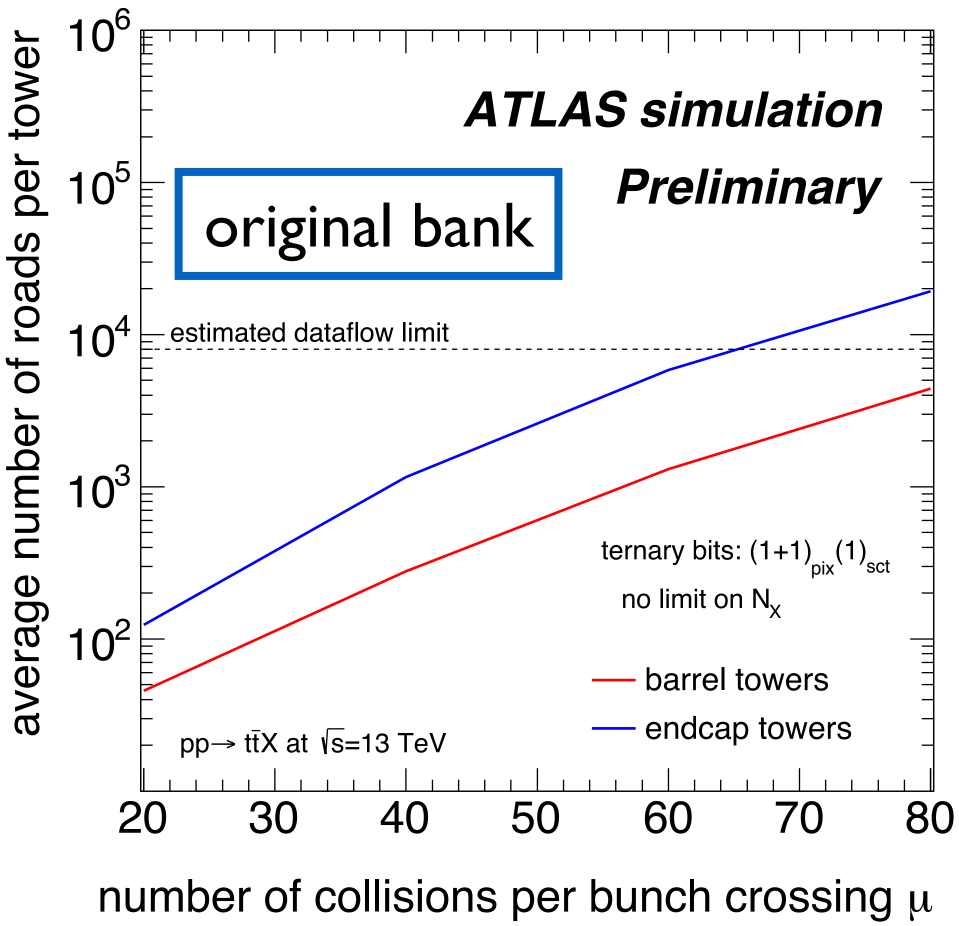
options to toggle in order to maintain performance with large pileup

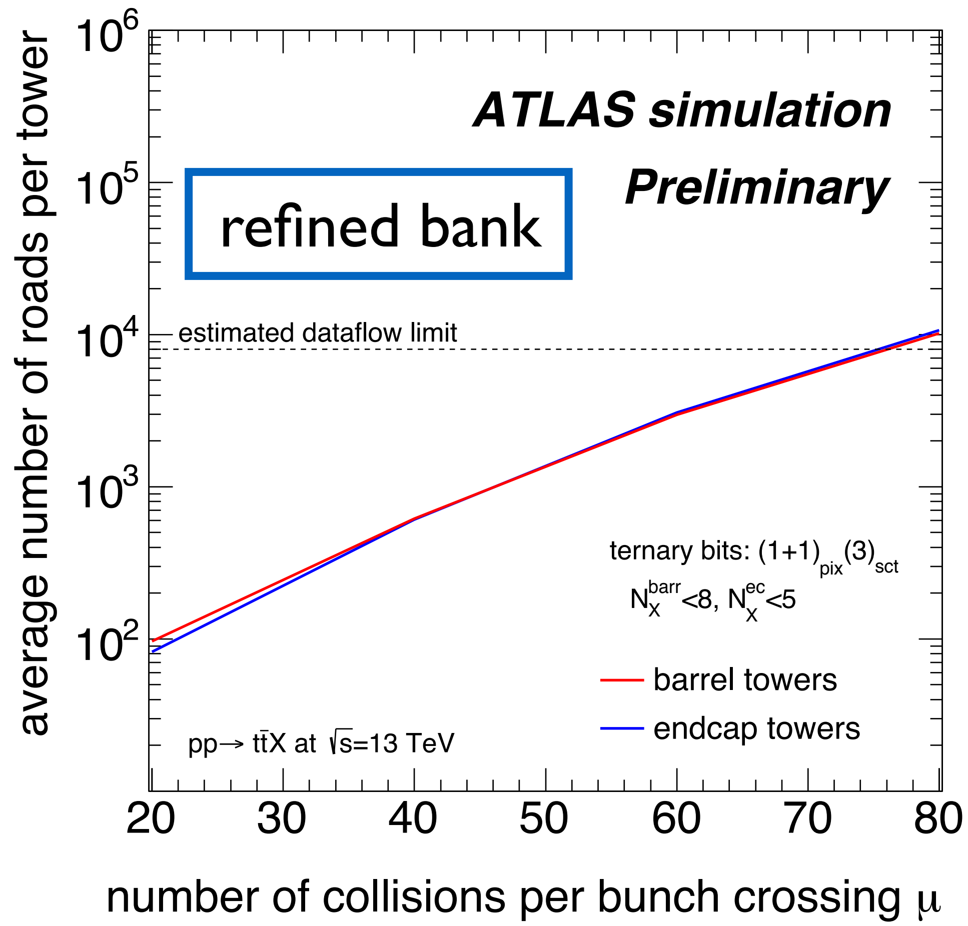
variable-sized patterns: number and regions of 'ternary bits'

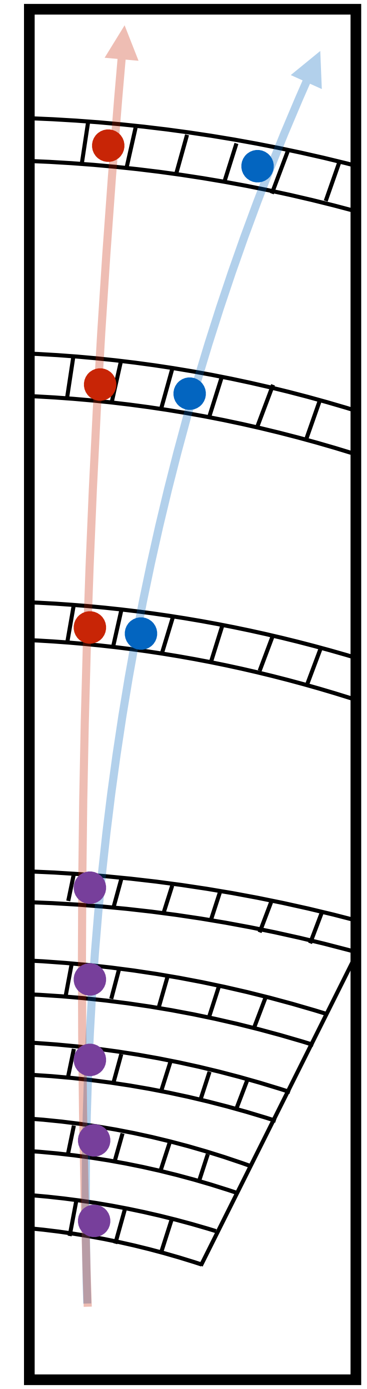
efficiency smoothing

pattern merging

Adapting to high-pileup environment







options to toggle in order to maintain performance with large pileup

variable-sized patterns: number and regions of 'ternary bits'

Two patterns?

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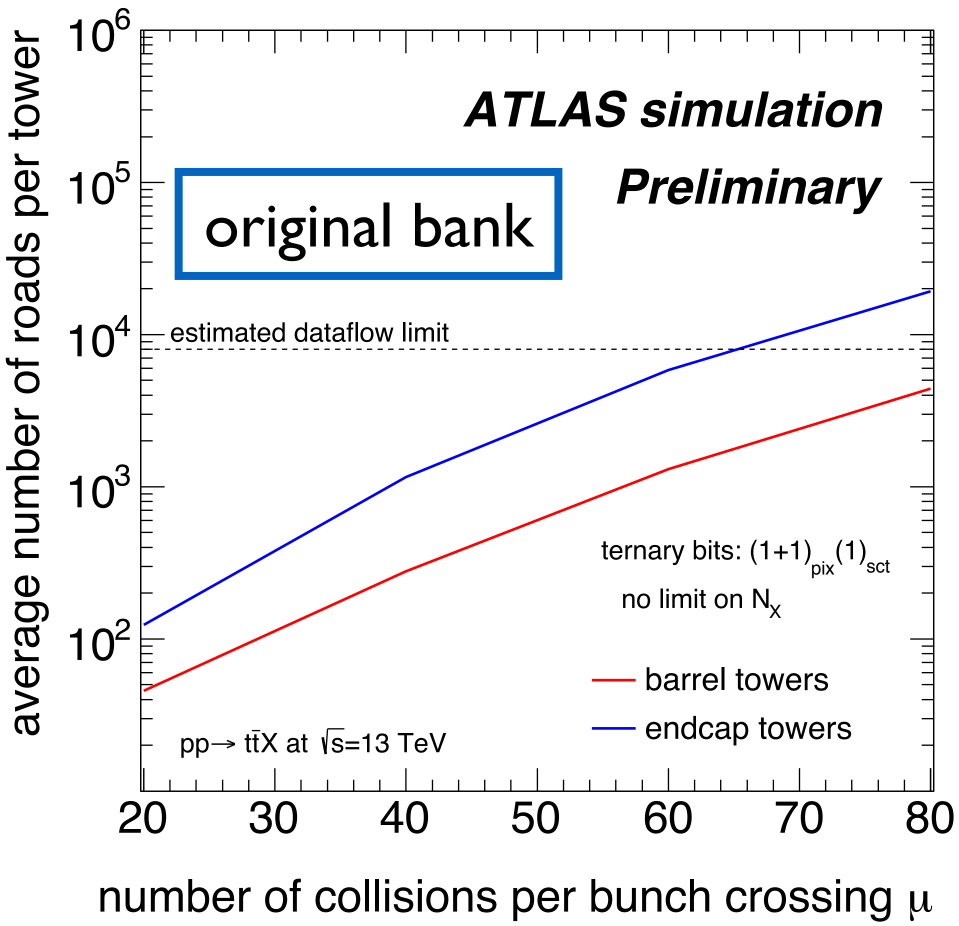
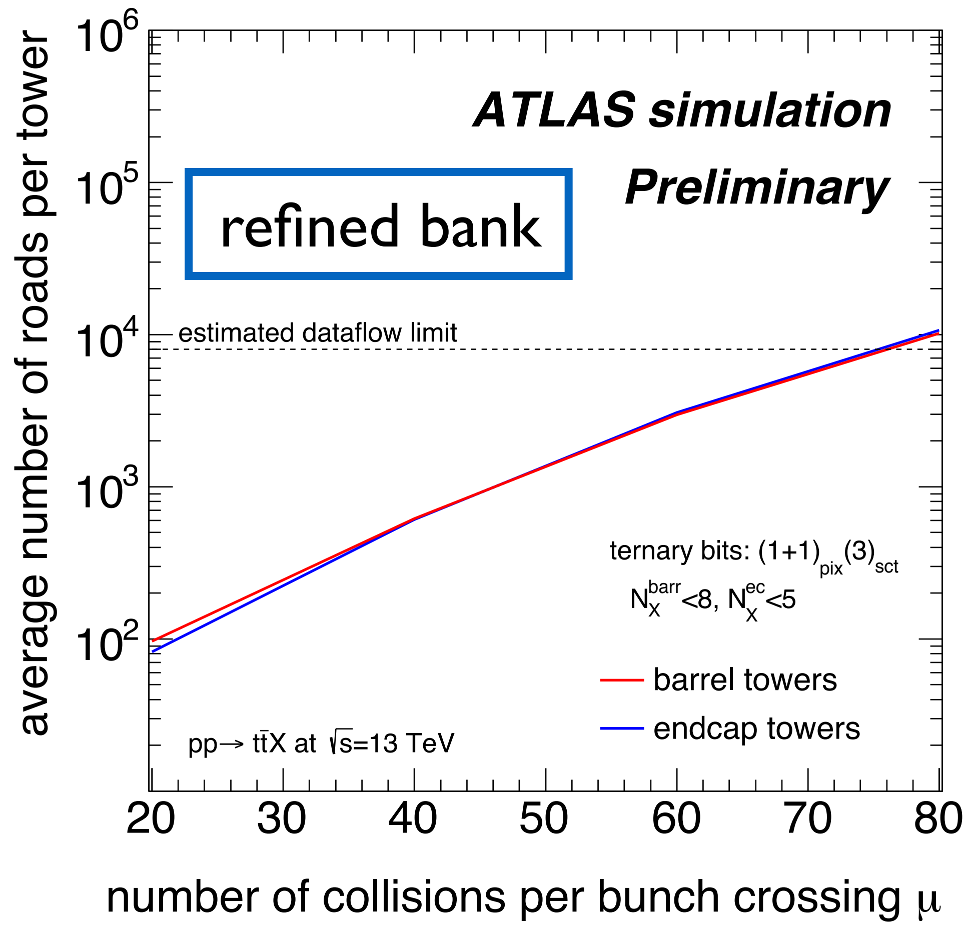
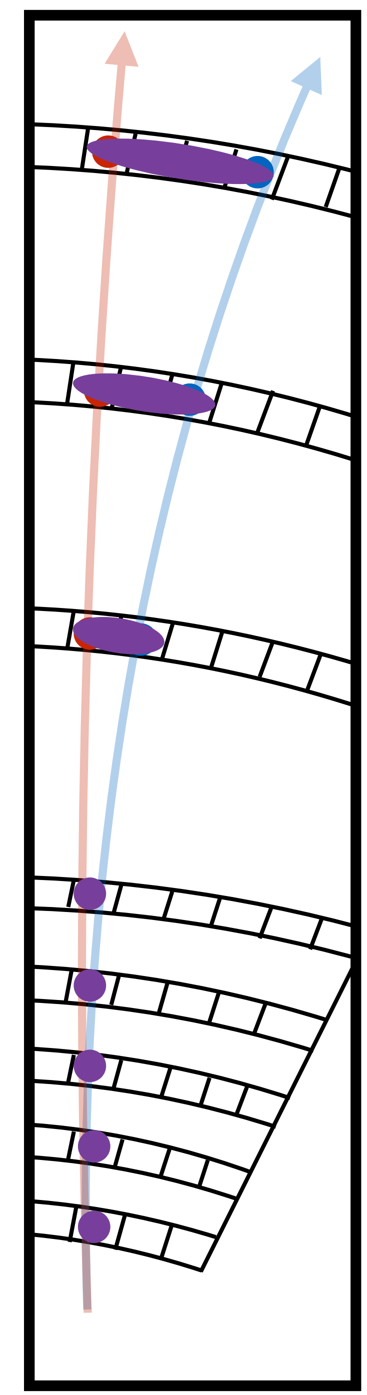
efficiency smoothing

pattern merging

Adapting to high-pileup environment







options to toggle in order to maintain performance with large pileup

variable-sized patterns: number and regions of 'ternary bits'

Or one?

efficiency smoothing

pattern merging

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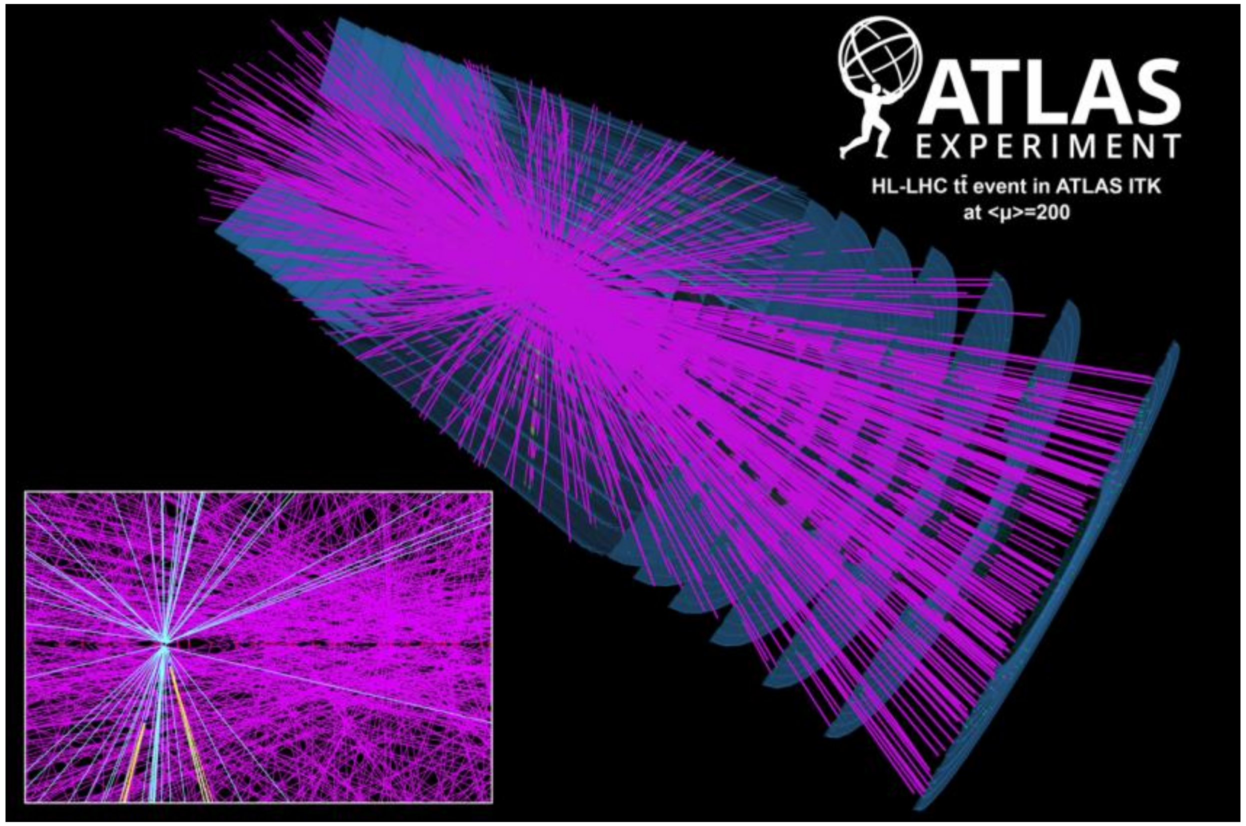
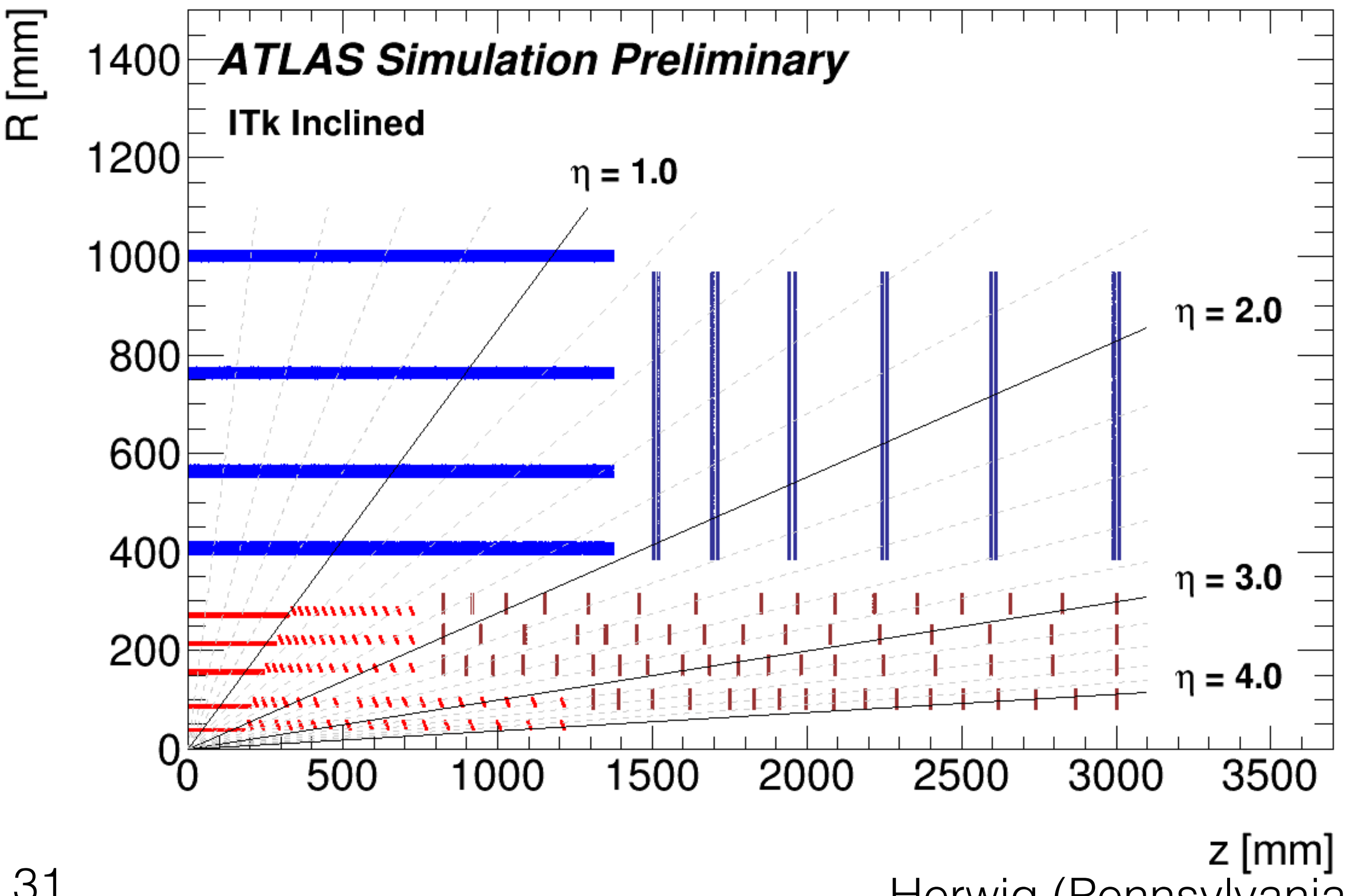
Towards the High-Lumi HLC (HL-LHC)

- Expect average of 200 collisions / crossing starting ~2026
  - Ultimately will collect 3000/fb of data (had 30/fb in 2016 !)
- ATLAS detector being upgraded to take full advantage
  - new all-silicon tracker, extending to very forward region
- Track trigger essential to identifying activity from the primary vertex





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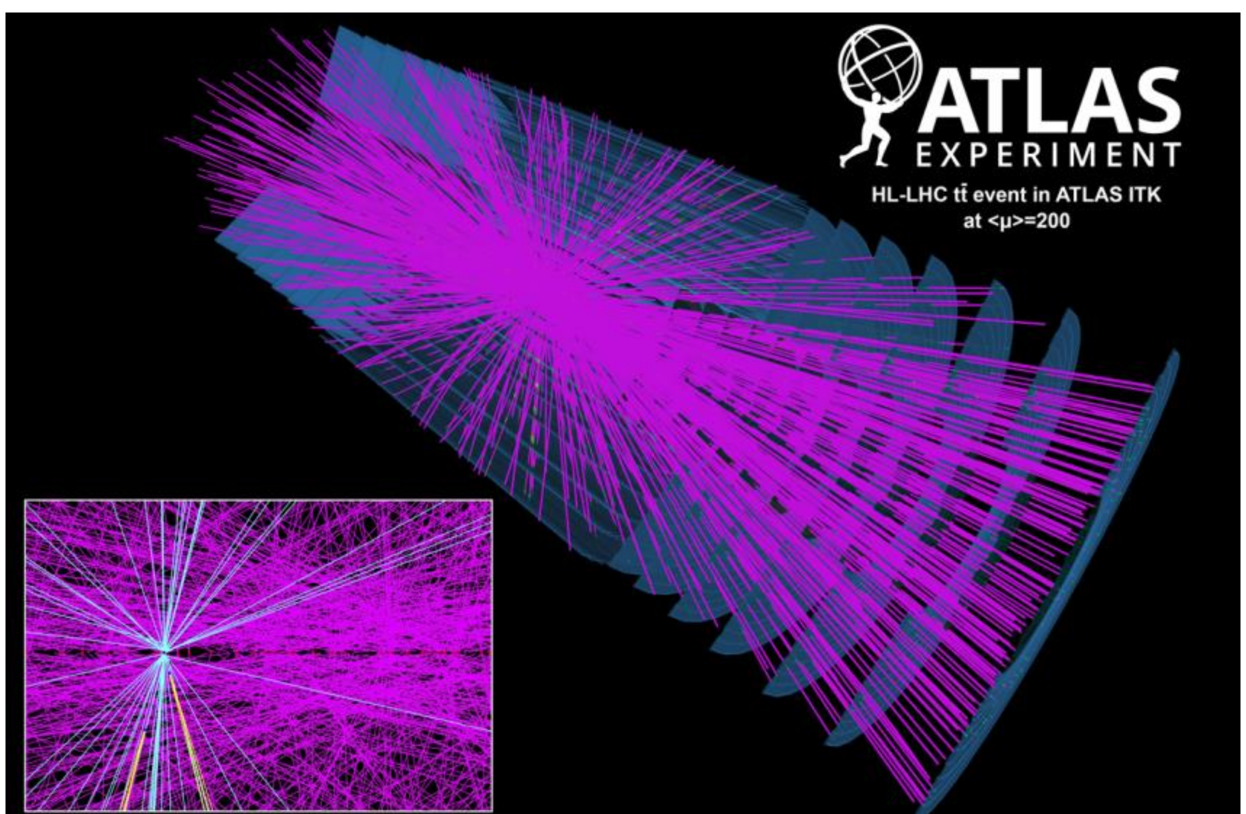

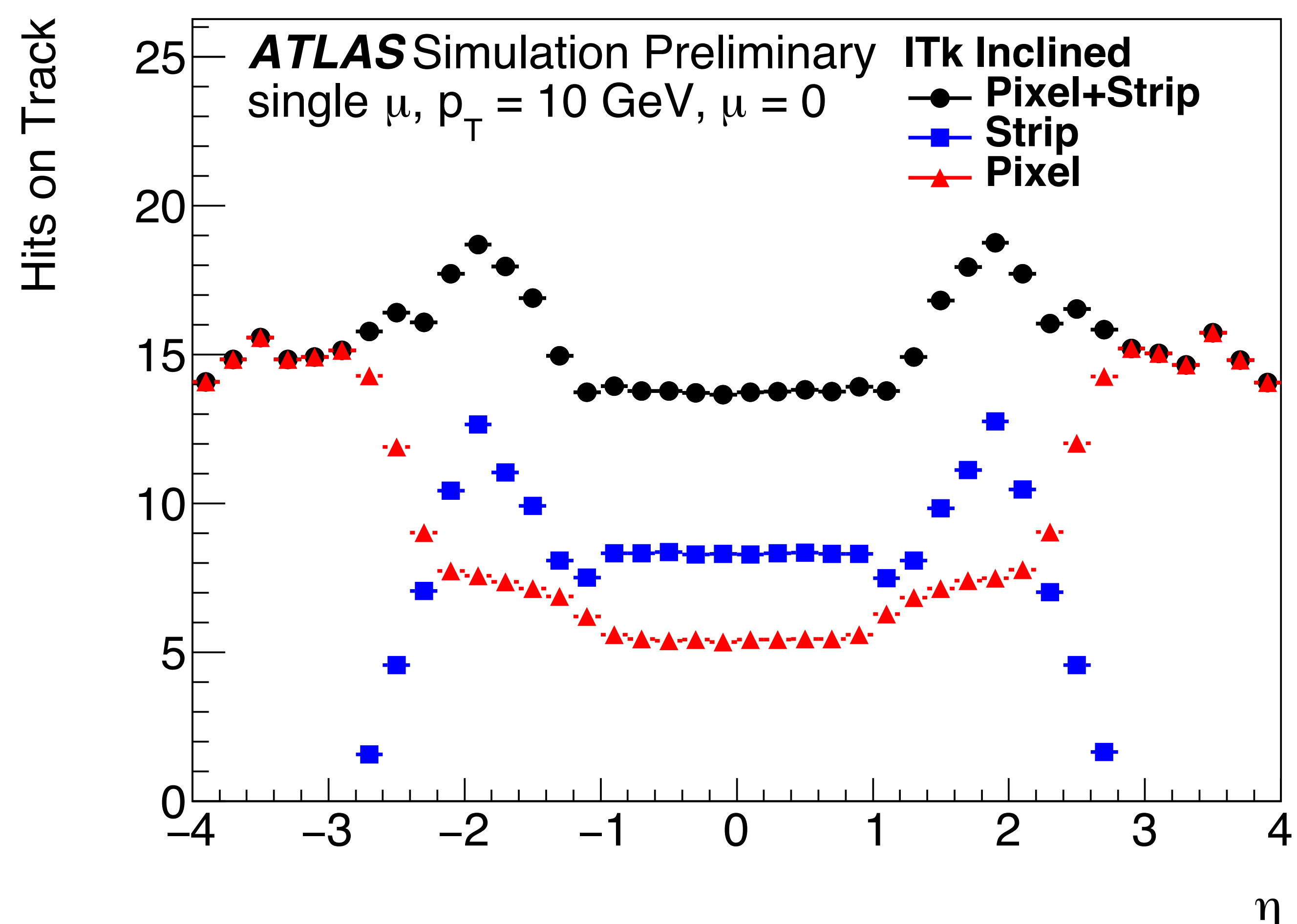

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Phase-II trigger designs

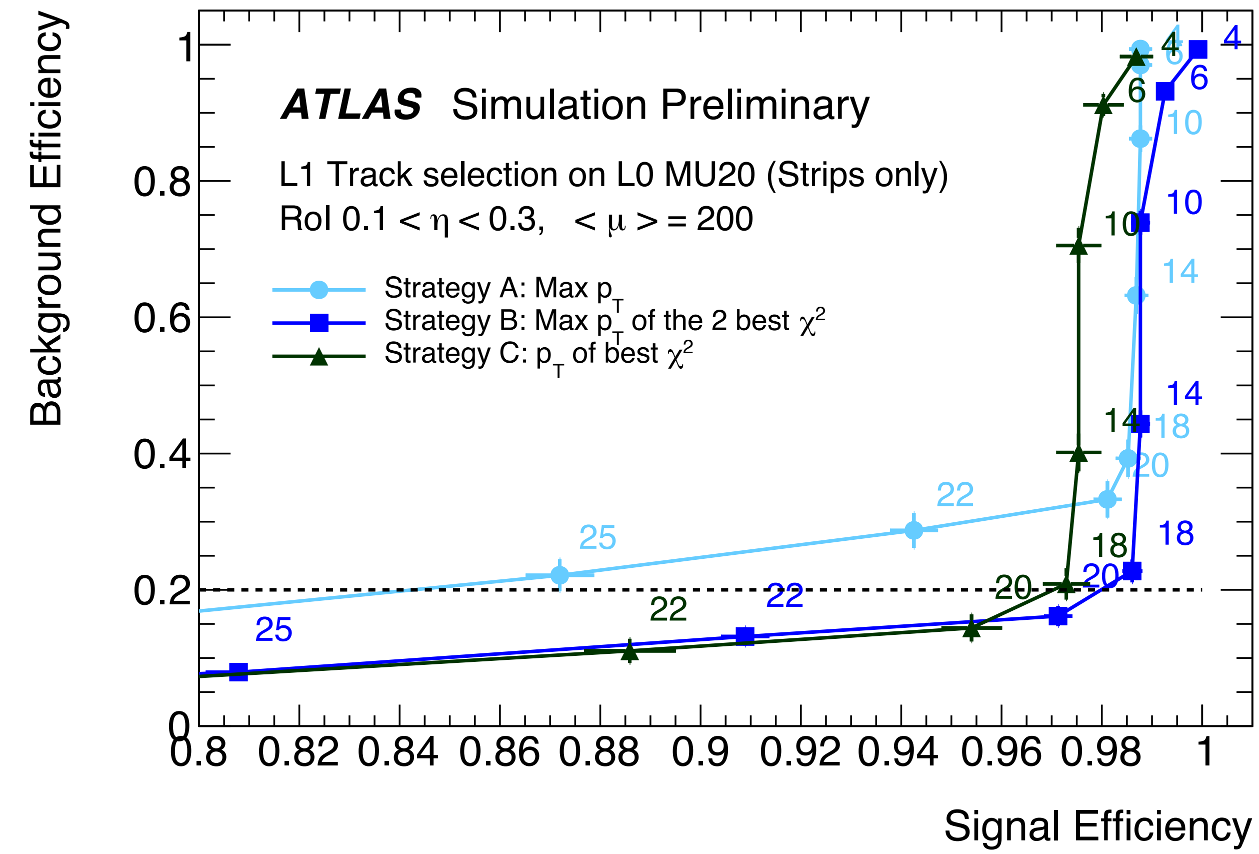
- Investigating new track-trigger based on the AM chip concept
  - Must handle tracks up to η=4 and a 15cm beamspot
- Nominal design is a 2-level system w/ hardware tracking
  - Potential to evolve to a 3-level system
  - Some choices remain; progressing towards a design

3-level system				
level	output rate	track params		name
L0	4 MHz	-	-	-
L1	400 kHz	regional	4 GeV	L1track
HLT	10 kHz	full-scan	1 GeV	FTK++

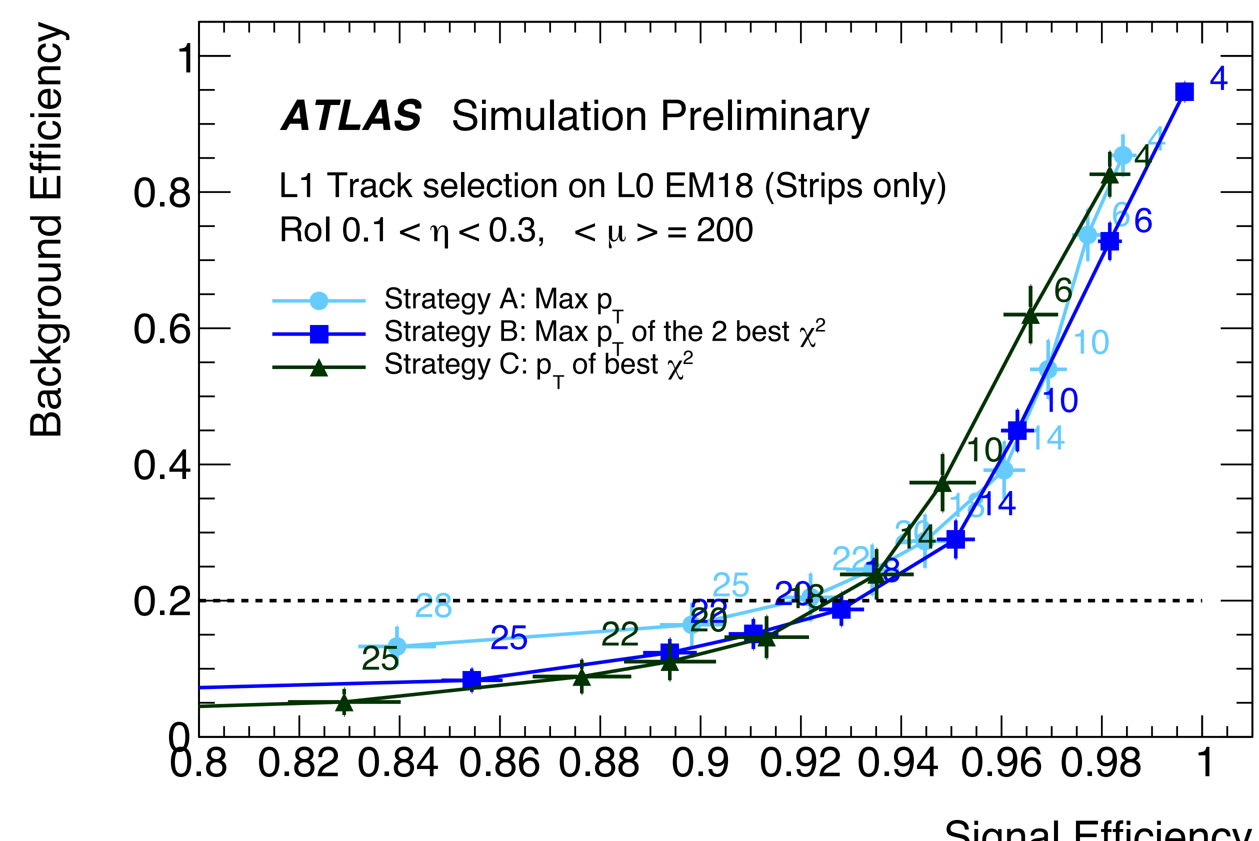
2-level system				
level	output rate	track params		name
L0	1 MHz	-	-	-
HLT	10 kHz	regional	2 GeV	EFtrack
		full	1 GeV	FTK++

L1 track studies

- L1track studies produced banks of 4 GeV tracks in 0.2x0.2 ROIs
- Studied "strips+pixel" = "8+0" and "7+1" layout
- Track p_T requirement targets 5x rate reduction



Detector layers	q/p_T [e/GeV]	$\phi[rad]$	η	d_0 [mm]	z_0 [mm]
Strip layers only	0.003	0.001	0.002	0.3	1.7
Strip + 1 pixel layer	0.003	0.001	0.001	0.2	0.3



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- Pixels layer usage improves z_0 by 1.7→0.3mm
- z_0 goal set by multijet triggers
  - vertex-matching reduces rate from coincident dijets

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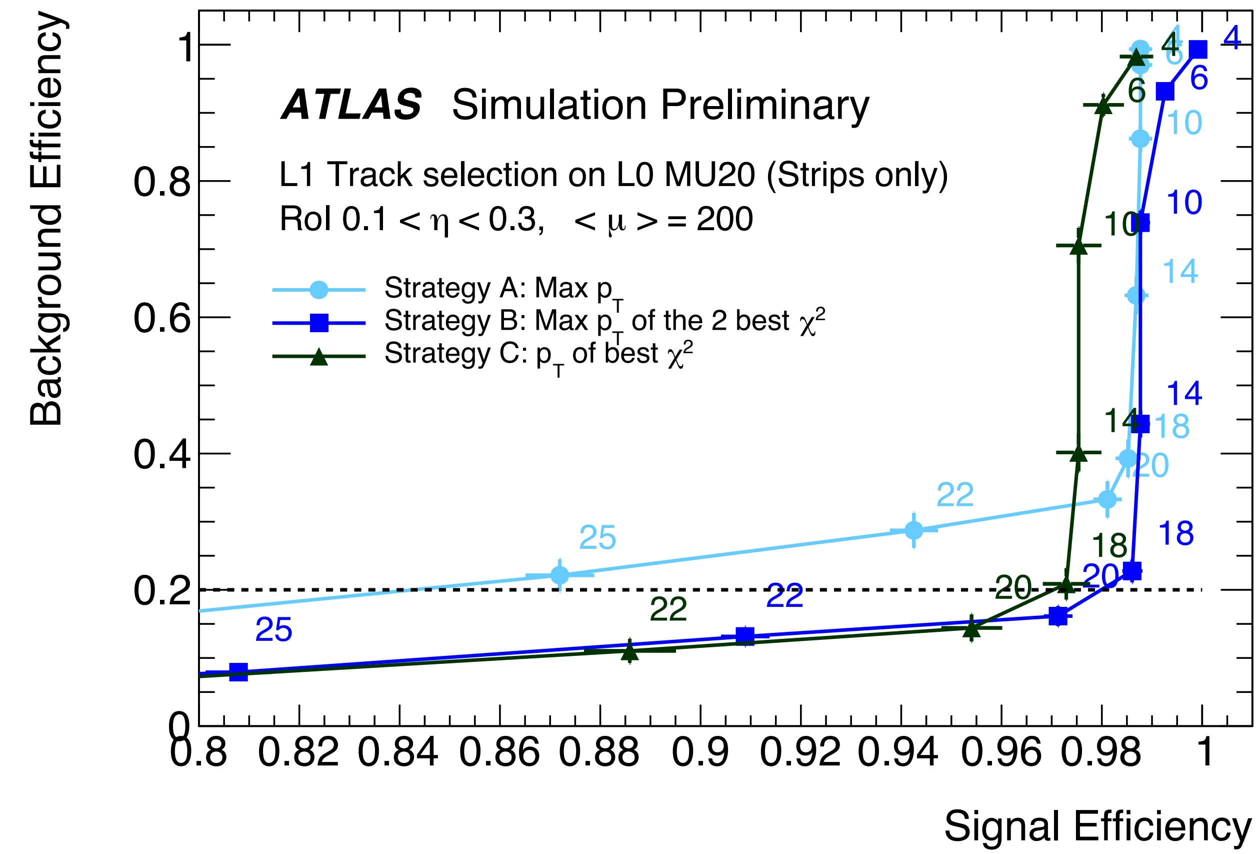

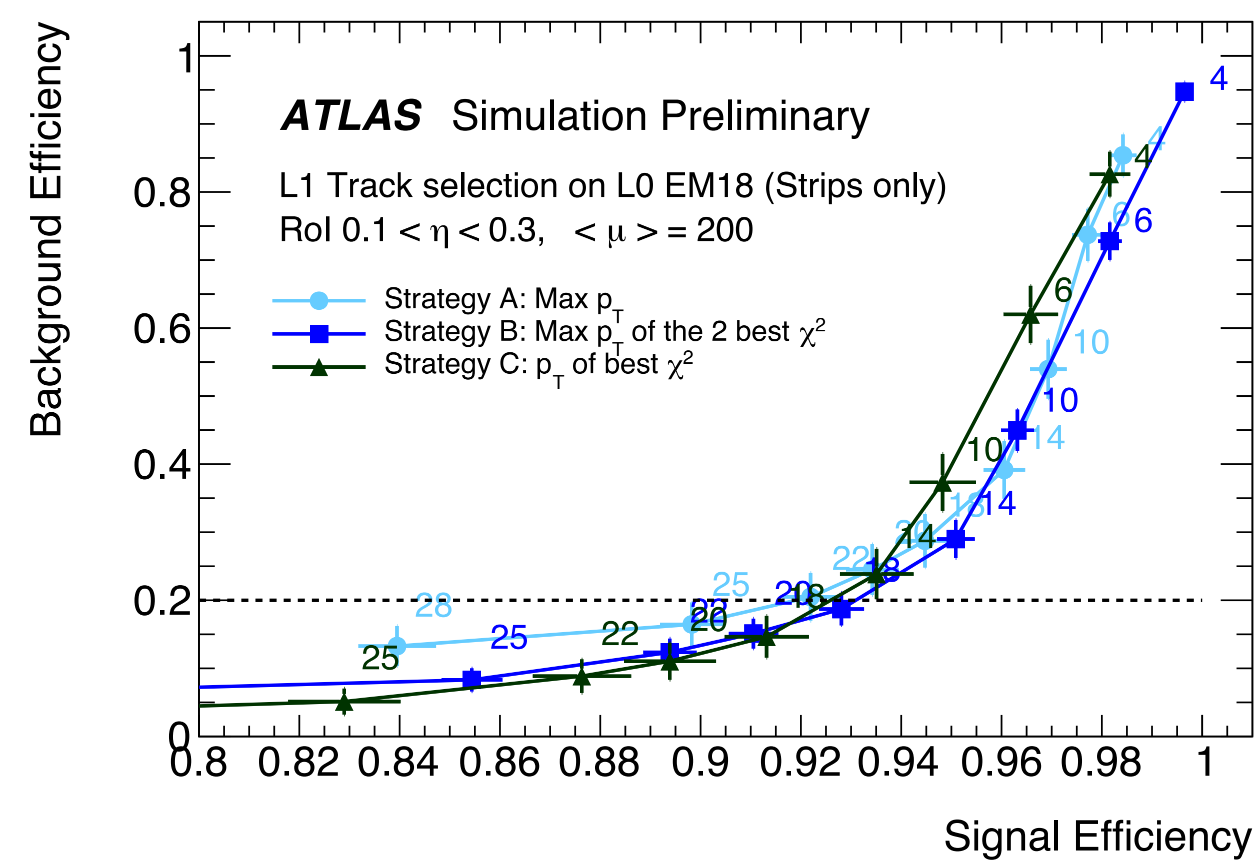

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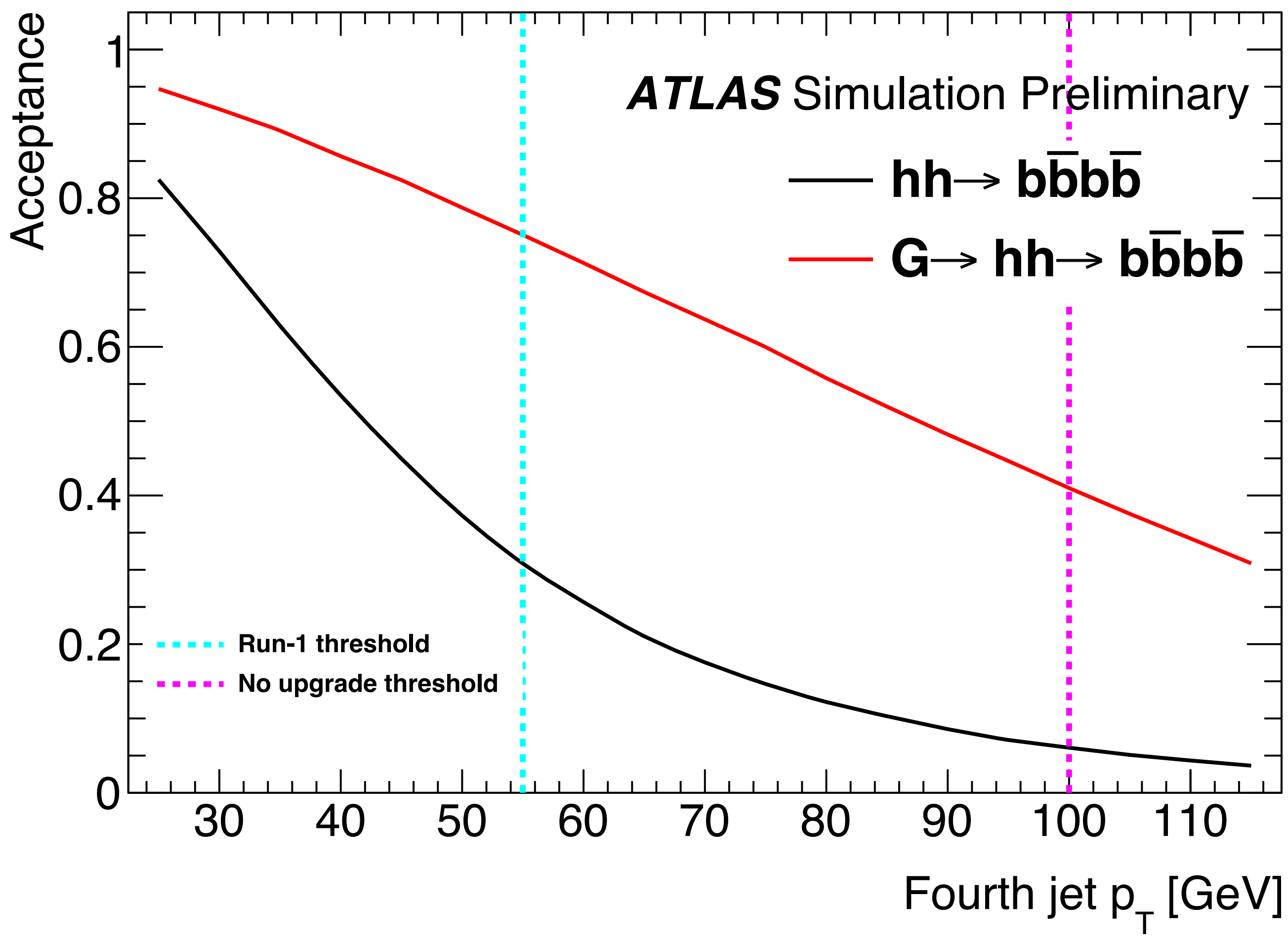
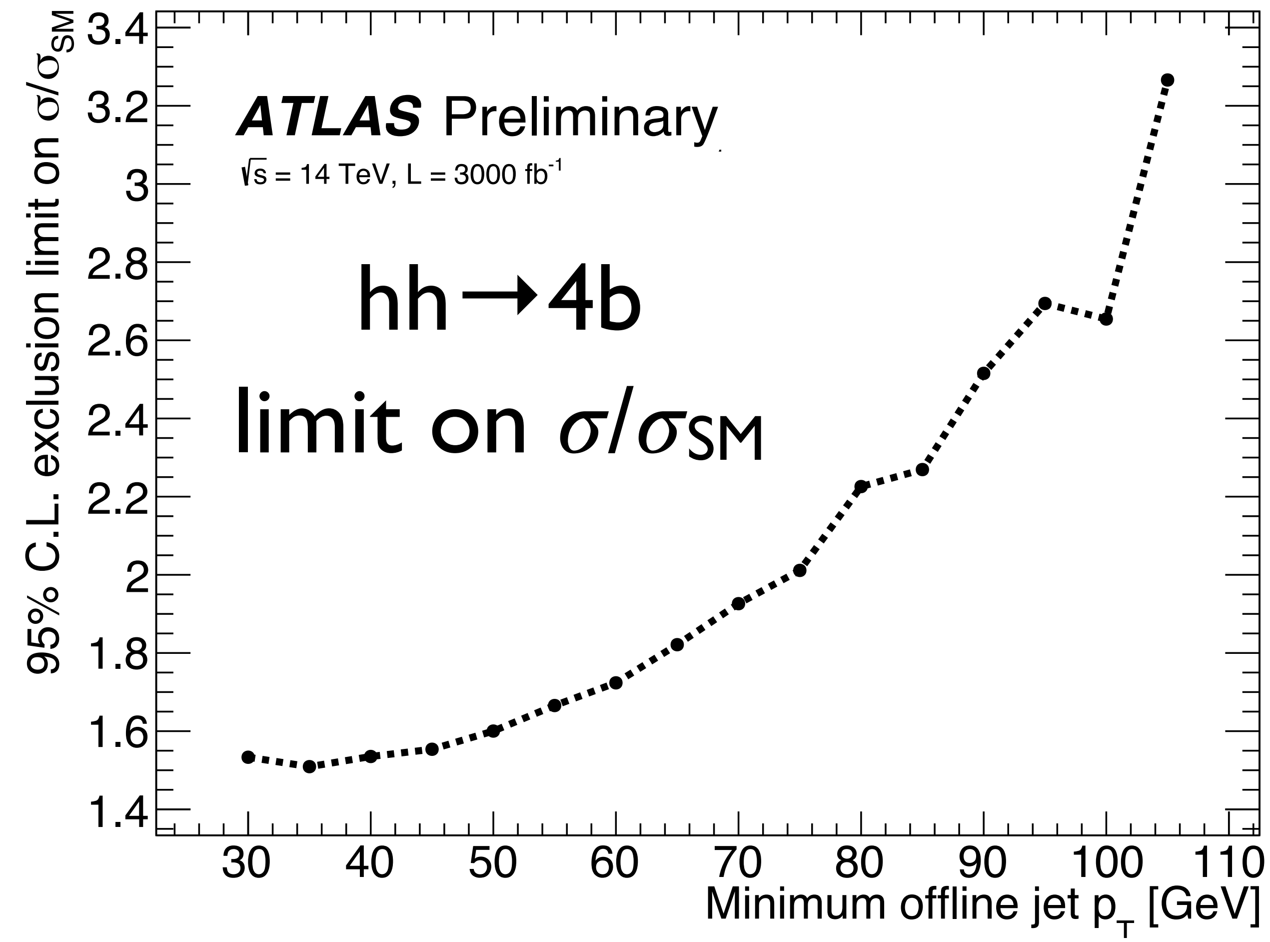
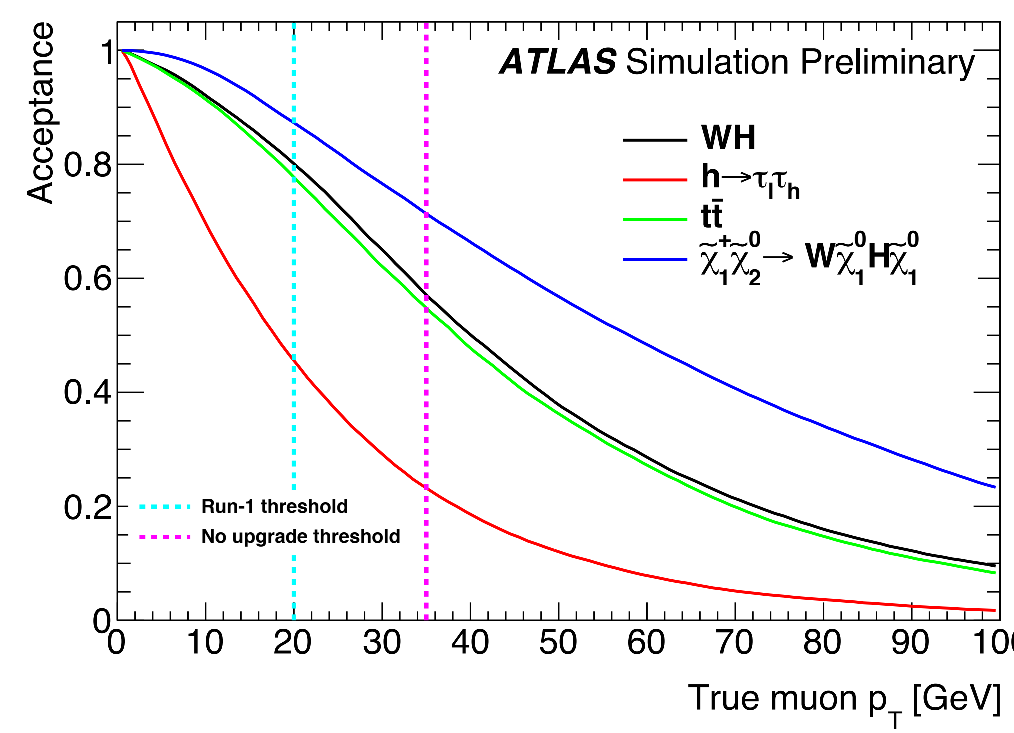
Much work to be done!





Our sensitivity to benchmark HL-LHC signatures relies on aggressive track triggers!



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Conclusions

Hardware track triggers offer significant improvements over traditional systems for a variety of physics signatures

Their utility increases significantly with upgraded machine luminosity

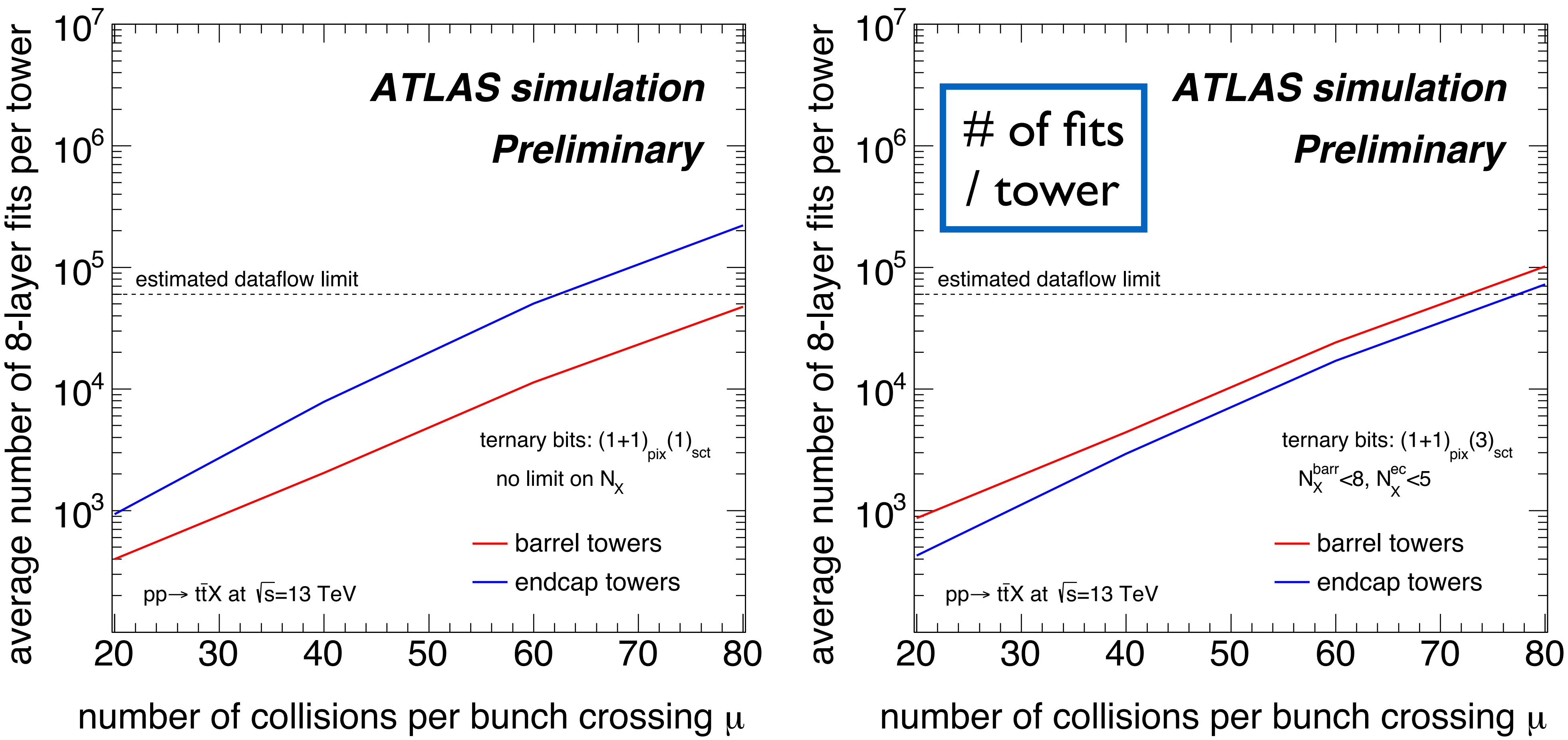
ATLAS FTK is running in "commissioning mode" for 2017 — crucial as the LHC continues to break lumi records

Track triggers will be central to the Phase-II TDAQ system for HL-LHC

Crucial to enable everything from benchmark physics searches to new ideas, yet-to-be thought up!

Backup

Adapting to high-pileup environment



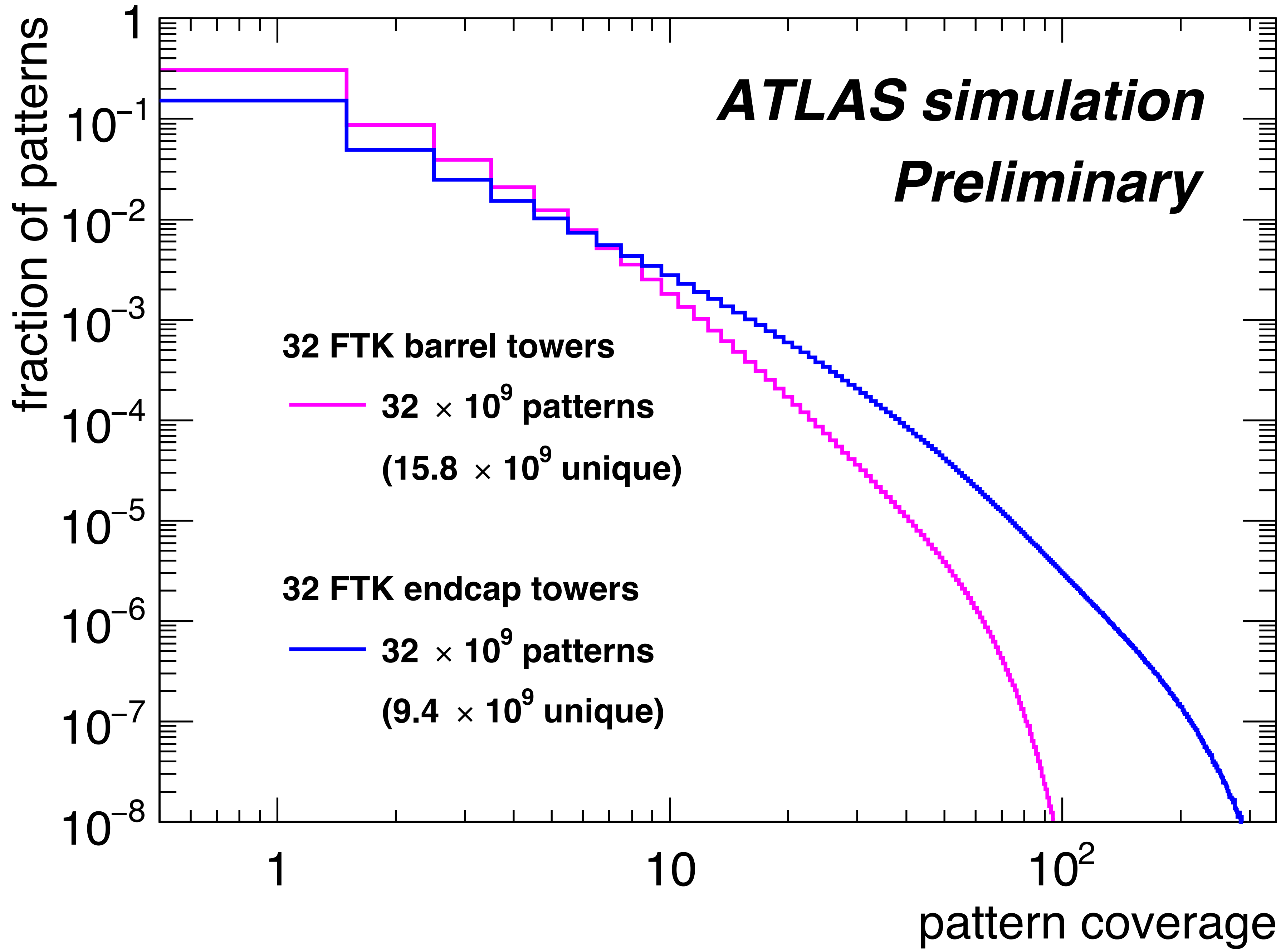
options to toggle in order to maintain performance with large pileup

variable-sized patterns: number and regions of 'ternary bits'

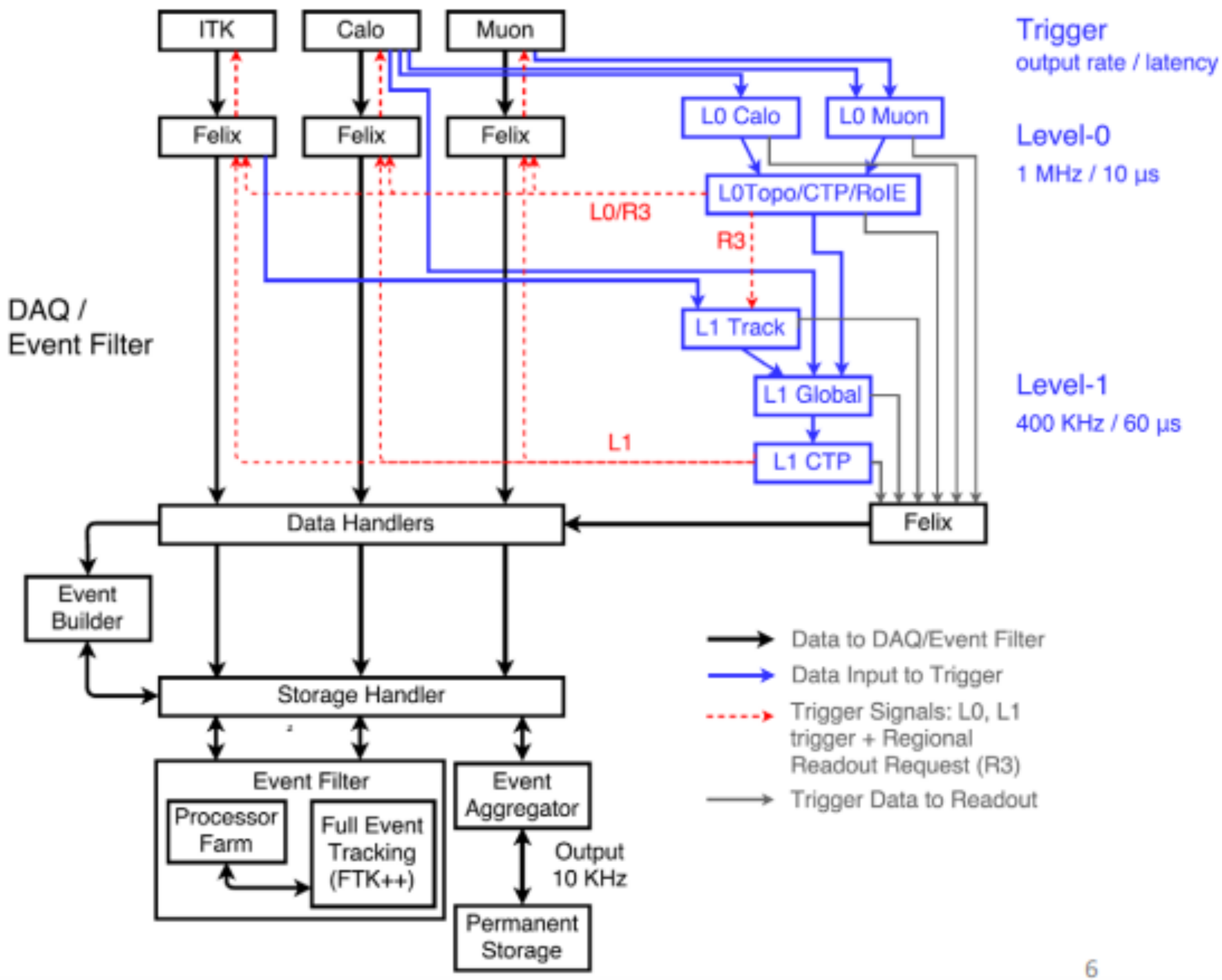
efficiency smoothing

pattern merging

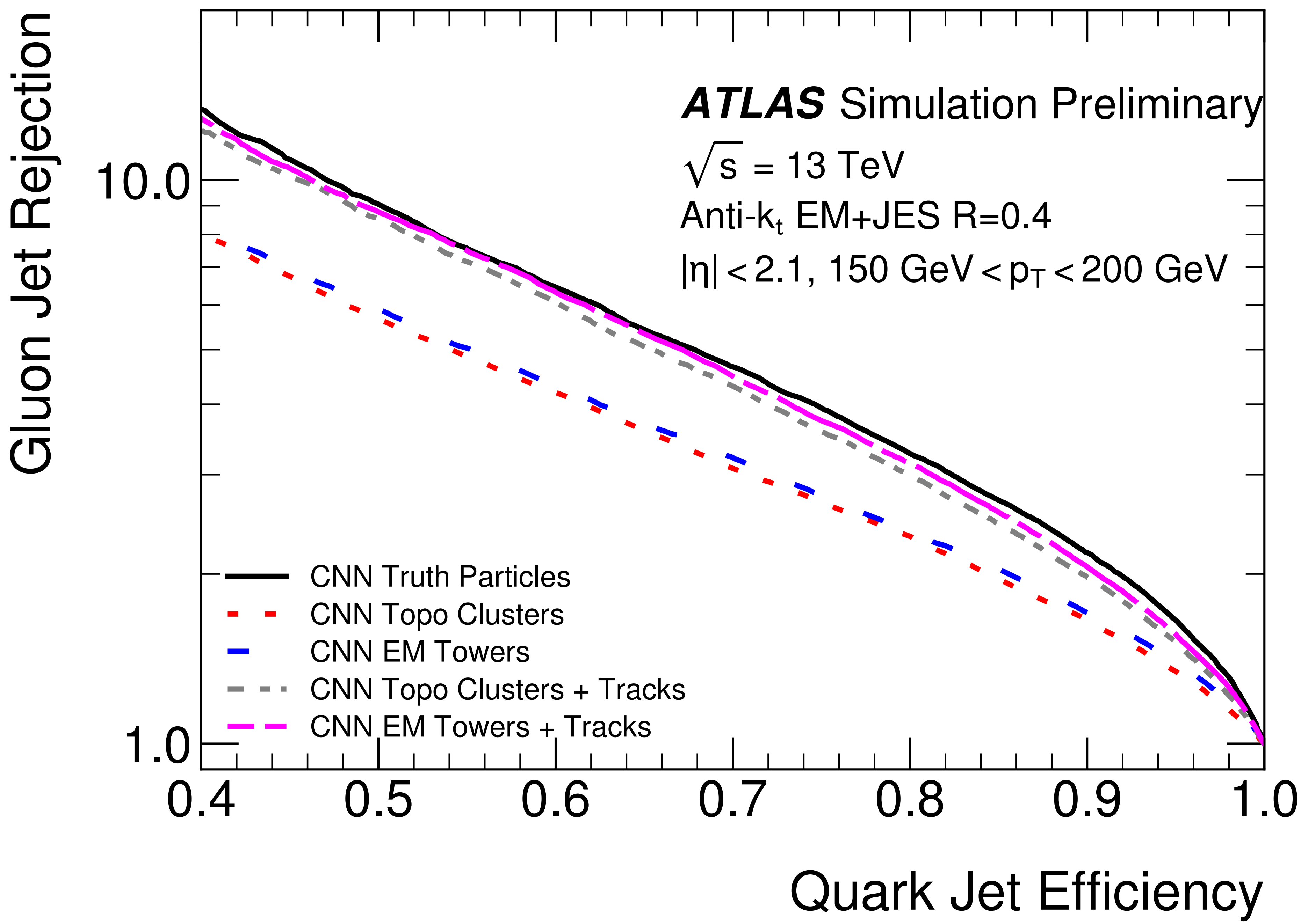
FTK track quality



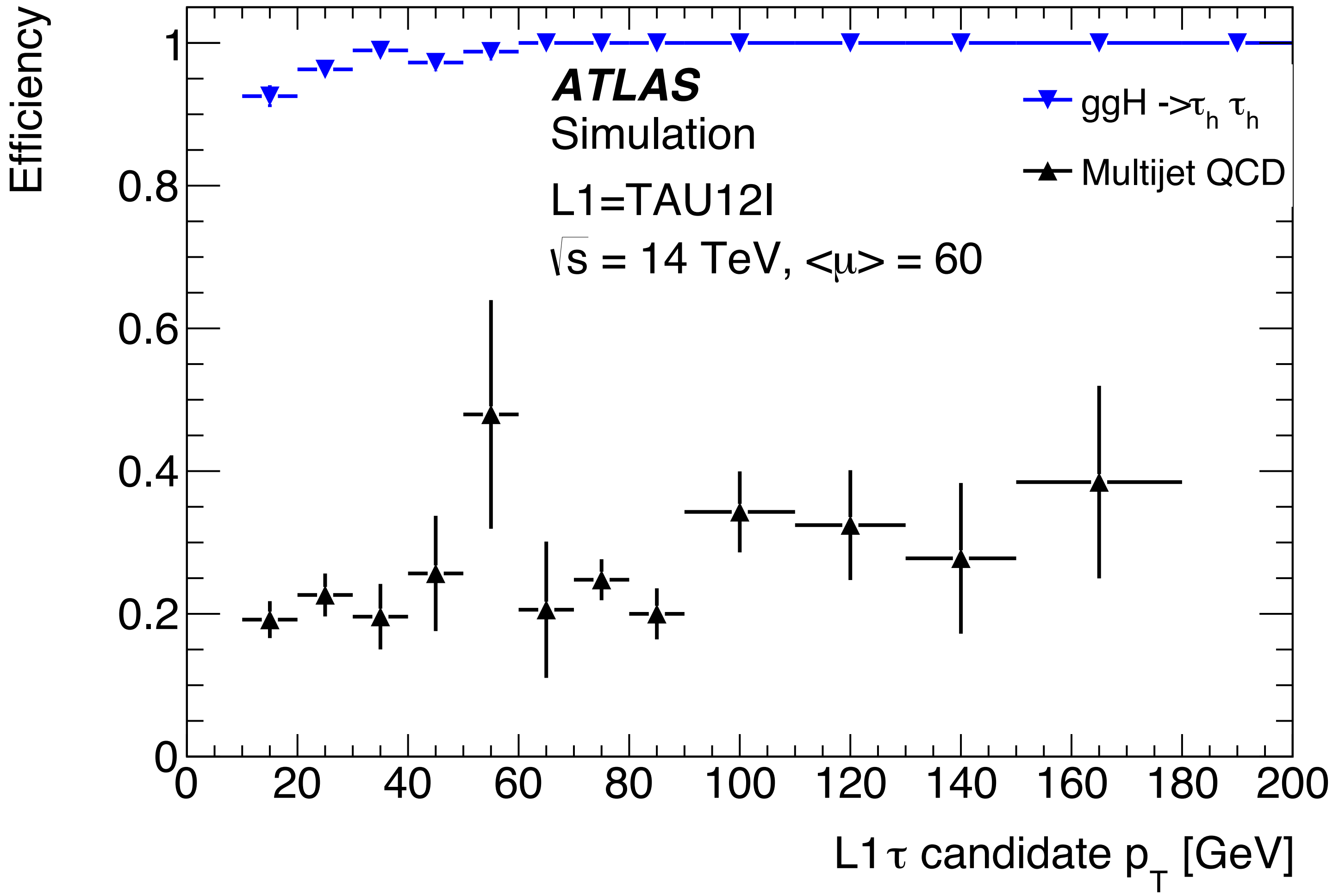
Potential Phase-II TDAQ schematic

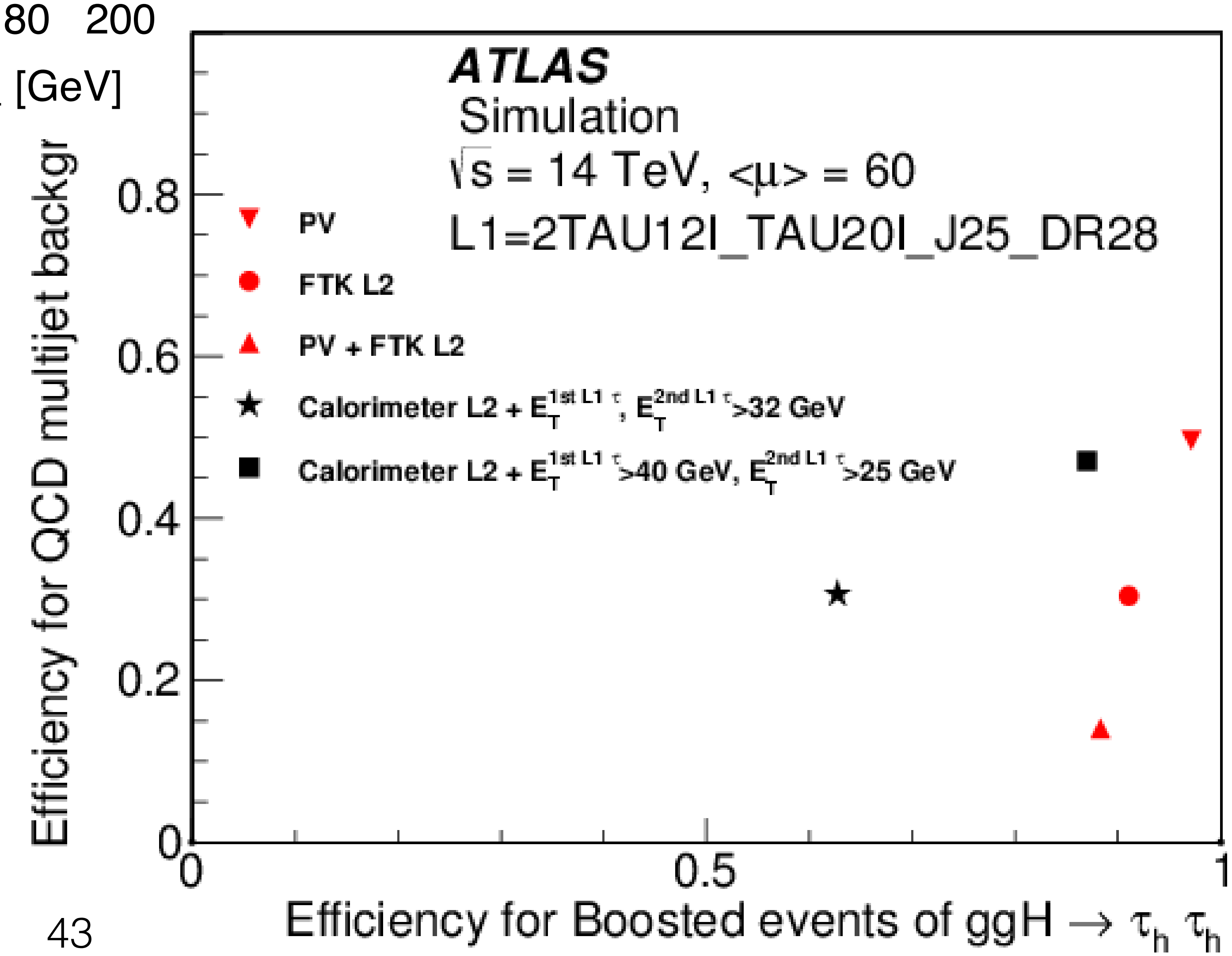


Physics motivations for track triggers

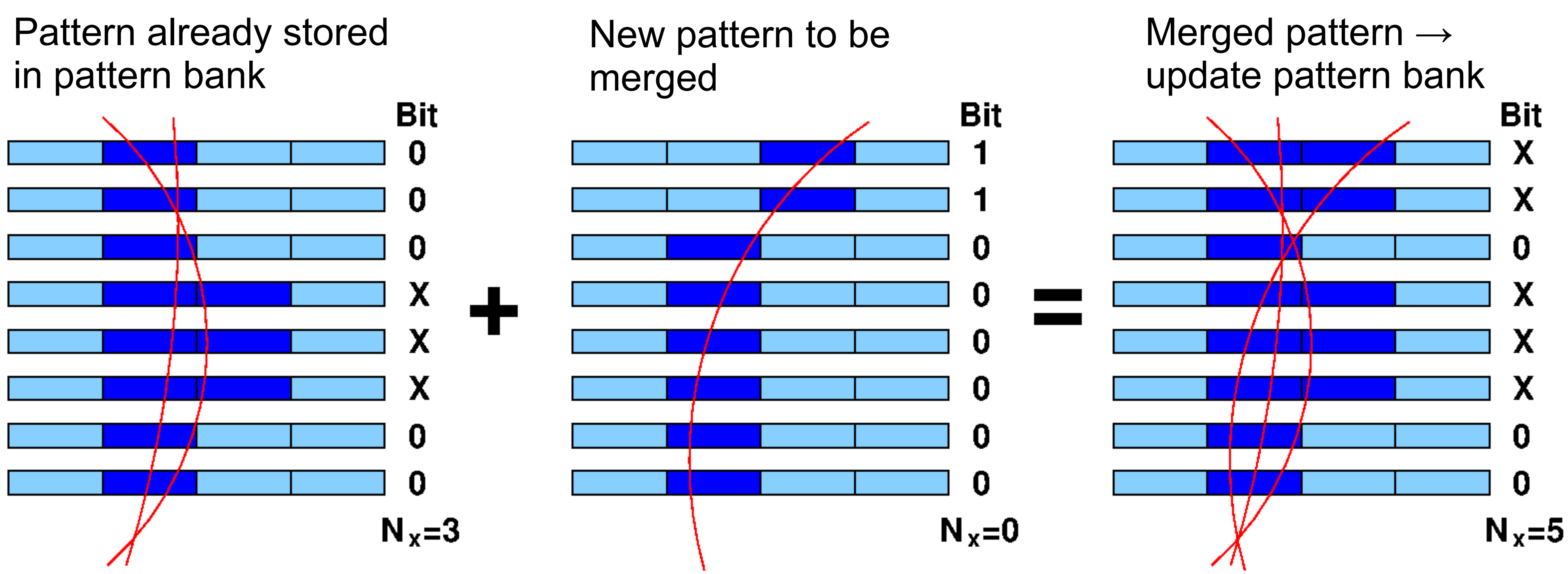


For example:
build a VBF trigger,
w/ quark-tagging?


ATLAS
Simulation
L1=TAU12I
√s = 14 TeV, <μ> = 60
ggH ->τh τh
Multijet QCD
Efficiency
L1 τ candidate pT [GeV]


ATLAS
Simulation
√s = 14 TeV, <μ> = 60
L1=2TAU12I_TAU20I_J25_DR28
PV
FTK L2
PV + FTK L2
Calorimeter L2 + ET1st L1 τ, ET2nd L1 τ>32 GeV
Calorimeter L2 + ET1st L1 τ>40 GeV, ET2nd L1 τ>25 GeV
Efficiency for QCD multijet backgr
Efficiency for Boosted events of ggH → τh τh

Ternary bit merging



- Patterns which differ only at the ternary bit positions can be packed into a single AM address
- Example: a pattern with N_X=3 changes to N_X=5 after adding another pattern

Ternary bits and Gray code

- For each AM chip address: hits are stored in eight layers, one 15-bit word per layer
- Of the 15 bits, 3 bits are ternary
- Ternary bit can encode three settings: 0, 1, X = {0 or 1}
- Ternary bits → many patterns can be saved in one address
- Shown here: a selection of superstrip sizes and positions which can be encoded using 3 ternary bits