



# High-Throughput Computing Collaboration

*Silicon*

21.09.2017 – CERN openlab Open Day

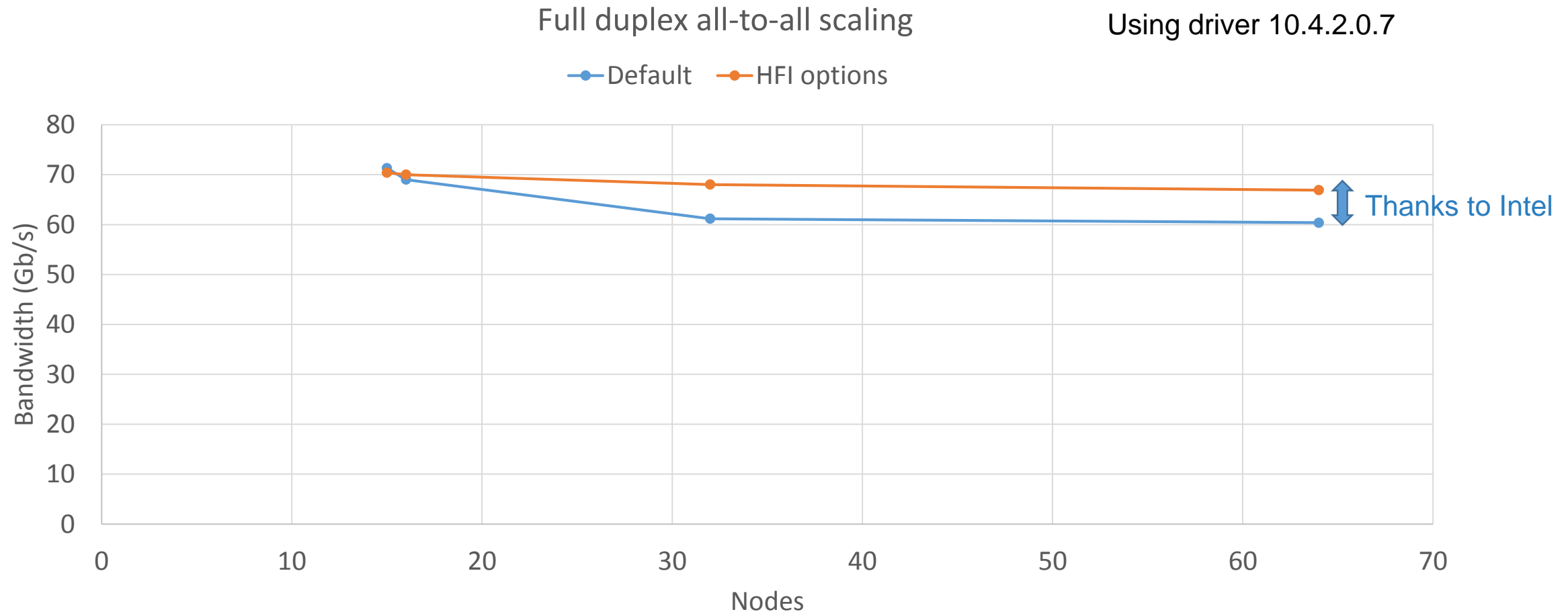
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# Intel® Omni-Path

- Provide 100 Gb/s fabric
- Used in HPC supercomputers
  - MareNostrum (13 in Top500)
  - Maroni (14 in Top500)
- For LHCb : Data Acquisition System (DAQ)
- In 2020 we need to transport 40 Tb/s
  - Require 80 Gb/s sustained on ~500 nodes



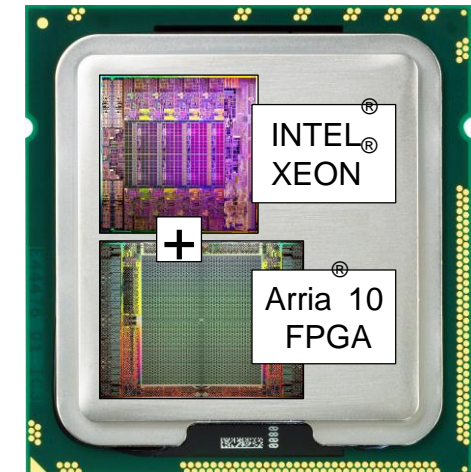
# Omni-Path test on Marconi



# Socket embedded FPGA

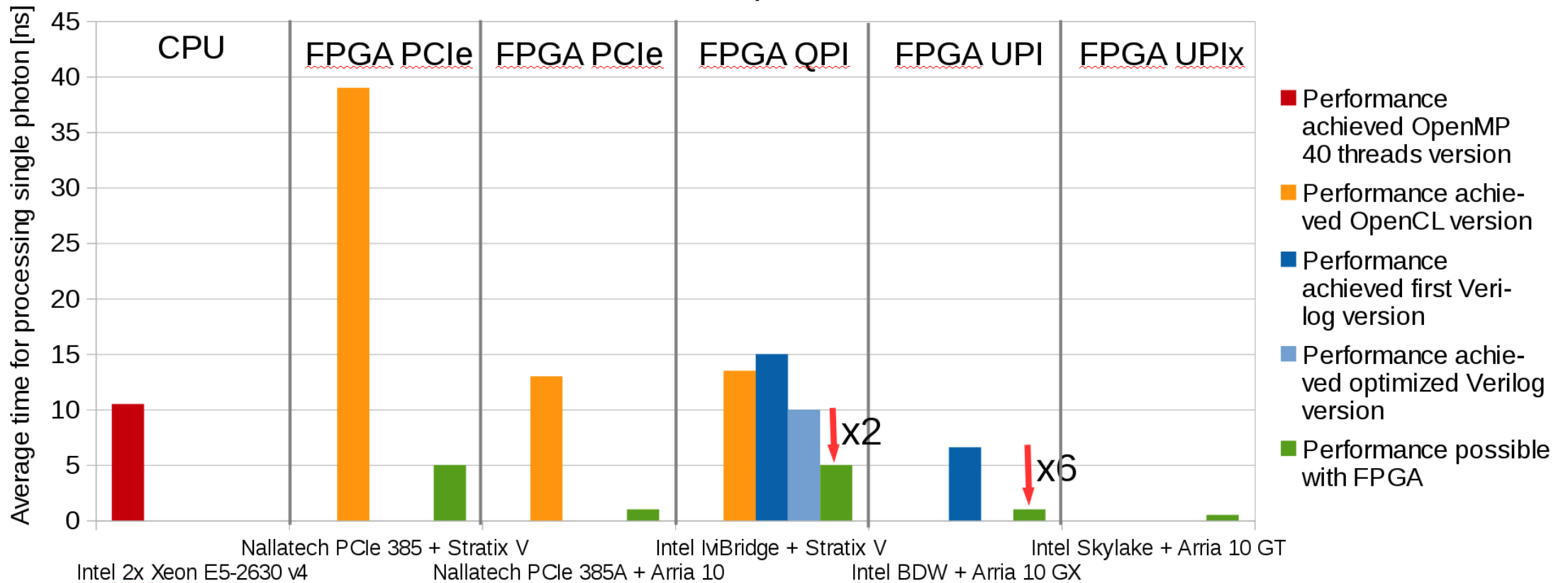
*Coming with the CPU*

- Multi-chip Broadwell package including:
  - Intel® Xeon® E5-2600 v4
  - Intel® Arria® 10 GX 1150 FPGA
- Hardened floating point add/mult blocks (HFB)
- Memory: Cache-coherent access to main memory
- Programming model: Verilog, OpenCL for Skylake



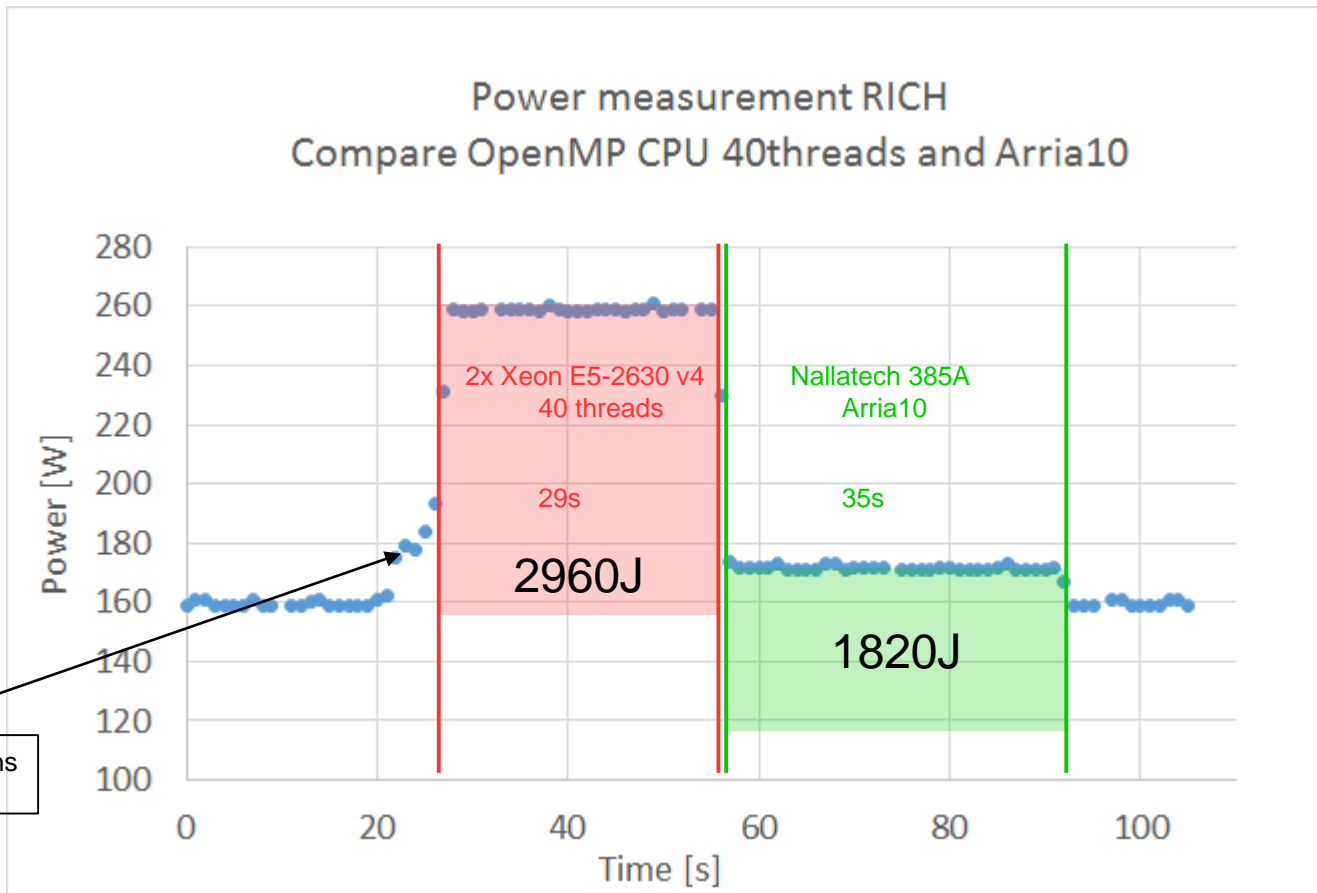
# Apply on LHCb photon reconstruction

Reached and possible run time for single RICH photon reconstruction with different platforms



# FPGA and energy

*There is an opportunity to improve energy efficiency*



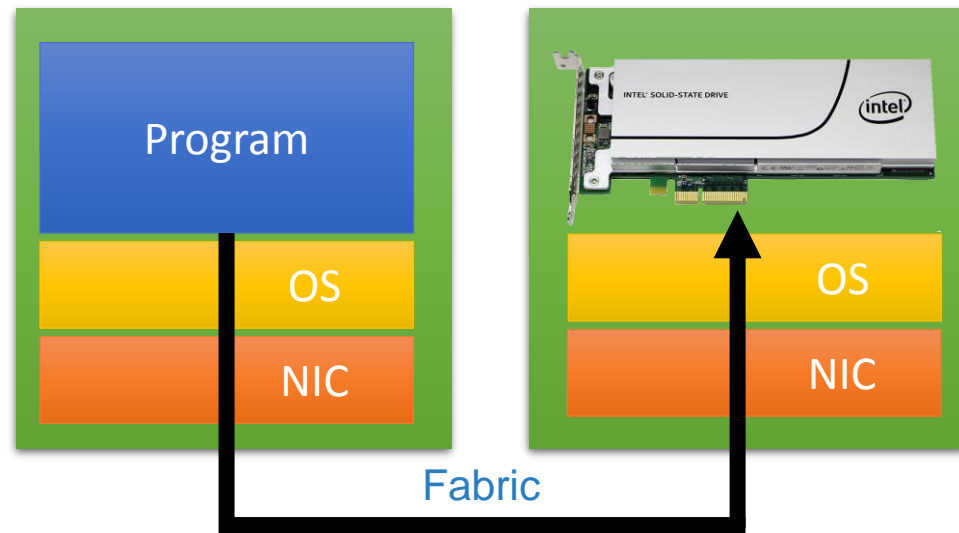
Create random photons  
single thread

# NVMe over fabric

Access to remote NVMe driver transparently

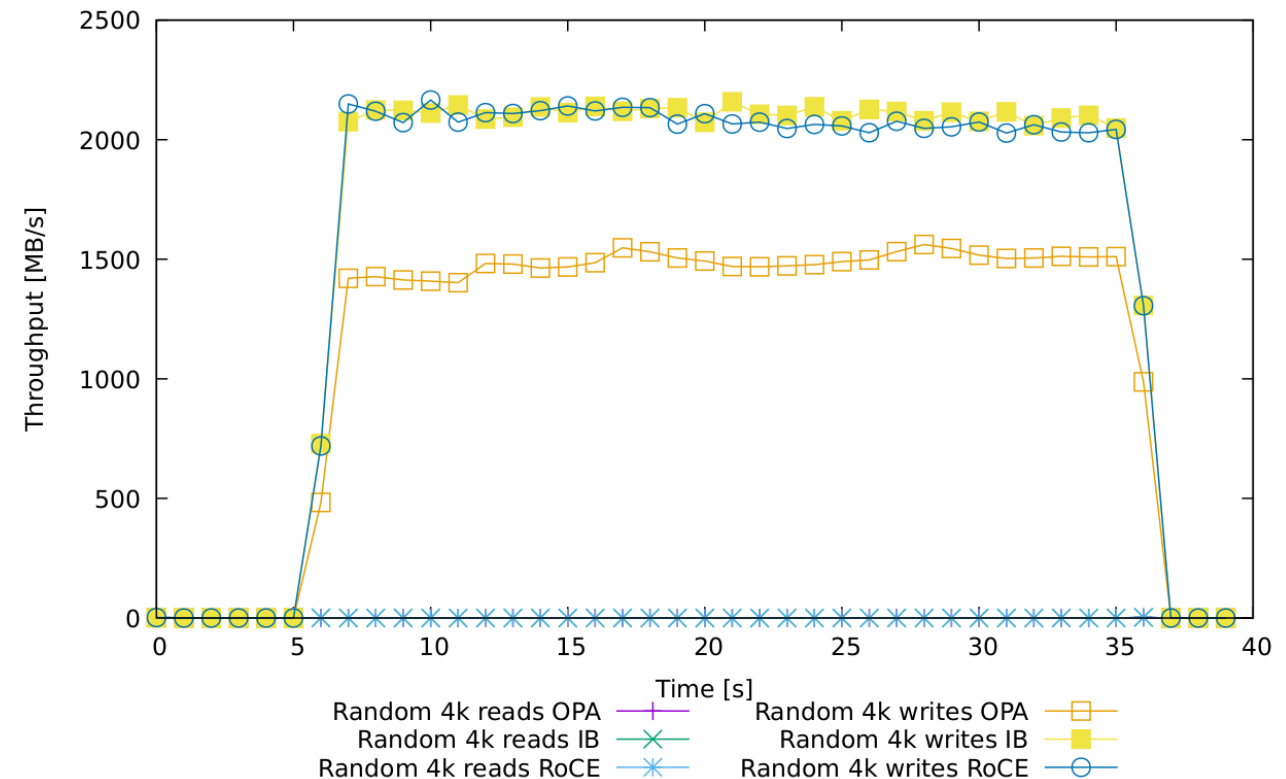
Over fabric.

Tested : Omni-Path, InfiniBand RoCE



Using driver 10.4.2.0.7

Intel Optane SSD throughput over fabric random 4k writes

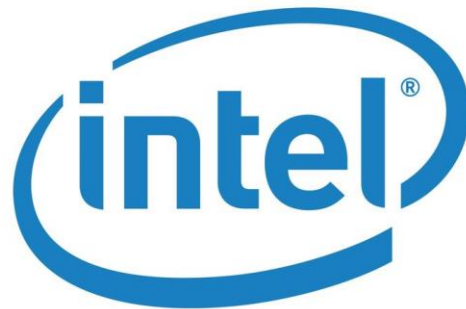


# Thank you

## CERN openlab High Throughput Computing Collaboration

Olof Barring, Niko Neufeld

Alexandru Amihalachioaei, Luca Atzori, Omar Awile, Daniel Cámpora, Paolo Durante, Christian Färber, Plácido Fernandez, Jon Machen, Flavio Pisani, Rainer Schwemmer, Sébastien Valat, Balázs Vőneki



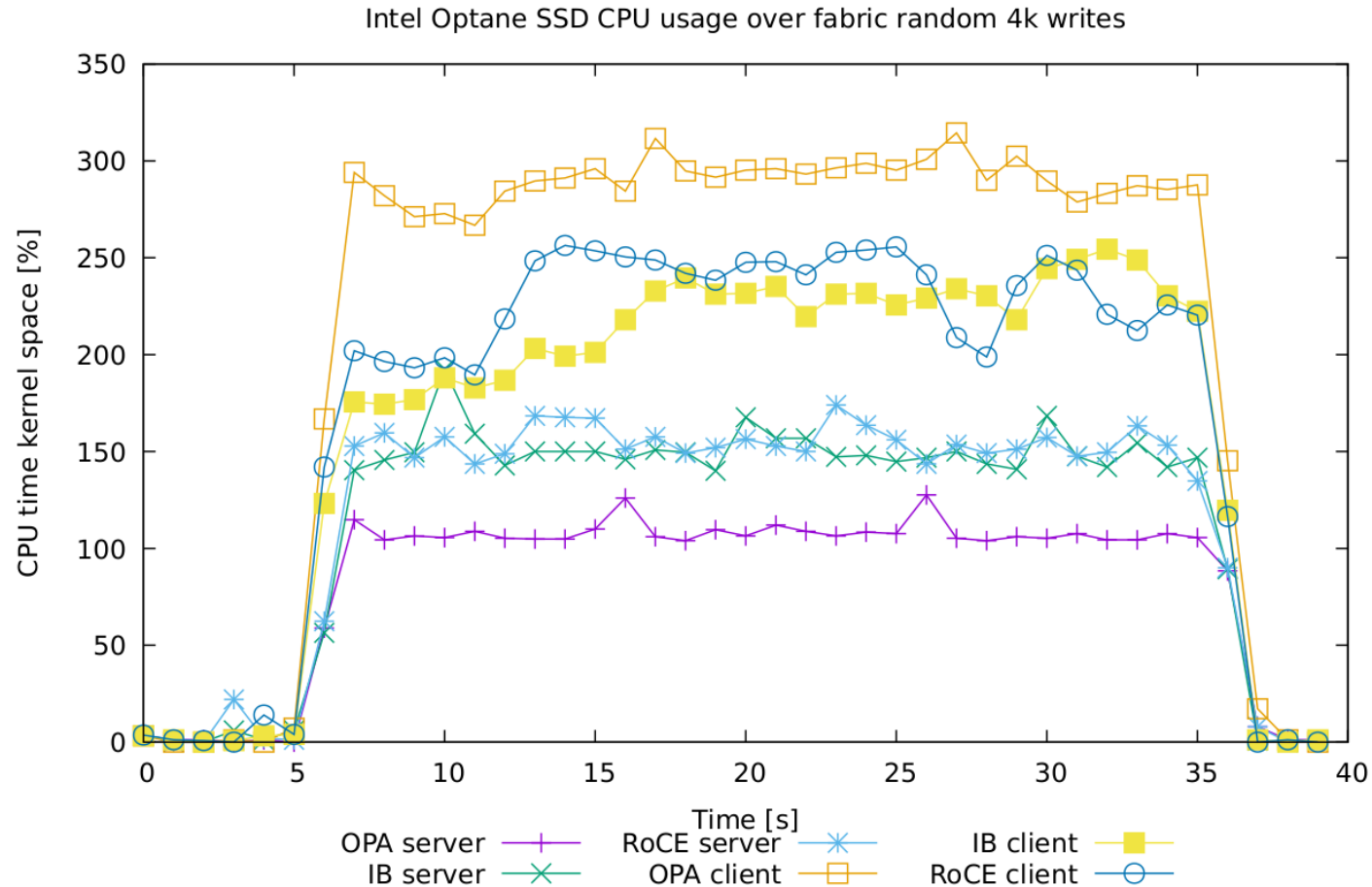




**EXTRA**

# NVMe over fabric

## CPU usage



# HTCC

- Members from Intel®, CERN LHCb and CERN IT
- Test Intel® technologies in the LHC computing environment
  - online computing
  - trigger and data acquisition (TDAQ) systems
  - accelerators for the High Level Trigger
- LHCb upgrade as use case, but applicable to all experiments

