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CONCEPTUAL DESIGN OF THE READOUT ELECTRONICS FOR T2K-II TPCS

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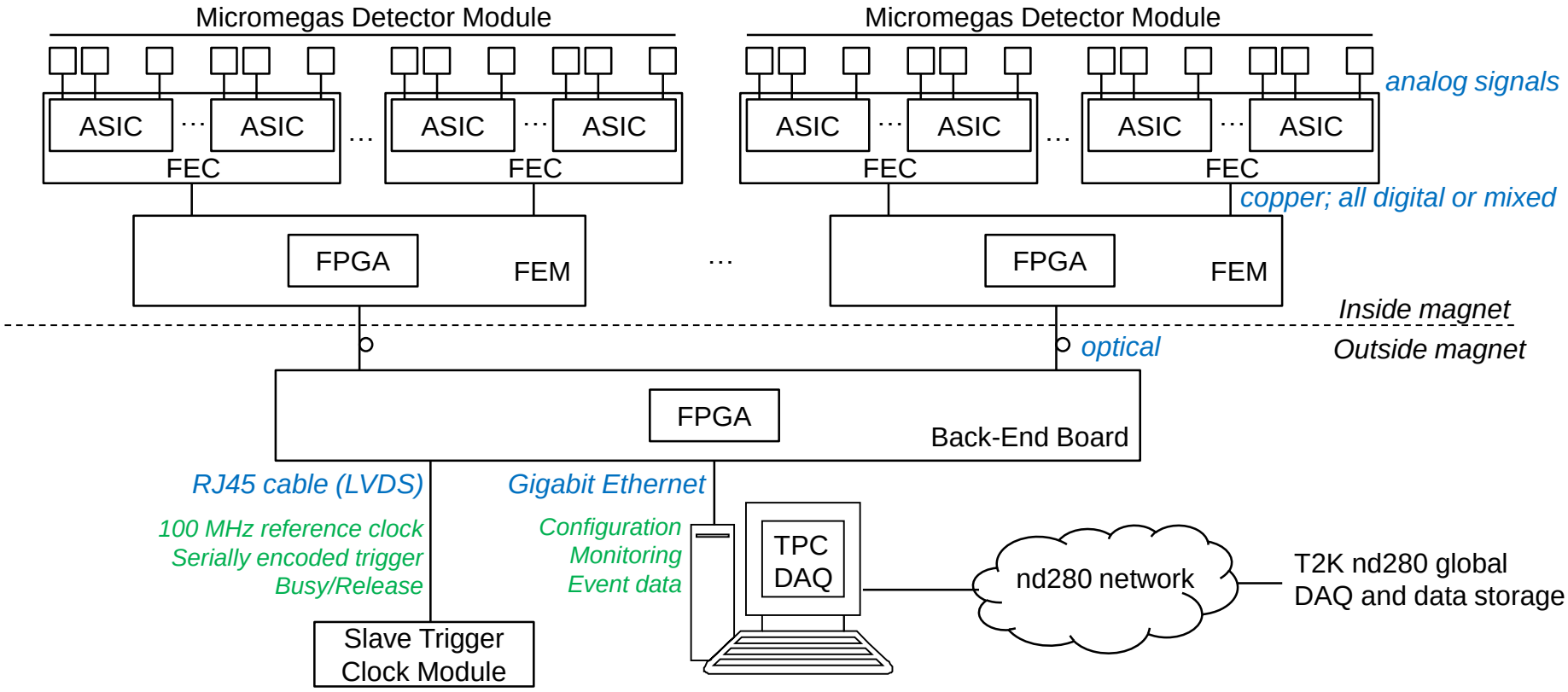
Irfu

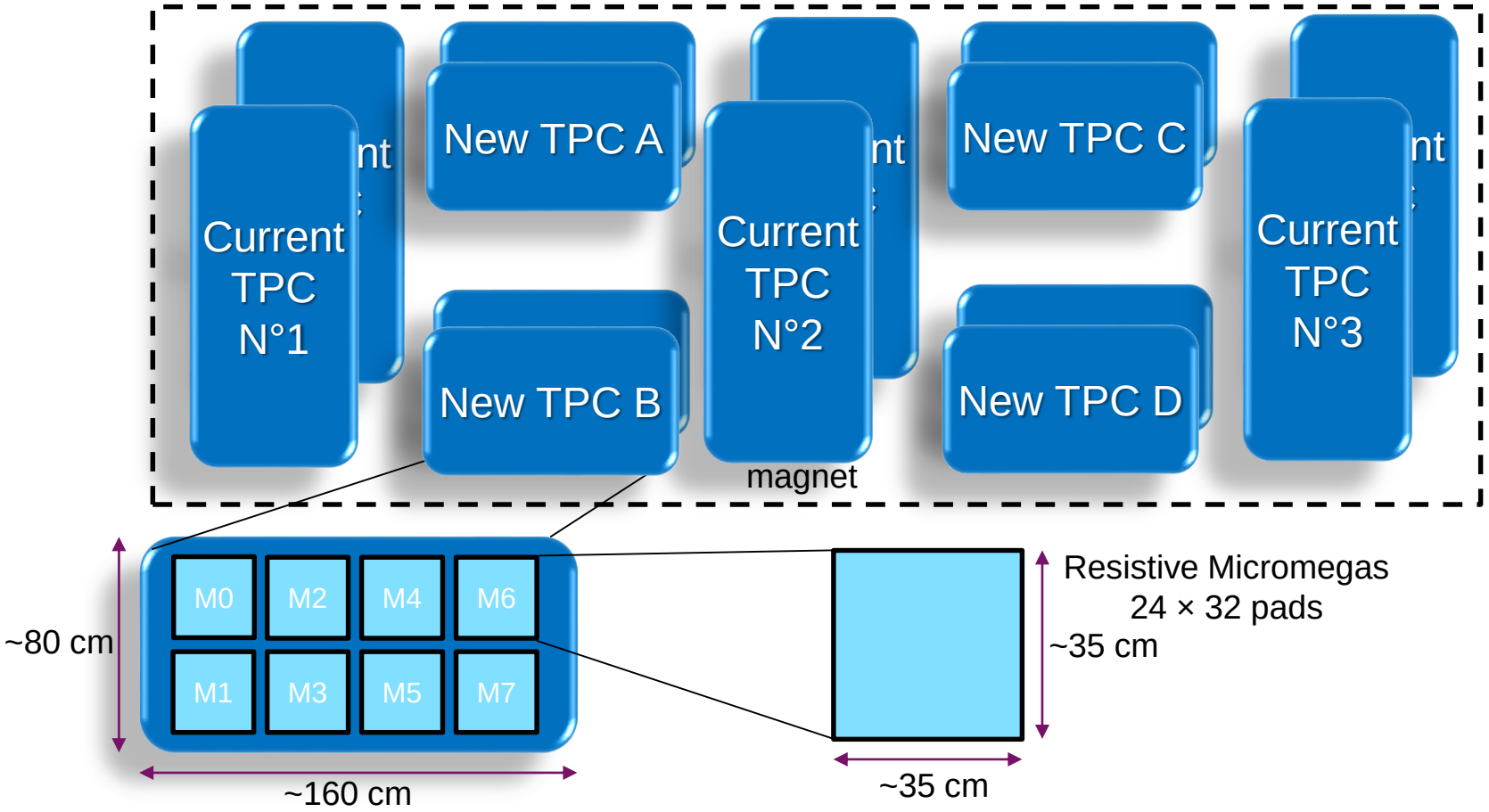
TPC READOUT ARCHITECTURE FROM DETECTOR TO DATA STORAGE



Same (proven) architecture as T2K phase 1:

- TPCs read out by Micromegas Modules; Electronics of each module composed of several front-end cards (FECs) populated with ASICs, controlled by a FPGA placed on a Front-End Mezzanine card (FEM)
- Multiple FEMs controlled by a Back-End Board, e.g. 1 per TPC; all controlled by a PC linked to global T2K nd280 event builder, DAQ, run control and data storage

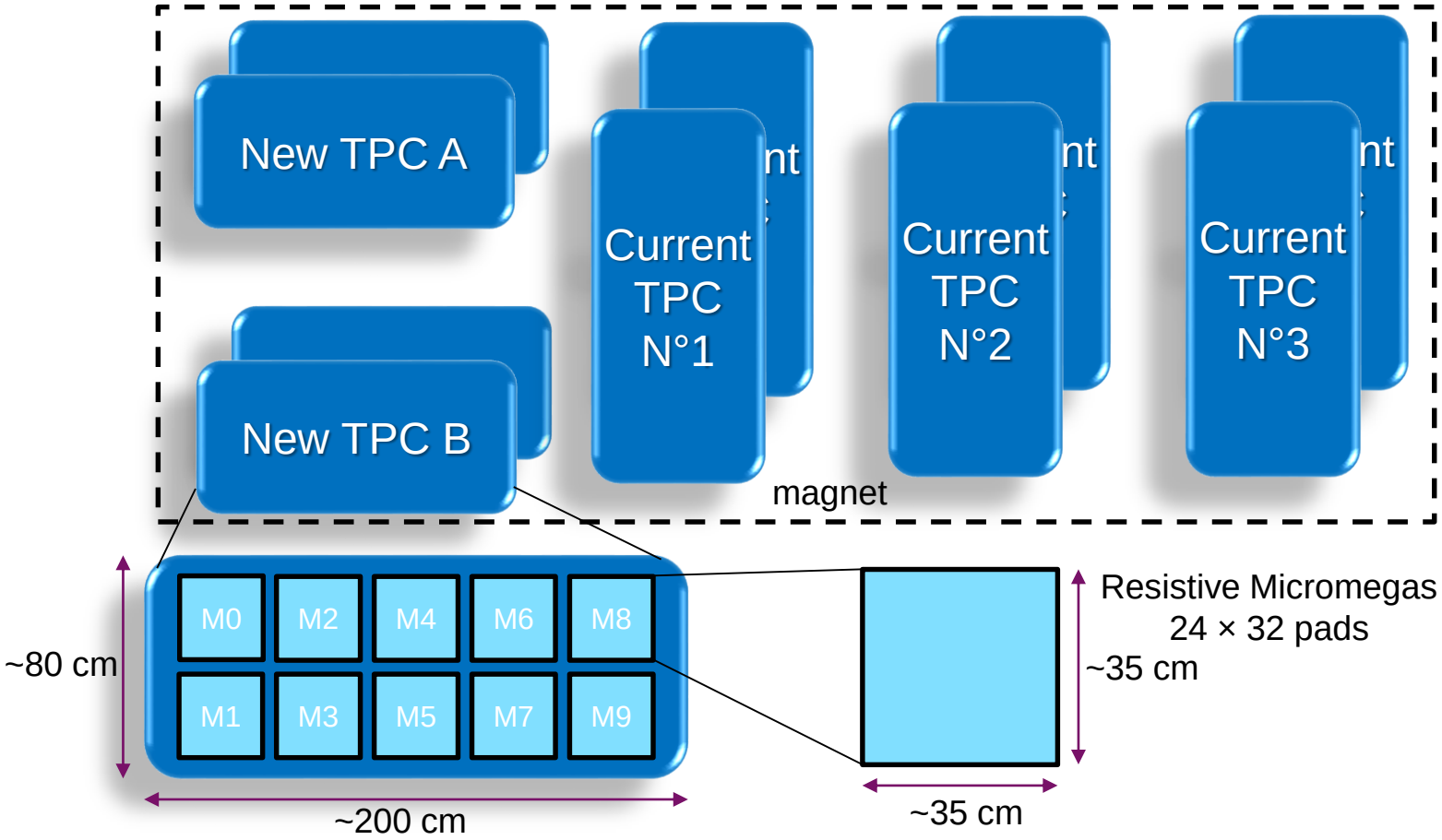
A POSSIBLE DEPLOYMENT



Structure

- **4** TPCs, each composed of **2** end-plates supporting **8** Micromegas modules segmented in **24 x 32 pads**
- Total of **64** detector modules; **48K-channels** (49.152)

ANOTHER POSSIBLE DEPLOYMENT



Structure

- **2** TPCs, each composed of **2** end-plates supporting **10** Micromegas modules segmented in **24 x 32 pads**
- Total of 40 detector modules; **30K-channels** (30.720)

BUILDING BLOCK N°1: FRONT-END ASIC

AFTER

- Designed and used in T2K. Current stock of tested and encapsulated chips: **~780** (53K-channel)
- Pros: low risk, ready now, no manpower, no cost up to ~40K-ch. Cons: limited stock, end of life product

AGET

- Also a proven chip. Current stock too low. Package obsolescence (same problem for AFTER)
- Pros: fresher design than AFTER. Cons: 64 channels rather than 72; no stock; package issue

DREAM

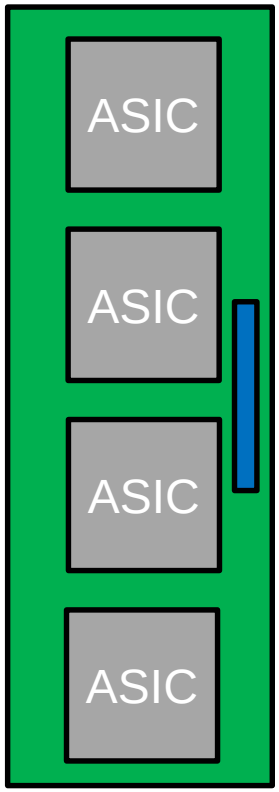
- Also a proven chip but not directly compatible with AFTER-AGET
- Pros: smaller size, packaging OK. Cons: 64 channels, need new production, less re-use from existing

ASTRE

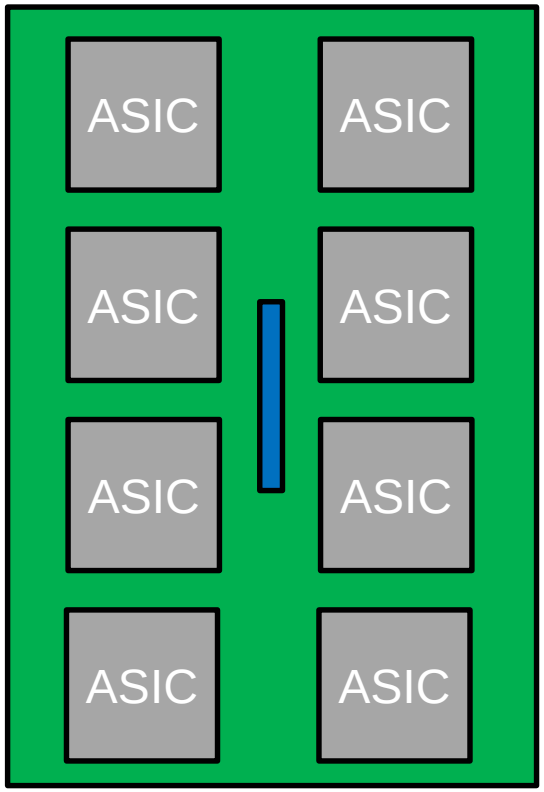
- Space grade version of AGET, also supports longer peaking time (up to 8 µs)
- Pros: most versatile chip. Cons: features not needed in T2K. Package issue. Cost of masks for mass prod.

→ New information from last workshop: found company able to reproduce obsolete package of AFTER-AGET. In parallel we study modifications to do on AGET-ASTRE to fit it in a package with longer life time. If pursued, may also make functional improvements, e.g. limit diffusion of saturation to adjacent channels

BUILDING BLOCK N°2: FRONT-END CARD

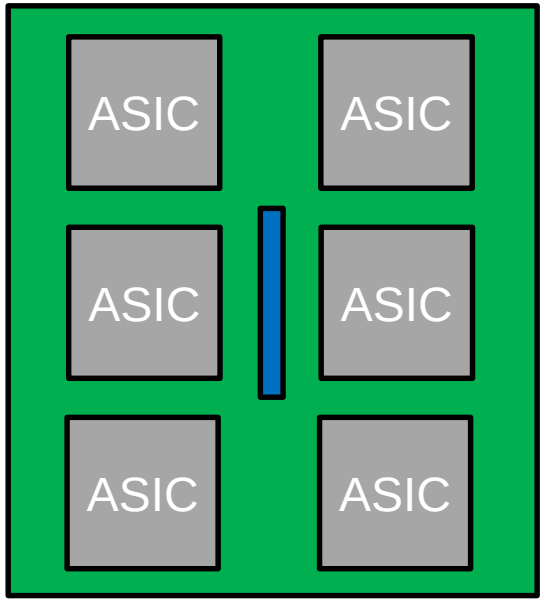


256[i](288[ii]) -channel FEC



512[i](576[ii])-channel FEC

→ Make careful choice of connectors – Those used on T2K phase 1 found fragile



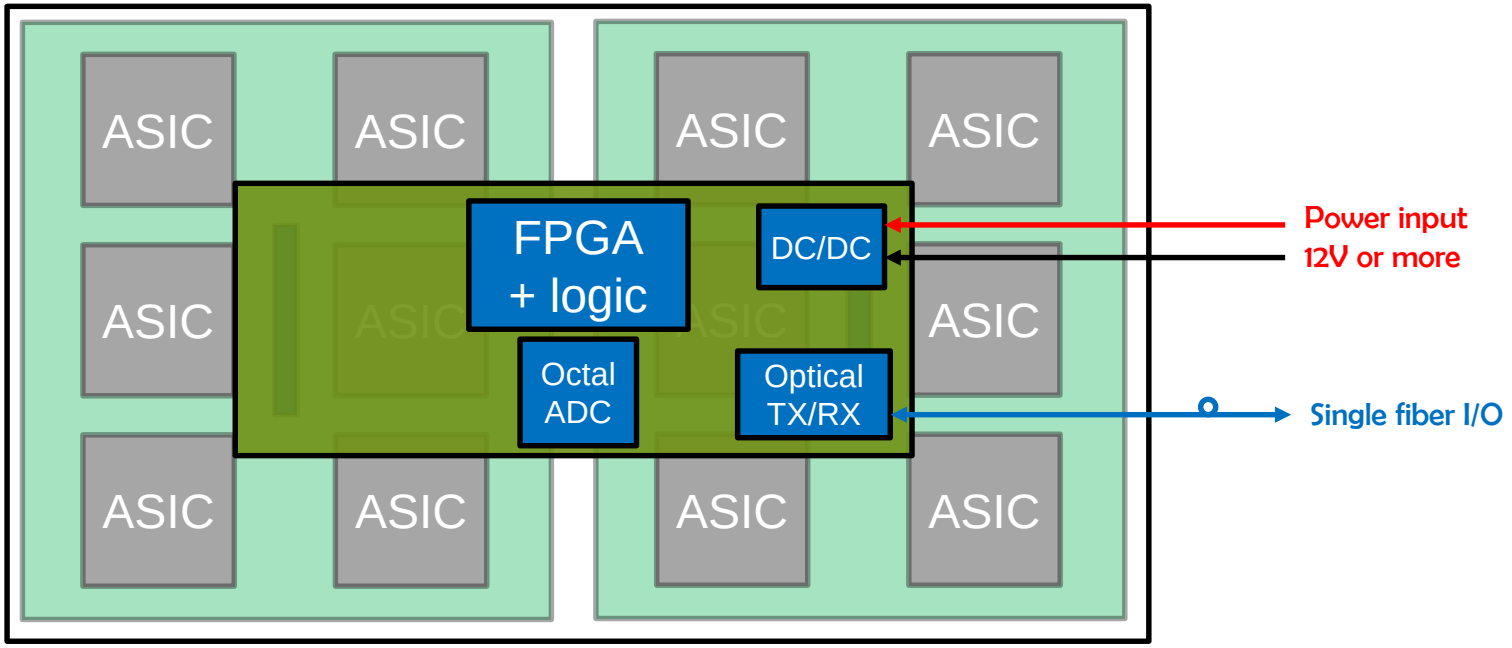
384[i](432[ii])-channel FEC

[i]: with 64-channel ASICs
[ii]: with 72-channel ASICs

Design principles

- Minimal complexity – no protection circuits (resistive MM), no local FPGA, may be not even ADC (multiplexed analog out), only ASICs (packaged…), connectors, simple clock/control fan in/out, power
- If card small enough could be mounted parallel to detector, otherwise perpendicular (like current TPCs)

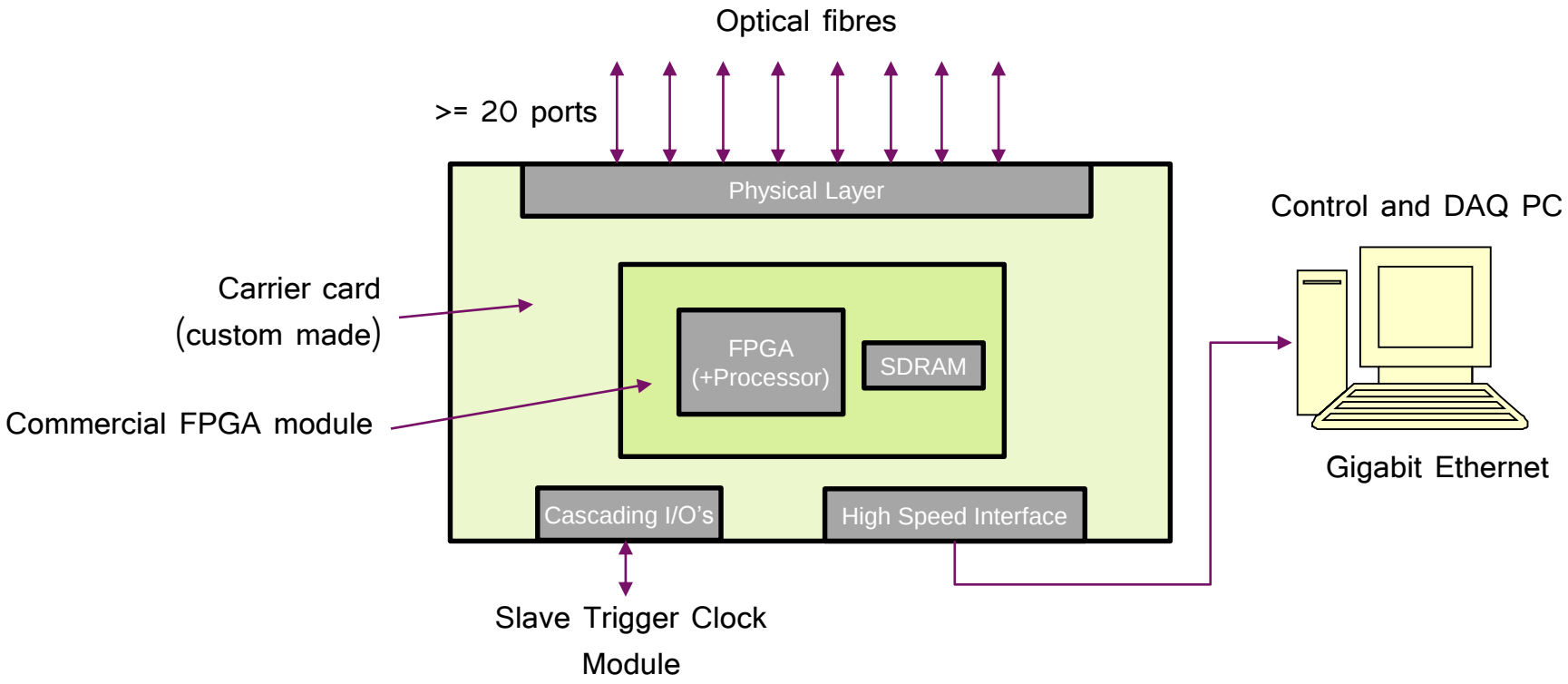
BUILDING BLOCK N°3: FRONT-END MEZZANINE CARD



Design principles

- All local intelligence done in FPGA wired-logic + additional components
- Need to study trade-off between ADC on FECs vs on FEM and parallel vs sequential digitization of ASICs
- Single optical fiber to back-end electronics for clocking, trigger, configuration, data and slow control
- No dedicated network and processor for slow-control (Canbus was used on T2K phase 1)
- High voltage input (e.g. 12 V) + efficient down conversion; possibly power distribution to FECs via FEM
- Less FECs per FEM by designing denser FEC (had 6 FECs with 4 AFTER per FEM in T2K phase 1)

BUILDING BLOCK N°4: BACK-END ELECTRONICS



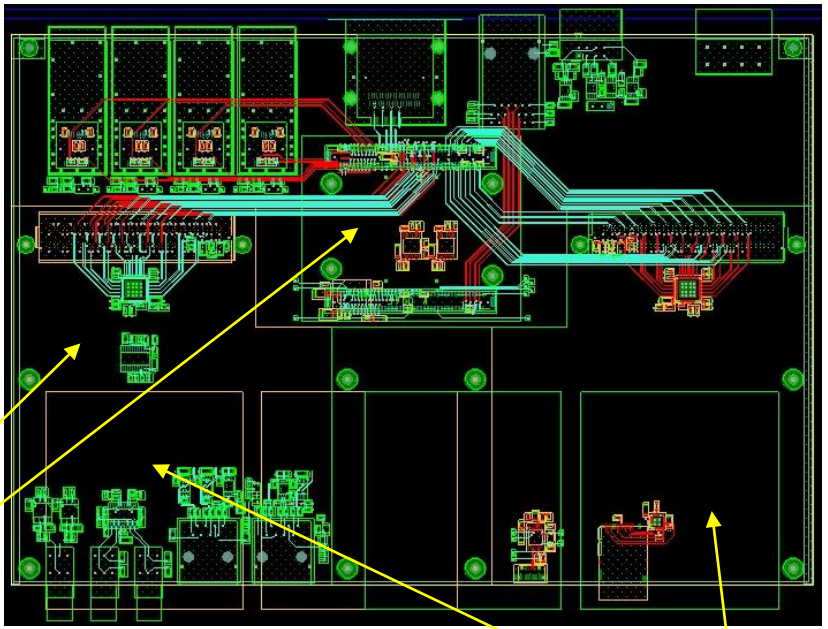
Design principles

- Carrier card + commercial System-On-Module + sufficient number of optical transceiver + Gigabit Ethernet interface to local control and DAQ PC + I/O's for clock and trigger
- FPGA firmware and on-board processor with embedded software – bare metal or Linux

BUILDING BLOCK N°4: BACK-END ELECTRONICS (CON'T)

Strategy

- Direct hardware re-use and large part of firmware/software re-use of the ***"Trigger & Data Concentrator Module - TDCM"*** under development at Irfu for PandaX-III experiment
- The TDCM supports the control and readout of up to 32 front-ends cards/modules



6U form factor custom carrier

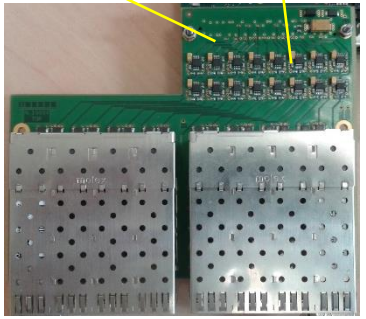
ENCLUSTRA FPGA SOLUTIONS

Commercial System-On-Module
Mercury ZX1 (Xilinx Zynq 7045)

PANDA X

Current status

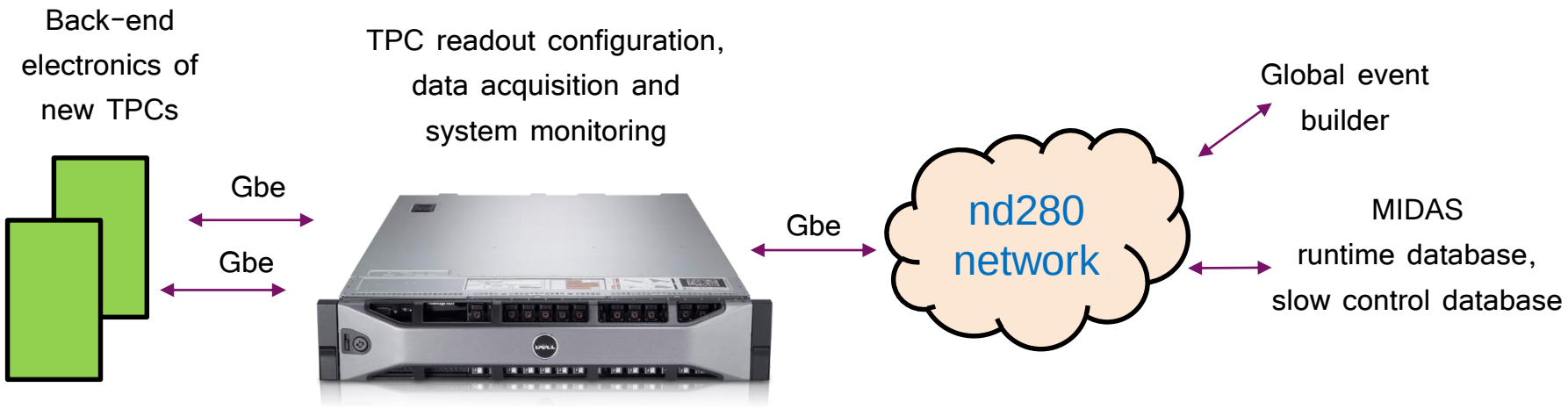
- Board design and layout completed. Prototype in production
- Large part of embedded firmware and software developed
- Test and debugging for PandaX-III planned for 2017
- Production of first batch in 2018
- Only software/firmware adaptations may be needed for T2K phase-II



16-optical ports
Mezzanine card

BUILDING BLOCK N°5: TPC BACK-END PC AND SOFTWARE

Quantity required: 1 + 1 spare
Estimated cost: 8k€



Proposed strategy and work package outline

- Entirely based on commercial hardware
- Develop on-line software to bridge new TPC readout system to current MIDAS based DAQ

→ Still available to contributors – Some expression of potential interest at Irfu

BUILDING BLOCK N°6: SERVICES

Power supplies & cabling

- LV for front-end electronics; LV for back-end electronics
- Cables and optical fibers

Goals for phase II

- Higher efficiency and smaller cable cross-section by having a higher voltage distribution and the use of magnetic field tolerant DC/DC converters locally
- Reduce local cabling by using board-board connectors to bring power to the FECs through the FEM instead of using a multi-drop cable harness
- Optical fiber count reduction by a factor 2 using single fiber bi-directional optical transceivers

→ Work shared between groups responsible of front-end and back-end electronics

Mechanics and cooling

- Support plates for front-end electronics, provides mechanical support, protection, shielding & cooling
- Water cooling system needed for front-end; ventilated crate for back-end

Goal for phase II

- Simplify mechanics and cooling plates (beautiful but very expensive on T2K phase 1)

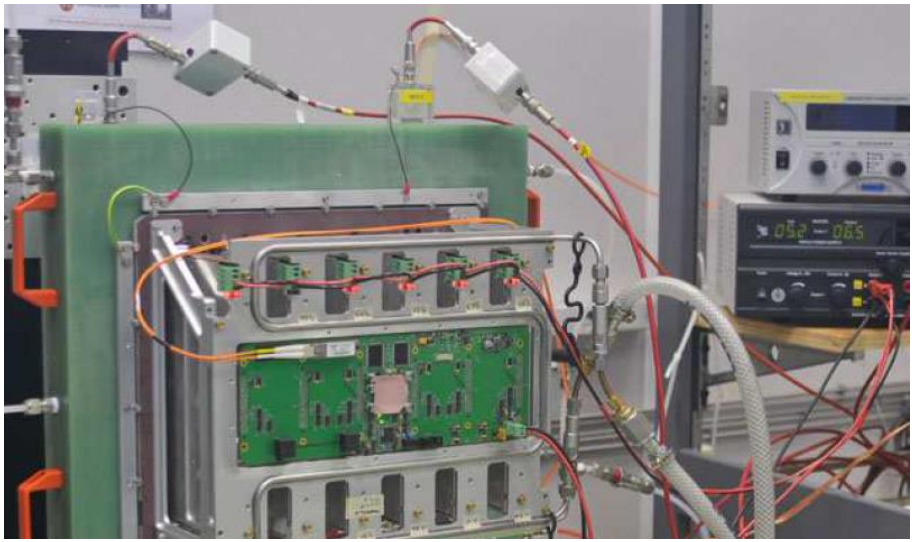
→ Separate tasks from the electronics itself (but close interaction)

Open to collaborators

BUILDING BLOCK N°7: DETECTOR PRODUCTION TEST BENCH

Purpose & tools

- Test all the detectors of the new TPC
- Robot arm to move radioactive source and scan detector
- Gas box, HV, LV, readout electronics for 1module and small DAQ cooperating with robot arm



Test bench for production of detectors T2K phase 1 (IFAE/CERN/IRFU)

Proposed strategy

- Probably difficult to re-use or adapt system used 10 years ago (obsolete, dismantled?)
- Mostly new system; need not wait until final electronics of T2K-II is made.

→ Interest of Warsaw group to take responsibility for this system. Funding request submitted. Waiting for results

T2K-II TPC READOUT ELECTRONICS BLOCKS AND TENTATIVE ASSIGNMENT

Void if AFTER is used and current stock of chips is sufficient

Front-End Card design, production, test — Lpnhe

Front-End Mezz. design, production, test — Irfu

Front-End Mezz. firmware — Irfu

Front-end card Prod. test-bench — Lpnhe

Front-end mezz. Prod. test-bench — Warsaw

on-detector

off-detector

Back-end Board design, production, test — Irfu

Embedded Firmware & Software — Irfu

DAQ hardware & software — ???

Power supplies Cabling, shared

Mechanics, Cooling — ???

Detector test & calib. Test-bench — Warsaw

Services and specific functions

Tentative work sharing

- Subject to the approval of the T2K collaboration and the management of each institute involved, as well as the obtaining of funding and resources to perform the corresponding tasks
- Still a few unassigned tasks

ELEMENT COUNT AND COST ESTIMATE

Component	Scenario 4 TPCs	Scenario 2 TPCs
# of Micromegas Modules	4 * 2 * 8 = 64	2 * 2 * 10 = 40
# of channels (Micromegas Module = 24 * 32 pads)	64 * 768 = 48 K	40 * 768 = 30 K
# 64-channel ASICs	768 0 € (existing stock of AFTER)	480 0 € (existing stock of AFTER)
# of FECs (6 ASICs per FEC i.e 384 channels)	128 128 * 400 = 51.2 k€	80 80 * 400 = 32 k€
# of FEMs (1 read 2 FECs, i.e. 1 MM)	64 64 * 600 = 38.4 k€	40 40 * 600 = 24 k€
# of Back-End Boards (reads 1 TPC i.e. 16 or 20 MM)	4 4 * 5000 = 20 k€	2 2 * 5000 = 10 k€
# of Back-end PC	1 8 k€	1 8 k€
Total estimated cost	117.6 k€ (2.4 €/channel)	74 k€ (2.4 €/channel)

Notes

- Excludes cost of R&D, prototypes, spares, services and manpower
- Optimistic low channel count OK with current stock of AFTER (add >50 k€ if new production required)
- Channel count per module can be 27 * 32 pads using AFTER (72-channel vs 64-channel ASIC)

HOW TO PROGRESS?

Critical items

- Need to know how many TPCs to build, define detector module count and detector segmentation
- Must confirm or infirm if resistive Micromegas can be used:
  - determines how much channel reduction can be made for a given resolution objective
  - defines if protection circuits are needed or not on the FECs
  - influences size of the FEC and board mounting (parallel or perpendicular to detector)
- From total channel count determine if stock of AFTER chips is sufficient: if not (or if we want to use another chip), there is substantial work to do, time needed and money to spend on microelectronics

Development roadmap

- Priority is to define a prototype detector as close as possible to final and make performance assessment
- R&D on connectors, power distribution/conversion, ASIC output digitization can be done independently
- Back-end boards may be the first piece to exist if re-used from a currently on-going development
- FEM and FECs can only be designed after some final choices are made but a first iteration of prototyping is possible. Large parts of the firmware of the FEM can be developed on currently existing hardware.