ToF Electronics

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ND280 UPGRD
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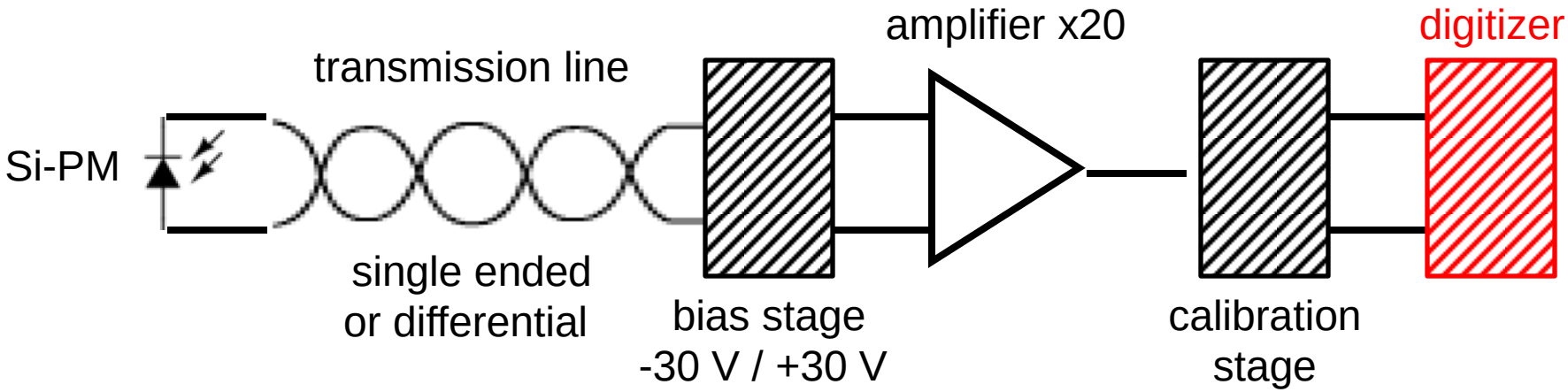
Simplified Block Diagram



no amplifier nor bias PS at the Si-PM

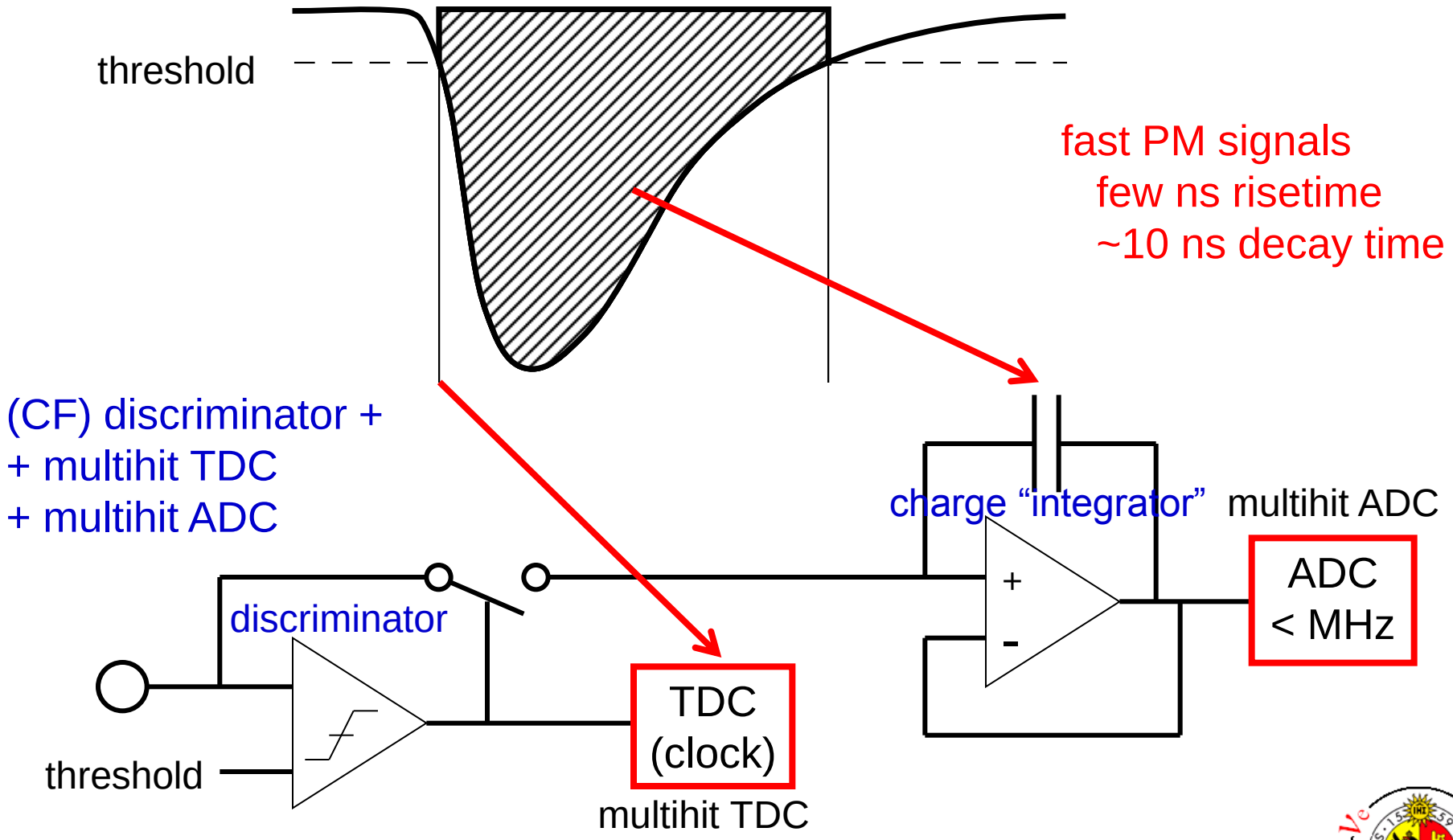
try to drive the Si-PM signal over a long cable (single ended or differential)

use same cable to bias the Si-PM

try to include everything on the same FE board:

- bias stage
- amplification stage
- digitization (+ readout)

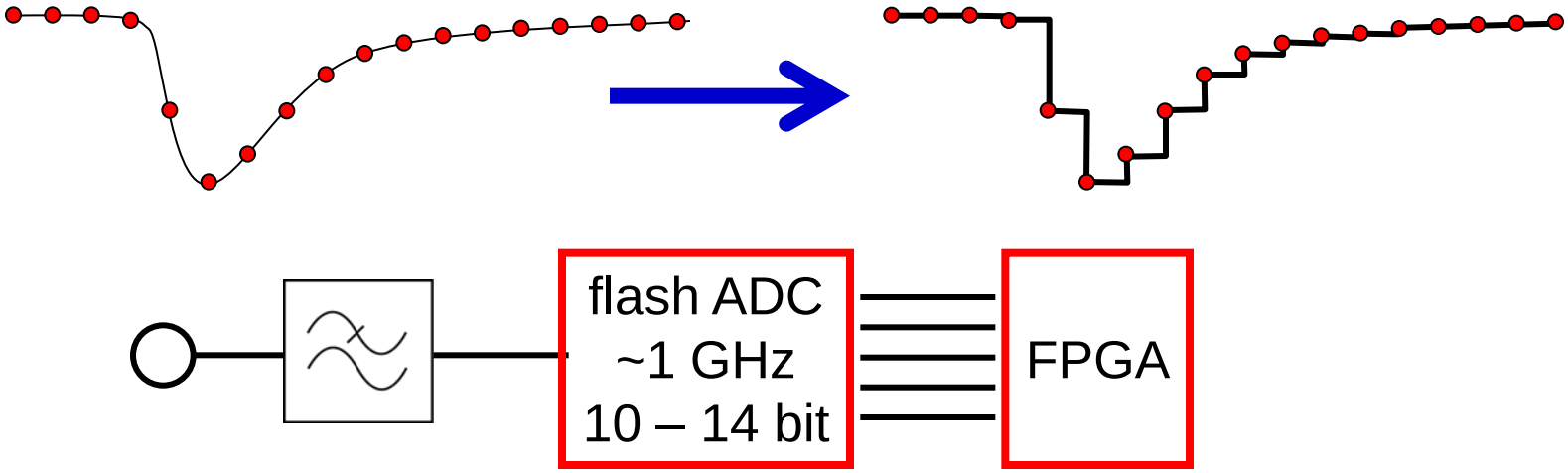
How To Measure Best Timing / Energy "Traditional" Approach



all this can be integrated in single ASIC

How To Measure Best Timing / Energy Waveform Digitizer

flash ADC
+ FPGA



continuous waveform recording / processing

The waveform approach combines different functionalities:

CFD, (multi-hit) TDC, Q-ADC, peak-sensing ADC, etc.

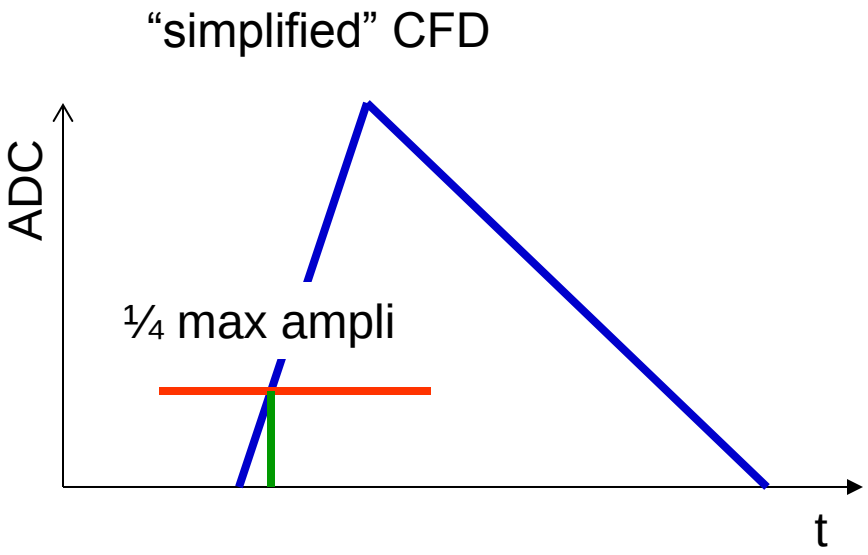
~100 ps resolution requires very high sampling rate ~GHz

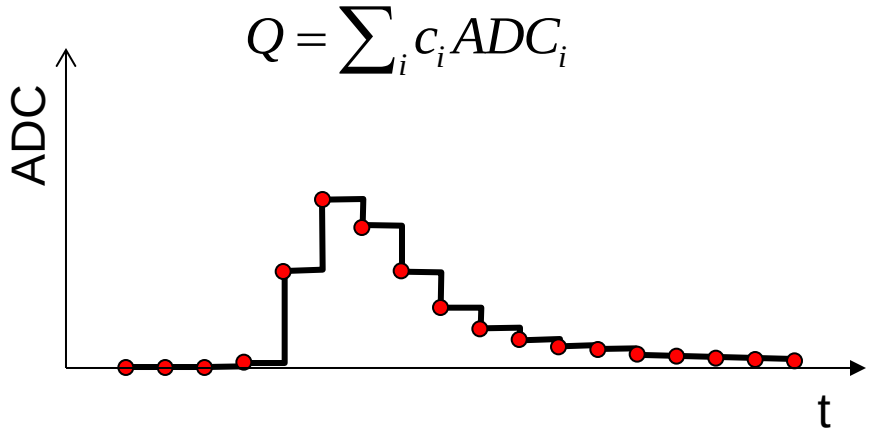
general trend in signal processing

less hardware, even “sloppy” amplifiers will work

storage of full waveforms allows for elaborate analysis

Waveform Processing





Time resolution

1000 ps sampling (1 GHz)

without doing anything
→ σ = 1000 ps / √12 ~ 300 ps

with "interpolation" can obtain
10 × better performance
→ σ < 50 ps

Charge resolution / dynamical range

12 bit over 1 V
→ σ = 0.25 mV

waveform sampled several times i.e. ~20 ×
"effective" # of bits: 12 bit + ½ $\log_2$ n → 14 bit
→ σ = 0.25 mV / √n < 0.1 mV
(10^4 dynamical range)

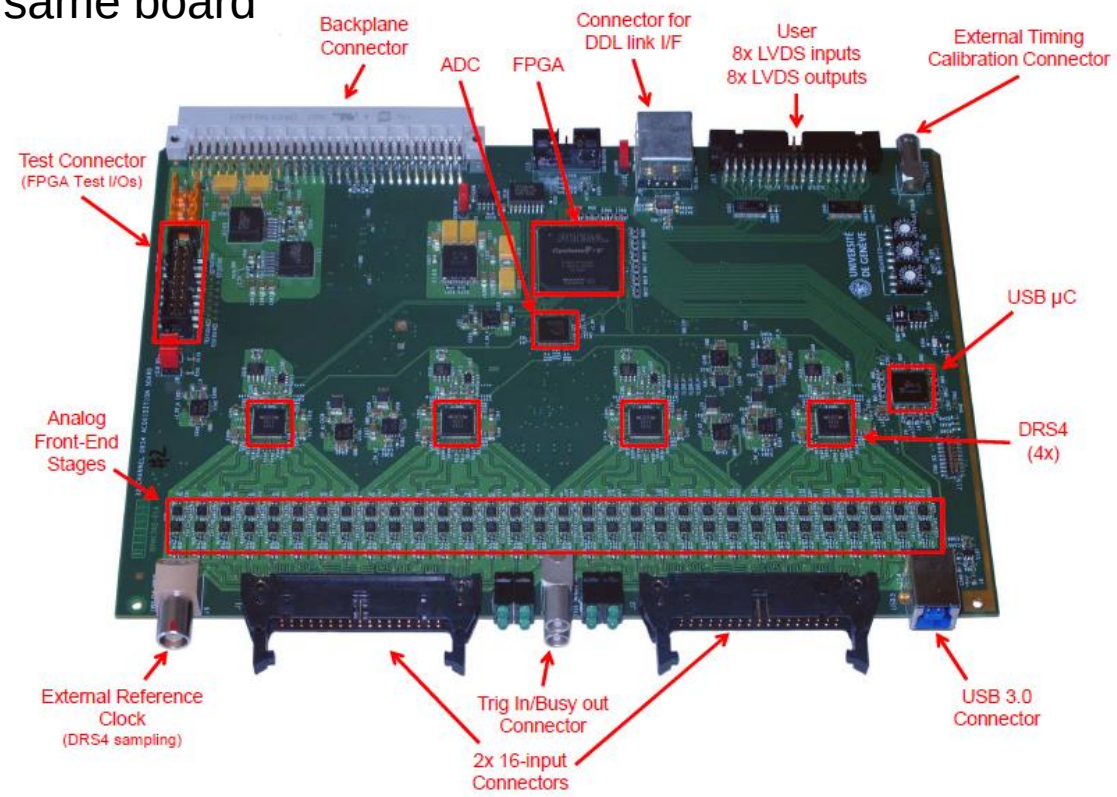
Proposed Solution

Use the DRS digitizer to record the signals from the ToF detectors
(see previous presentations on the functioning of the DRS digitizer)

Technology well mastered at UniGE (A. Bravar and S. Debieux)

“Adapt” the DRS deep buffer version under development for NA61 to ND280
include Si-PM amplifier on the same board
include bias stage on the same board

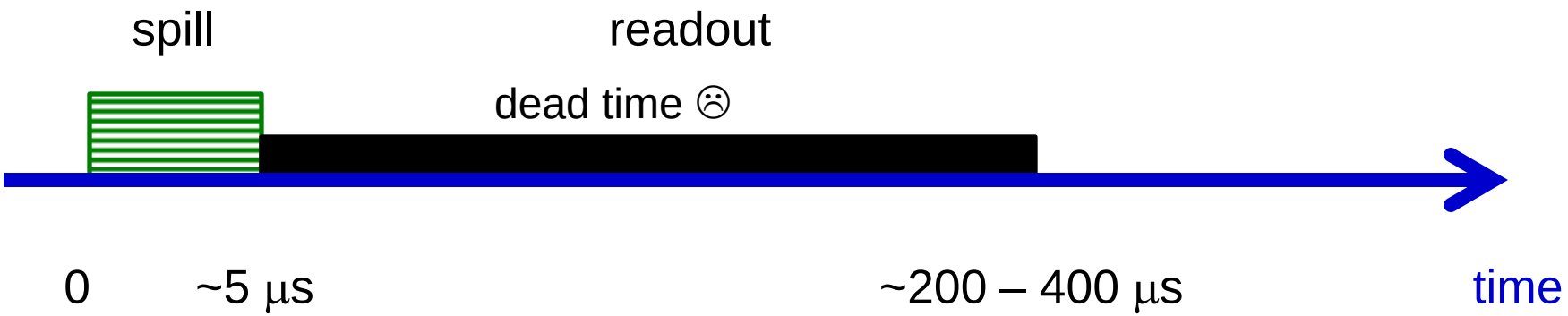
16 ch. / board
(8 DRS ASICs / board)
sampling speed ~ 1 GHz
buffer depth ~ 5 μs



Implementation in ND280

spill length ~ 5 μs
sample continuously the signals from the ToF detectors during the spill, and digitize later
(buffer deep enough to record also Michel electrons + 1τ ~ 2 μs)

with capacitor arrays cannot sample and digitize simultaneously → deadtime
for a low rate application the deadtime is not an issue, kHz DAQ rate



Buffer depth and sampling speed
driven by “active” window and
signal speed (for good timing, require 4 or 5 samples on the rising edge)

Outlook

Once we decide which way to go can start assessing the suggested readout scheme
- Si-PM transmission line (differential vs. single ended, length, noise, distortion)
- biasing the Si-PM “remotely”
- develop 20x Si-PM amplifier

The design of the digitizer will start from the existing (NA61) design
- keep the digital part (ADC, FPGA) with minor modifications
- 16 ch. (8 DRS chips) / board (to contain costs)
- use same calibration scheme

and develop new input stage (amplifier and bias on the same board)

About 9 months to develop such electronics
(can start working on this in fall 2017)

Need to develop the readout for the DRS boards to be used in ND280 (help welcome!)

Cost: too early for details, expect something around 100 $.

Final timing resolution will depend on the scintillator ⊗ WLS fiber response
- need some optimization work (fast scintillator and fast WLS fiber)
- easy, quick, and not expensive R&D interesting also for other applications