Characterisation of Capacitively Coupled HR/HV-CMOS Sensor Chips

Iraklis Kremastiotis
(CERN, Karlsruhe Institute of Technology)

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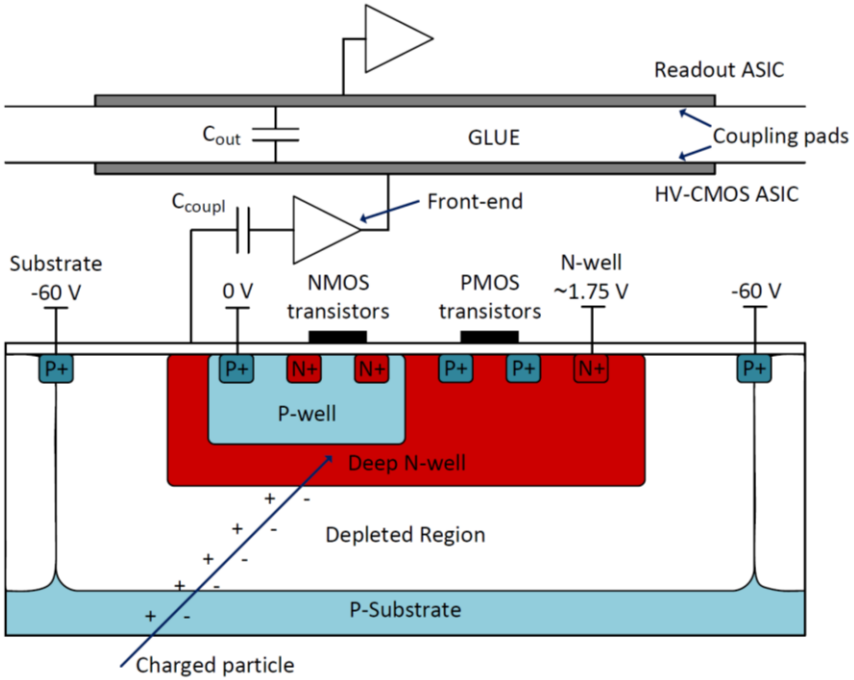
Introduction to capacitively coupled pixel detectors

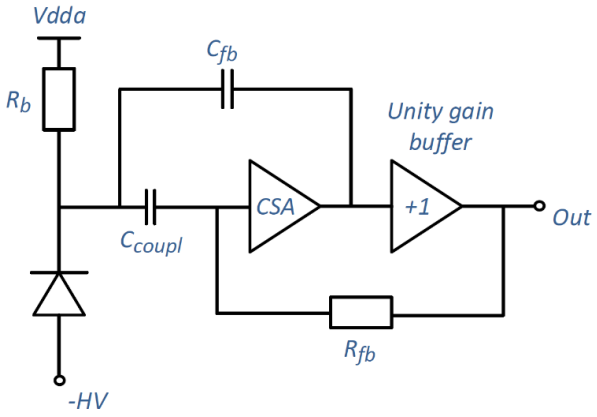
- Capacitively coupled pixel detector:
  - In the HV-CMOS device, all electronics are placed in a deep N-well
  - The deep N-well is also the collecting electrode
  - The charge is amplified in a Charge Sensitive Amplifier (CSA) and then transferred through a thin layer of glue to the readout chip for further processing



- An assembly consisting of the C3PD HV-CMOS sensor chip *[1]* and the CLICpix2 readout chip *[2]* has been built in order to study the concept of capacitive coupling in the framework of the CLIC vertex detector studies
  - Both chips are the successors of a 1st generation of chips that have been tested in capacitively coupled assemblies *[3]*

The CLICpix Capacitively Coupled Pixel Detector (C3PD)

- HV-CMOS sensor to be capacitively coupled to the CLICpix2 readout chip
  - Produced in a commercial 180 nm HV-CMOS process
  - Requirements:
    - 128×128 square pixels with $25\ \mu m$ pitch
    - Rise time: $\sim 20\ ns$
    - Charge gain: $> 120\ mV/ke^-$
    - Power consumption: $< 50\ mW/cm^2$ (both for sensor and readout chip, after power pulsing)
  - The analog front-end is based on a charge sensitive amplifier (CSA), followed by a unity gain buffer
  - A standard I²C interface is used for configuration *[4]*
  - A 3×3 cluster of pixels is multiplexed and buffered to the IOs in order to monitor the front-end output
  - One of the monitored pixels is used to directly monitor the injected test pulse



- Submission with higher resistivity wafers
  - C3PD sensor chips with higher values for the substrate resistivity ($\sim 20, 80, 200, 1000\ \Omega\text{cm}$) are expected to be received soon
  - The higher substrate resistivity is expected to be beneficial for the charge collection thanks to the larger depleted volume *[5]*
  - A layout modification took place in order to achieve a higher breakdown voltage

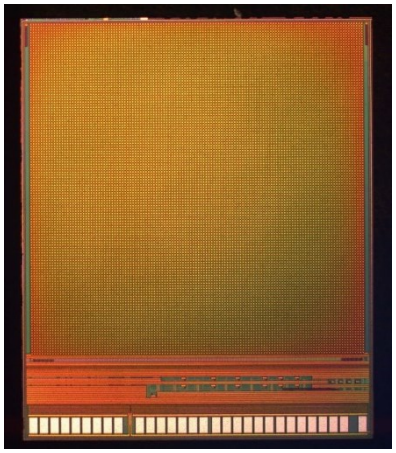
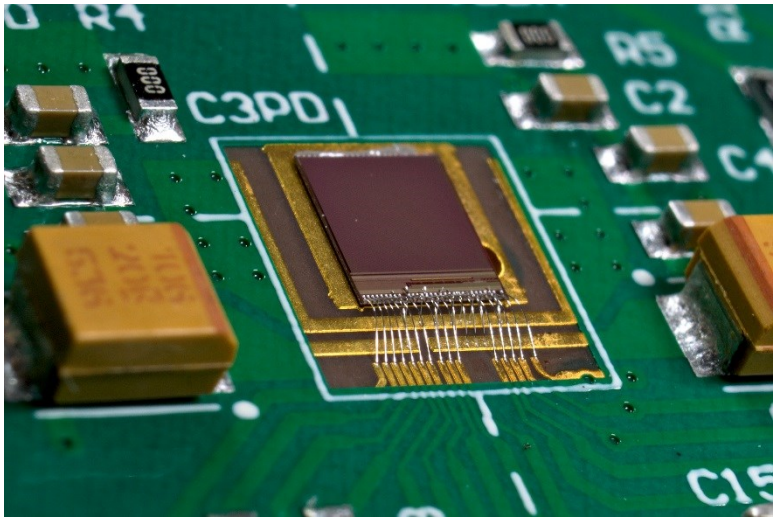
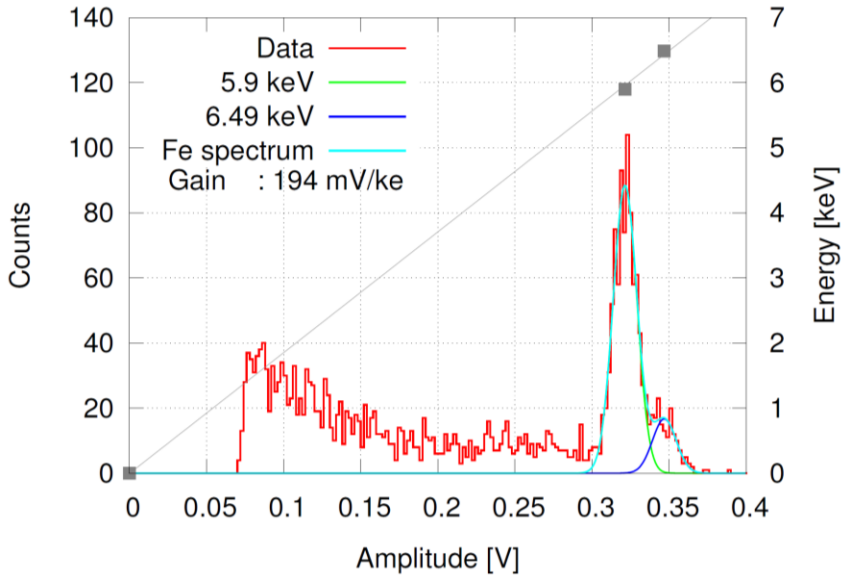


Photo: J. Alozy

Measurements with bare C3PD chips

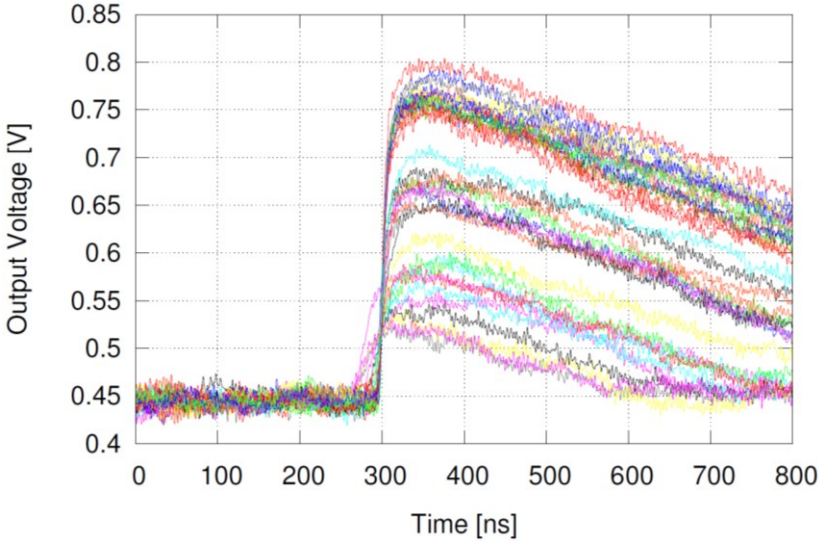
- A standalone characterisation was performed using bare C3PD chips, before receiving assemblies with the readout chip
- The chip has been tested using the internal test pulse injection, as well as with a ^{55}Fe source
- The results have shown an average charge gain of $190\ mV/ke^-$, an RMS noise of $40\ e^-$ and a rise time of $20\ ns$, for a power consumption of $\sim 5 \mu W$ per pixel (in continuous power mode)
- Samples thinned down to $50\ \mu m$ have been tested, apart from the standard thickness of $250\ \mu m$, without any observed impact on their performance

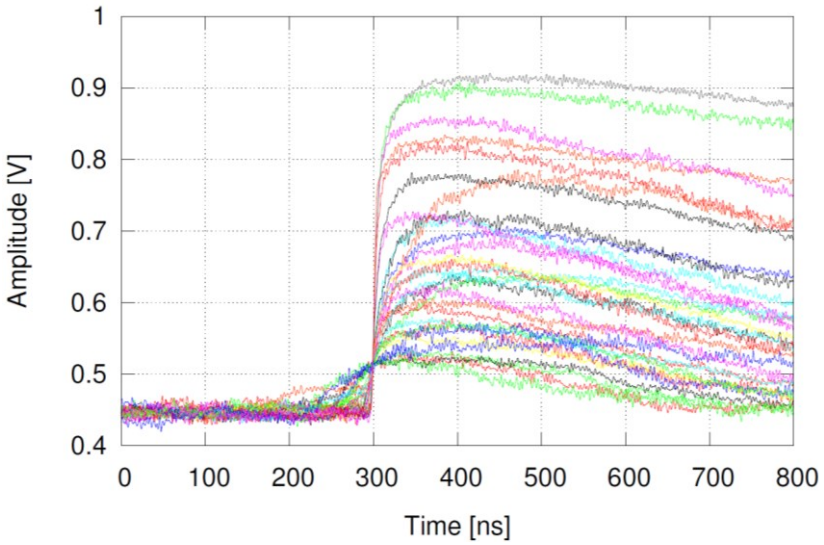




Measured output pulses

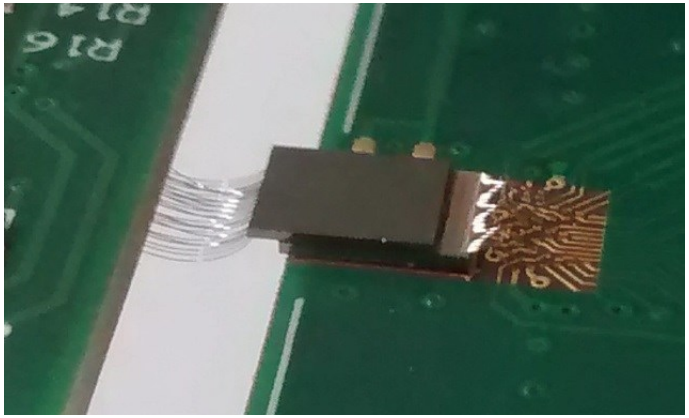
- Measured pulses at the output of one of the monitored pixels are presented for a test with a ^{55}Fe (left) and a ^{90}Sr source (right)





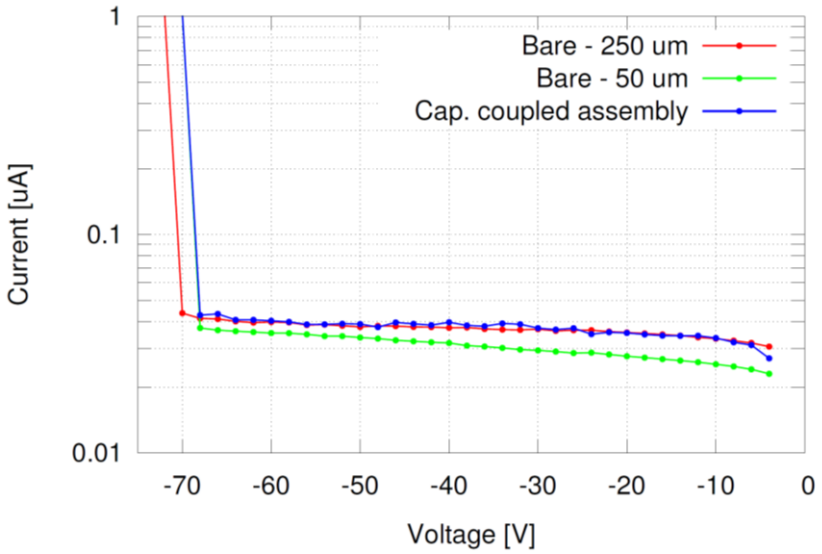
CLICpix2 and C3PD assembly

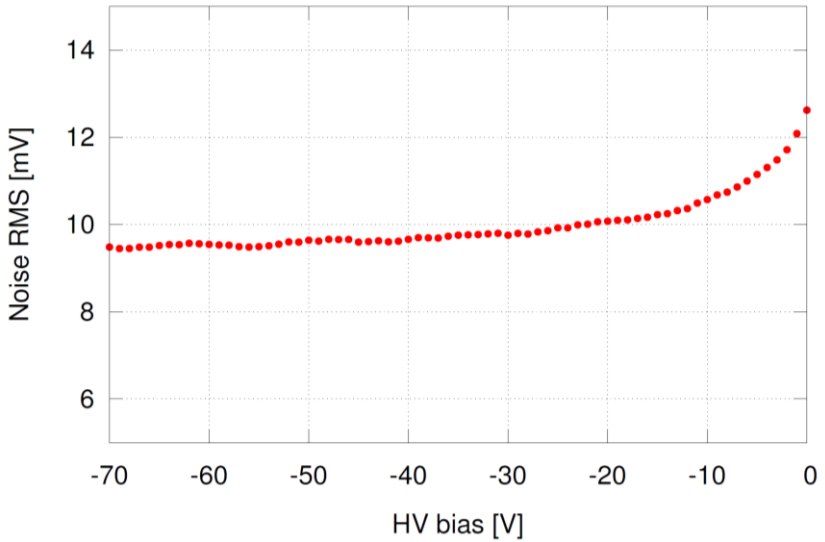
- Assemblies with the C3PD HV-CMOS sensor capacitively coupled to the CLICpix2 readout chip have been produced
- The chips are mounted and wire-bonded on a custom designed PCB, which is then connected to the CaRIBOu data acquisition system *[6] (see talk from A. Fiergolski)*
- Measurements on C3PD where performed with both the sensor and the readout chip operating in continuous power mode
- Due to the geometry of the glue assembly, it was challenging to illuminate the C3PD pixels using the ^{55}Fe source.
  The test was therefore performed using the C3PD internal test pulse injection



I-V characteristic

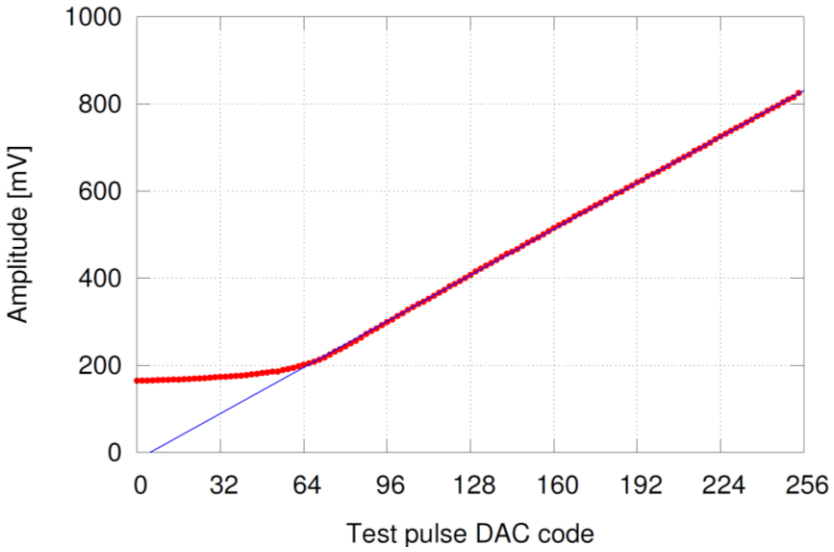
- The sensor leakage current was measured as a function of the applied HV bias
  - CLICpix2 was powered on during this measurement
  - At nominal bias of $-60\ V$: $I_{leak} \cong 40\ nA$
  - Breakdown voltage: $-70\ V$
  - The noise at the output of one of the monitored pixels was also measured as a function of the applied HV bias
  - Noise is minimised for a bias $< -40\ V$

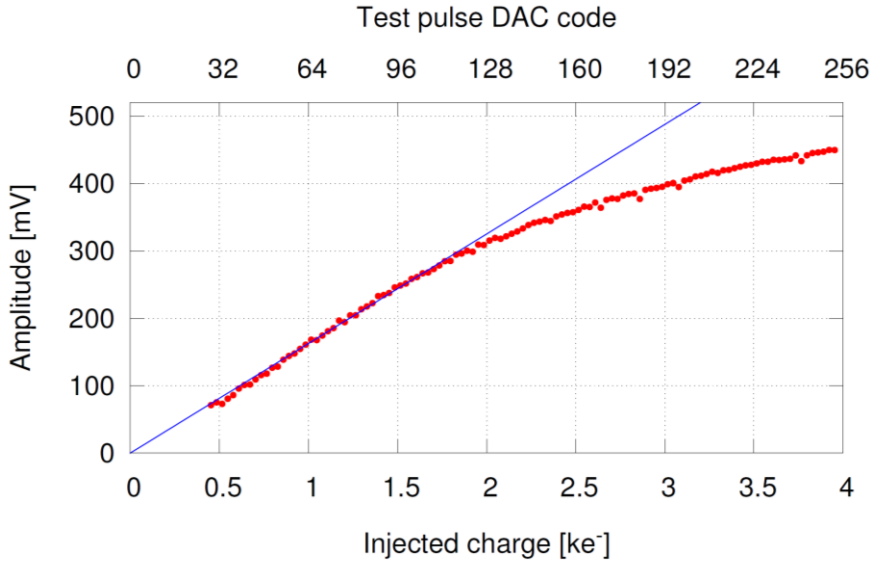




Internal test pulse injection

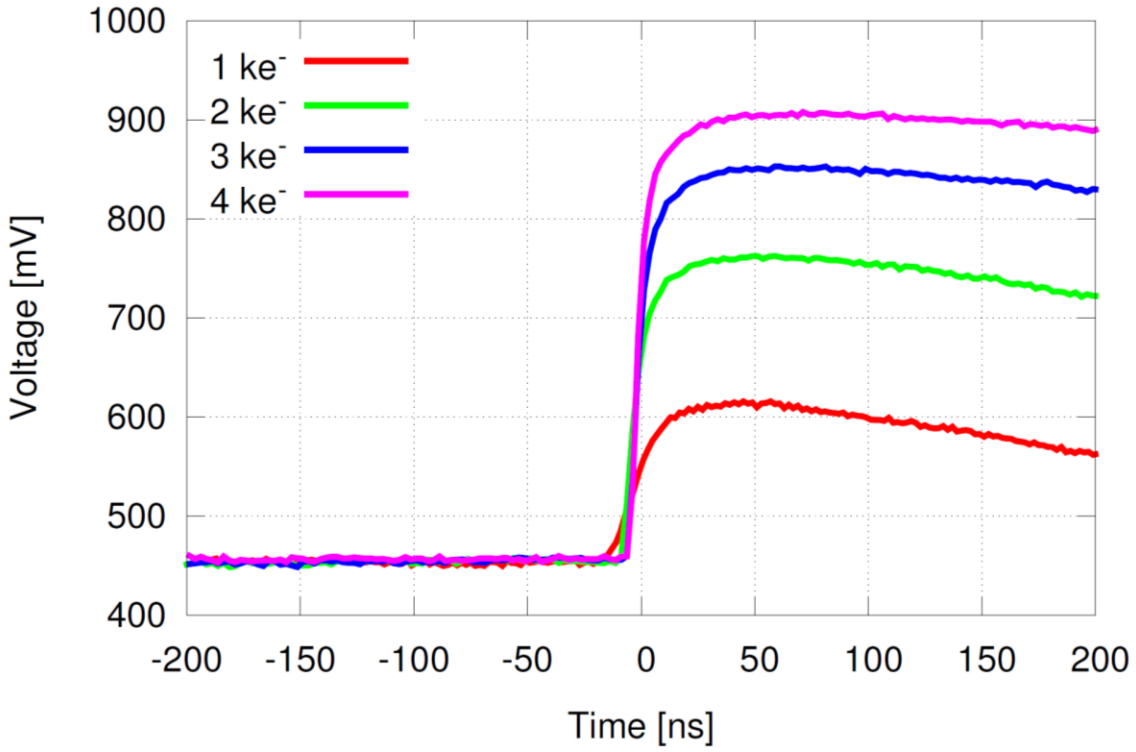
- The injected test pulse voltage was scanned as a function of the DAC code, using the C3PD test pulse monitoring pixel
- The output amplitude was measured as a function of the injected test pulse DAC code
  - The injected charge was calculated using the design value ($0.8fF$) for the test pulse injection capacitance (C_{test})





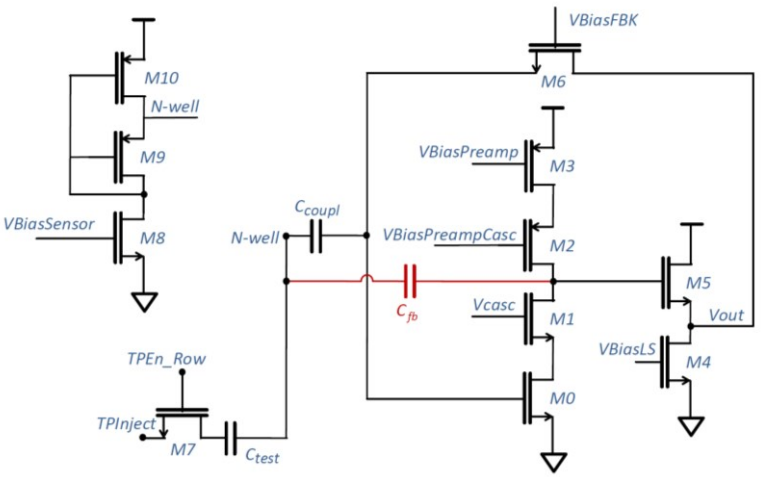
Internal test pulse injection

- Output pulse of the C3PD amplifier for different charges injected using the internal test pulse:

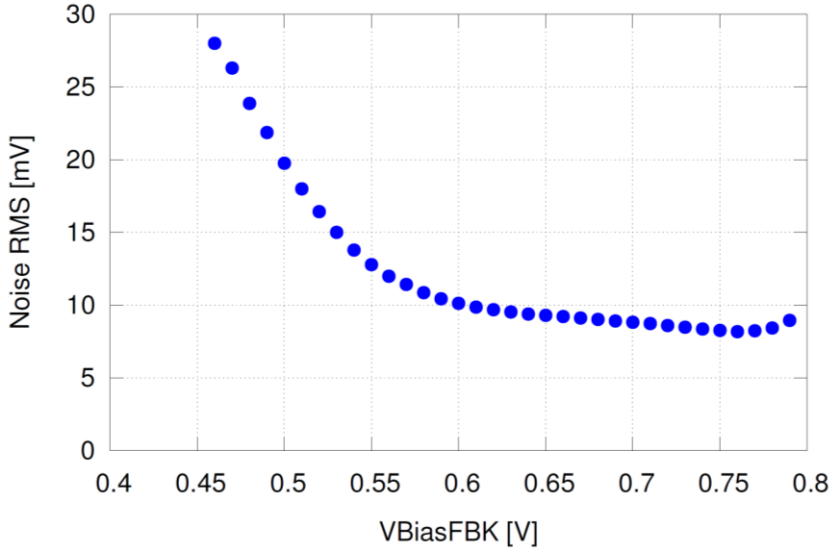


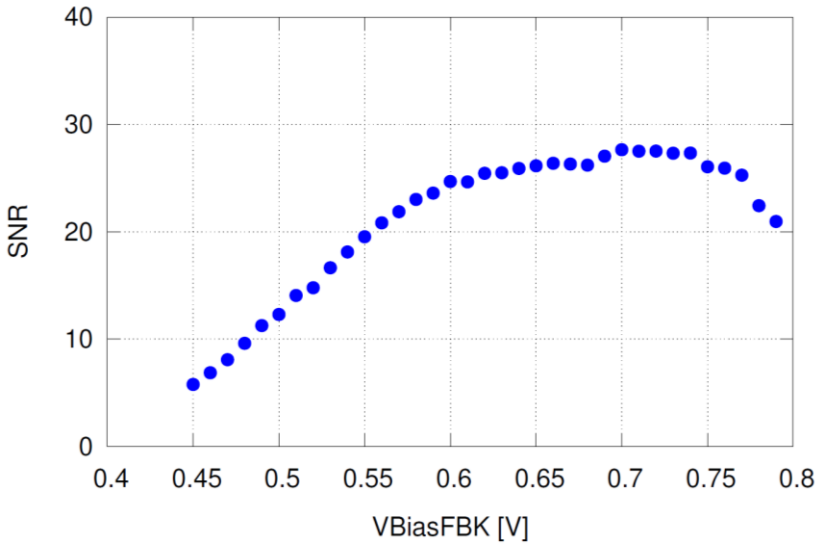
Calibration using test pulses

- Key parameters of the C3PD front-end were measured as a function of the biasing of different nodes of the front-end are presented
  - Injected charge: $\sim 1.63ke^-$ (using internal test pulse)
  - These scans were used in order to optimise the operating point of the C3PD front-end for the capacitively coupled assembly



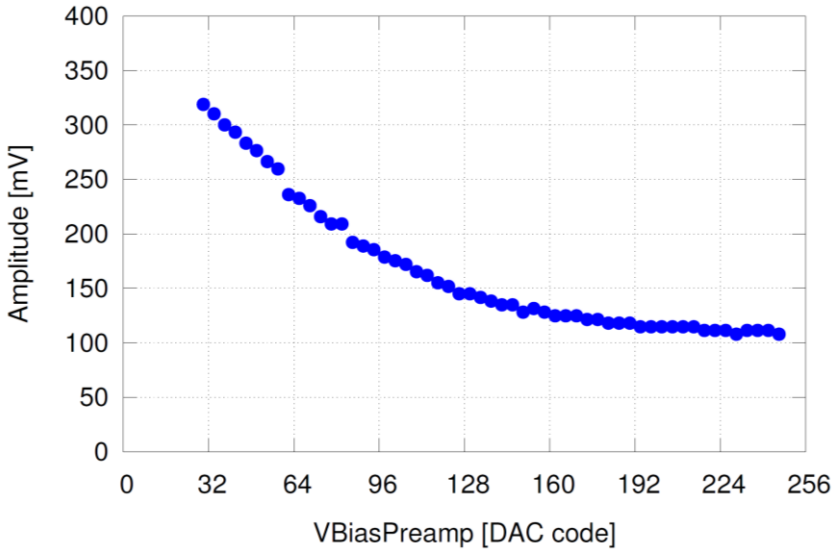
- Plots of the measured RMS noise (left) and Signal-to-Noise ratio (right) as a function of the feedback biasing

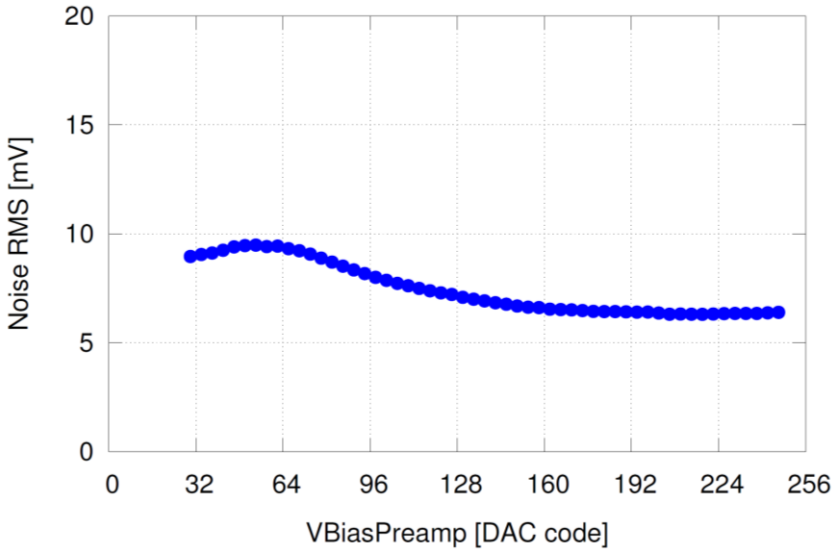




Calibration using test pulses

- Plots of the measured output amplitude (left) and RMS noise (right) as a function of the preamplifier biasing





- The operating point was selected such that the maximum Signal-to-Noise Ratio is achieved, while keeping a fast rise time ($\sim 20\ ns$). The power consumption needs to be kept at reasonably low levels.
  - For the selected operating point the average output amplitude was measured to be $278\ mV$, the RMS noise $7\ mV$ and the rise time $17.6\ ns$
  - The power consumption was estimated to be $\sim 5\ \mu W$ per pixel during 'power-on, and $\sim 95\ nW$ per pixel during 'power-off'

Summary and further testing

- The C3PD chip has been tested in standalone mode
  - Bare chips, as well as capacitively coupled assemblies have been tested
  - Samples thinned down to $50\ \mu m$ have been tested, without any observed impact on the sensor performance
  - The average power consumption over the $50\ Hz$ cycle of the CLIC beam was estimated to be $\sim 16\ mW/cm^2$ (assuming $30 \mu s$ to power cycle the chip)

- Further testing to be performed using capacitively coupled assemblies
  - Using the readout chip testing of C3PD is not restricted to a limited number of monitored pixels
  - Pixel-to-pixel mismatch, top-down effects and homogeneity across the pixel matrix will be studied
  - First results with capacitively coupled assemblies have already been obtained *(see talk from A. Nurnberg)*
  - A version of C3PD with higher resistivity wafers ($\sim 20, 80, 200$ & $1000\ \Omega\mathrm{cm}$) has been submitted and samples are expected to be received soon
  - Testing of the higher resistivity sensor chips will be performed using future capacitively coupled assemblies

References

[1] *I. Kremastiotis et al: Design and characterisation of a capacitively coupled HV-CMOS sensor for the CLIC vertex detector (2017), https://cds.cern.ch/record/2261927*

[2] *E. Santin, P. Valerio andA. Fiergolski: CLICpix2 User's Manual (2016)*

[3] *N. Alipour Tehrani et al., Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector (2016) https://doi.org/10.1016/j.nima.2016.03.072*

[4] *S. Kulis and A. Fiergolski: C3PD-sc – A slow control interface for C3PD chip (2016)*

[5] *M. Buckland: TCAD simulations of High-Voltage-CMOS Pixel structures for the CLIC vertex detector (2016), https://cds.cern.ch/record/2159671/*

[6] *A. Fiergolski: A multi-chip data acquisition system based on a heterogeneous system-on-chip platform (2017), https://cds.cern.ch/record/2272077/*

Back-up

C3PD Double Pixel Layout