# SEE Single Event Effects

Radiation Environment and its Effects in EEE Components and Hardness Assurance for Space Applications

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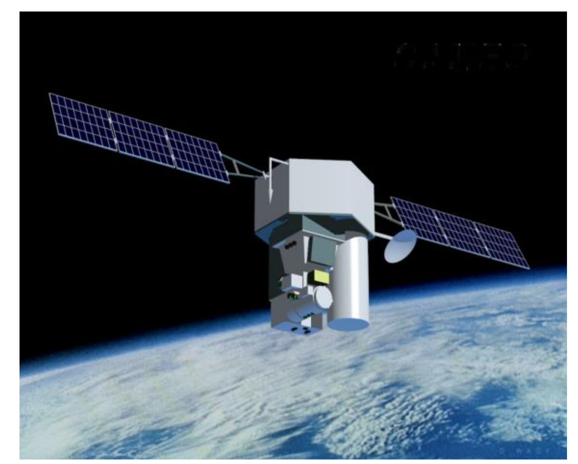
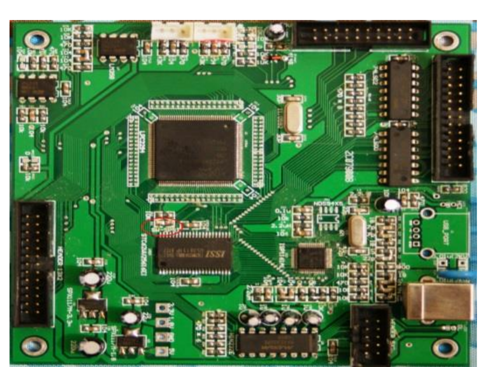
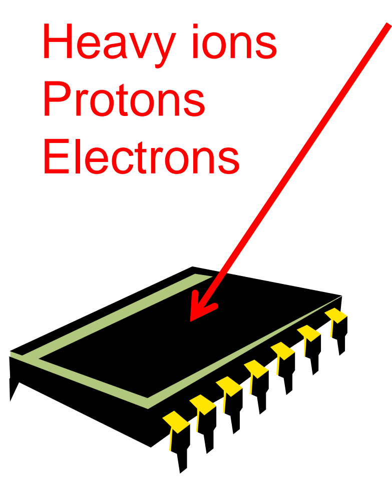
# Single event effects in space environment

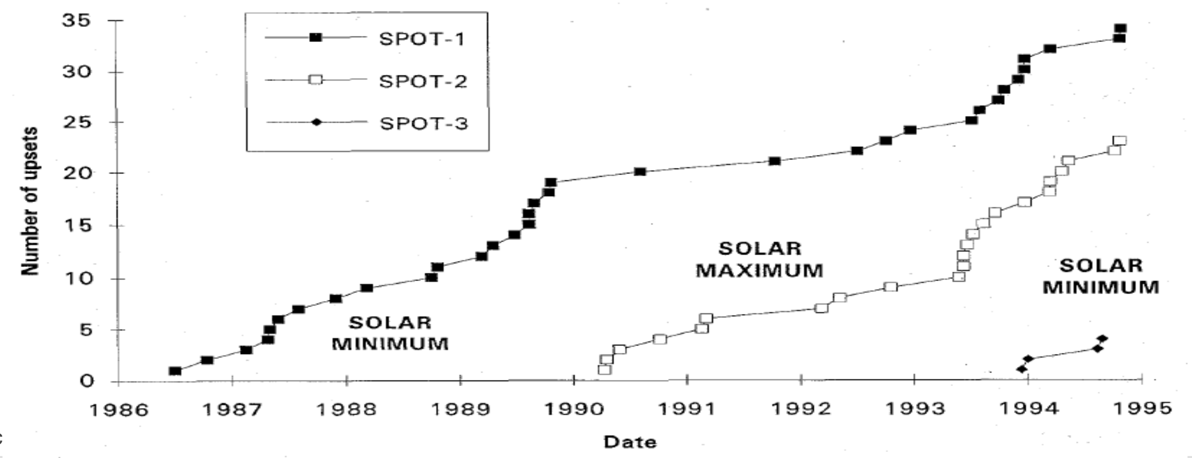






# Historical facts

- **1975: [Binder]** first reported “single event effect” SEE anomalies; unexpected triggering in bipolar digital circuits due to cosmic rays
- **1978 – 1985**: SEUs in Pioneer 12 (Venus probe), in a 1024 bit PMOS shift register
- **1985-1995**: SEU example in the OBC of Spot1-2-3; Half of these SEUs lead to operational problems, including switching the satellite to safe mode.




*[R. Ecoffet, TNS 1995-2013]*

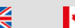
# Outline

- SEE basic mechanisms
  - Beam: LET, range, energy
  - Counting events, cross-section

- Different types of SEEs
  - SEU, SET SEL SEB SEGR
  - New effects: MBUs, proton and electron direct ionization

- Practical aspects of SEE testing
  - Checking the beam
    - PIN diode, SEU monitor, RPUM
  - Statistics, Uncertainties, Error Bars
  - Part-to-part variations





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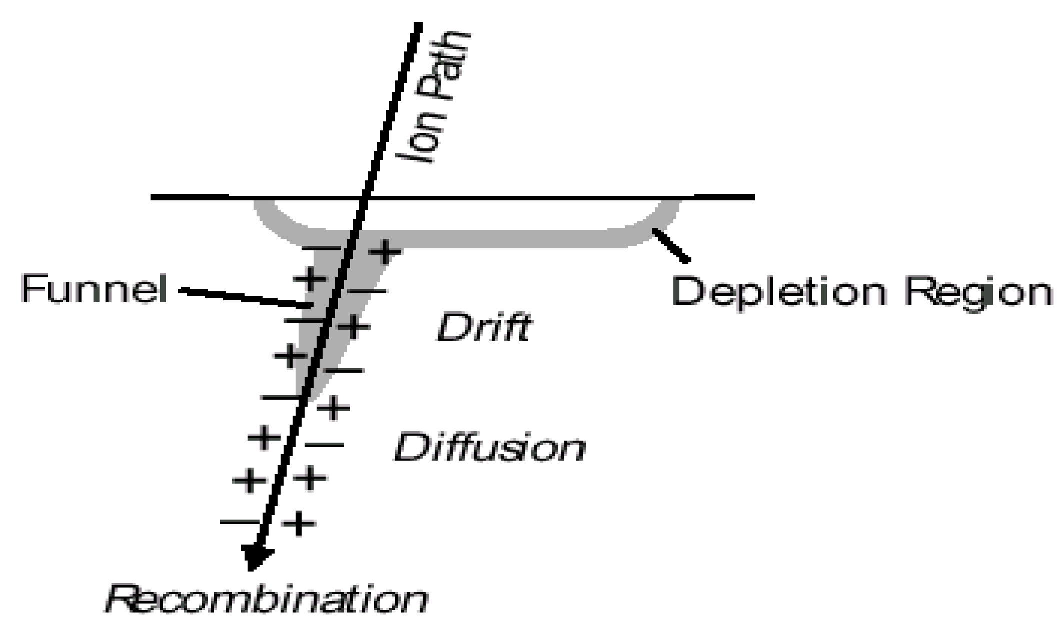
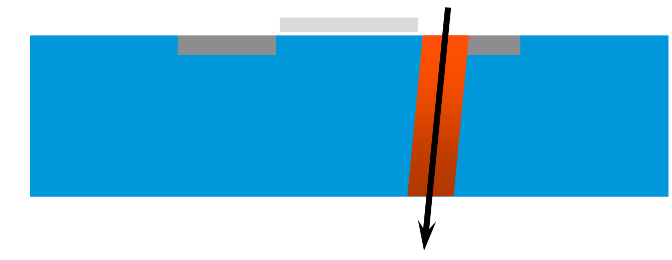
# SEE basic mechanisms



# Both Heavy ions ($Z \geq 2$), protons can induce SEE

## Heavy ion

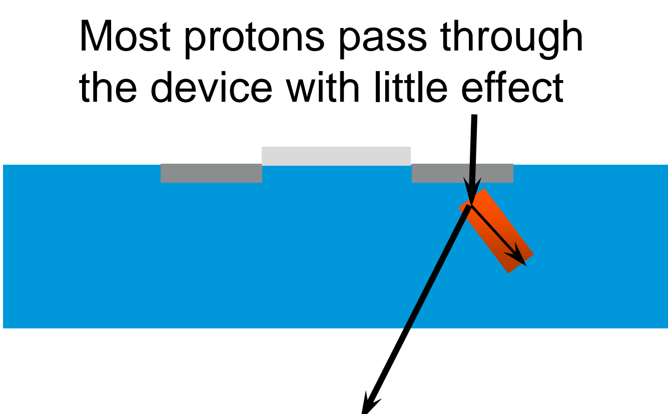
Each ion produces
an ionizing track



Direct energy deposition by the ion along the track.

## High energy proton electron or neutron

Most protons pass through the device with little effect



A few protons ($\sim 10^{-5}$) cause nuclear reactions

Short range recoils produce ionization

Energy mainly deposited by fragments of nuclei, from inelastic collision between a proton and a silicon nucleus. The fragments usually deposit in turn all their energy along their track or produce a cascade of particles.

# Ion deposited charge: Linear Energy Transfer

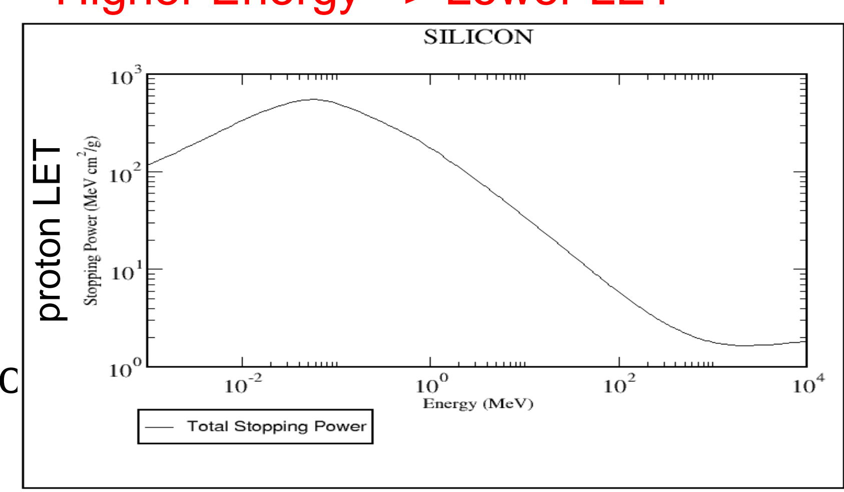
$$\text{Dose}\,[\text{rad(Si)}] = \text{LET}\,[\text{MeVcm}^2/\text{mg}] \times \text{Fluence}\,[\text{cm}^{-2}] \times 1.6\,10^{-5}\,[\text{mg rad/MeV}]$$

$$\text{LET} = \frac{1}{\rho}\frac{dE_d}{dx} \quad [\text{MeVcm}^2/\text{mg}]$$

LET (MeVcm²/mg) vs. Travel distance in Si (μm) — RADEF 9.3 MeV/amu; curves: Xe, Kr, Fe, Ar, Si, Ne, N

Higher LET => Lower range

Higher Energy => Lower LET



# Example of test facility: RADEF

# Example of ion beam cocktail at RADEF

**9.3 MeV/amu cocktails (M/Q≈3.7, ‡M/Q≈3.3).**

| Ion | Energy [MeV] | $LET^{MEAS}$ @surface [MeV/mg/cm²] | $LET^{MEAS}$ @Bragg peak [MeV/mg/cm²] | *$LET^{SRIM}$ @surface [MeV/mg/cm²]* | *$Range^{SRIM}$ [microns]* | *$LET^{SRIM}$ @Bragg peak [MeV/mg/cm²]* |
|---|---|---|---|---|---|---|
| $^{15}N^{+4}$ | 139 | 1.87 | 5.92 (@191 um) | *1.83* | *202* | *5.9 (@198 um)* |
| $^{20}Ne^{+6‡}$ | 186 | 3.68 | 9.41 (@138 um) | *3.63* | *146* | *9.0 (@139 um)* |
| $^{30}Si^{+8}$ | 278 | 6.74 | 13.7 (@114 um) | *6.40* | *130* | *14.0 (@120 um)* |
| $^{40}Ar^{+12‡}$ | 372 | 10.08 | 18.9 (@100 um) | *10.2* | *118* | *19.6 (@105 um)* |
| $^{56}Fe^{+15}$ | 523 | 18.84 | 29.7 (@75 um) | *18.5* | *97* | *29.3 (@77 um)* |
| $^{82}Kr^{+22}$ | 768 | 30.44 | 41.7 (@68 um) | *32.2* | *94* | *41.0 (@69 um)* |
| $^{131}Xe^{+35}$ | 1217 | 54.95 | 67.9 (@57 um) | *60.0** | *89** | *69.2 (@48 um)* |

# Charge collection by drift and diffusion

3
2
1
0
Drain current (mA)

drain

fast collection by
funneling (drift)

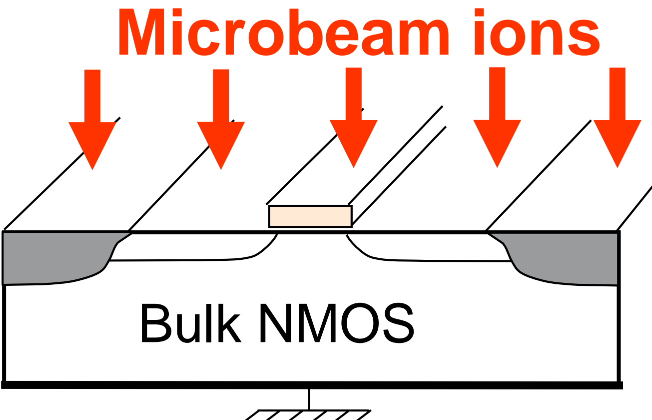
slower collection
by diffusion

source

-0.5 0.0 0.5 1.0 1.5 2.0

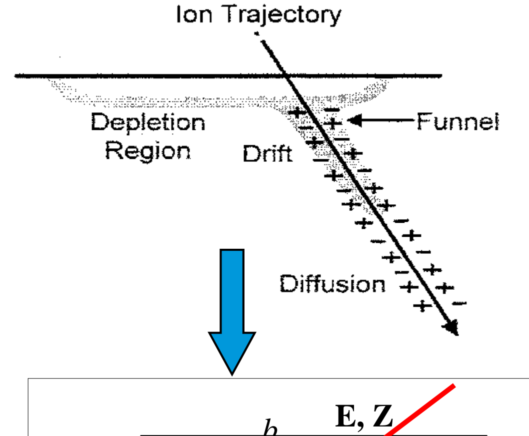
Time (ns)

[Ferlet-Cavrois, 2006]

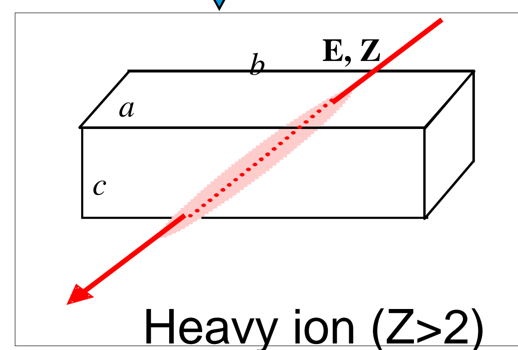


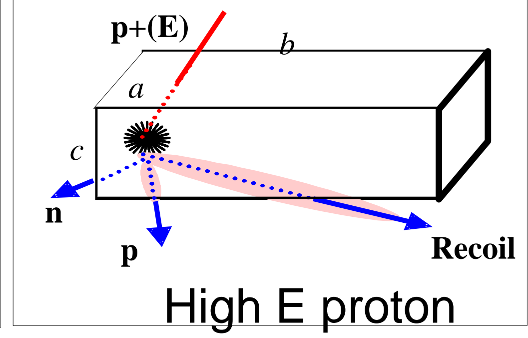

Multiple pulse amplitudes and shapes are measured depending on the ion strike location

# Sensitive Volume SV




The volume responsible for charge collection for a SEE (in $\mu m^3$)



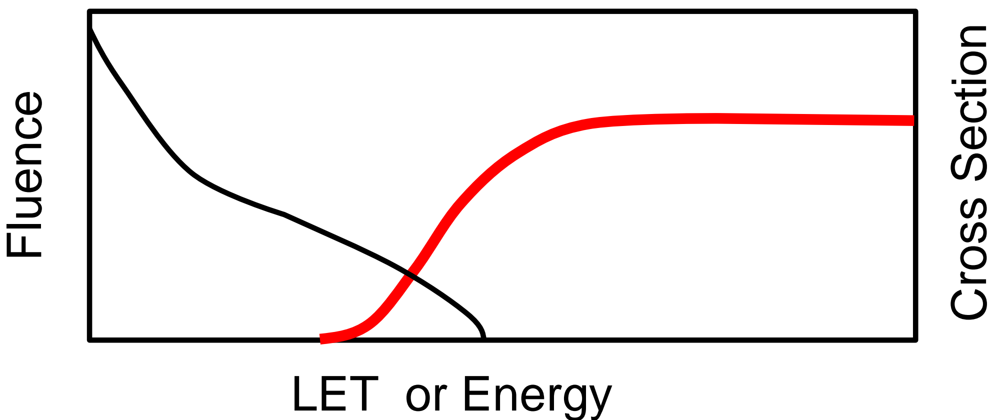

Real sensitive volumes do not really have regular shapes and therefore, not only incidence angle but also pitch and roll may have an impact in the total amount of charge collected.

# Why SEE testing? For SEE rate prediction

Need to know:

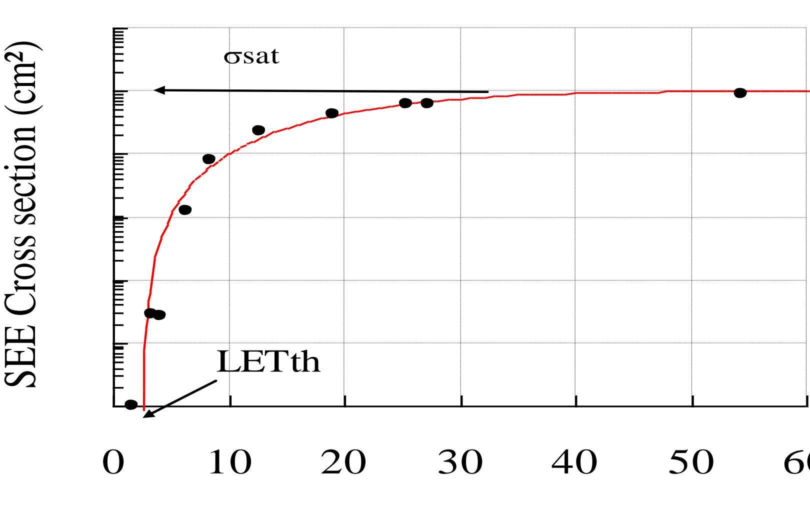
a. Space Environment: Integral flux as a function of LET or energy

b. **Cross-section vs. ion LET or proton energy**



# SEE Cross Section Curve vs LET

The SEE cross section measures the probability for a SEE to occur




$$[\mathrm{cm}^2] \longrightarrow \sigma = \frac{N_{events}}{\mathrm{Fluence}} \longleftarrow [N_{particules}/\mathrm{cm}^2]$$

Fit with Weibull (integral form)

$$\sigma = \sigma_{sat}\left(1 - \exp\left(\frac{LET - LET_{th}}{W}\right)^{S}\right)$$

W and S are fitting parameters

SEE cross-section is a crucial input for in-orbit SEE rate prediction.

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# Some Classes of SEE

Soft Errors (no permanent damage)

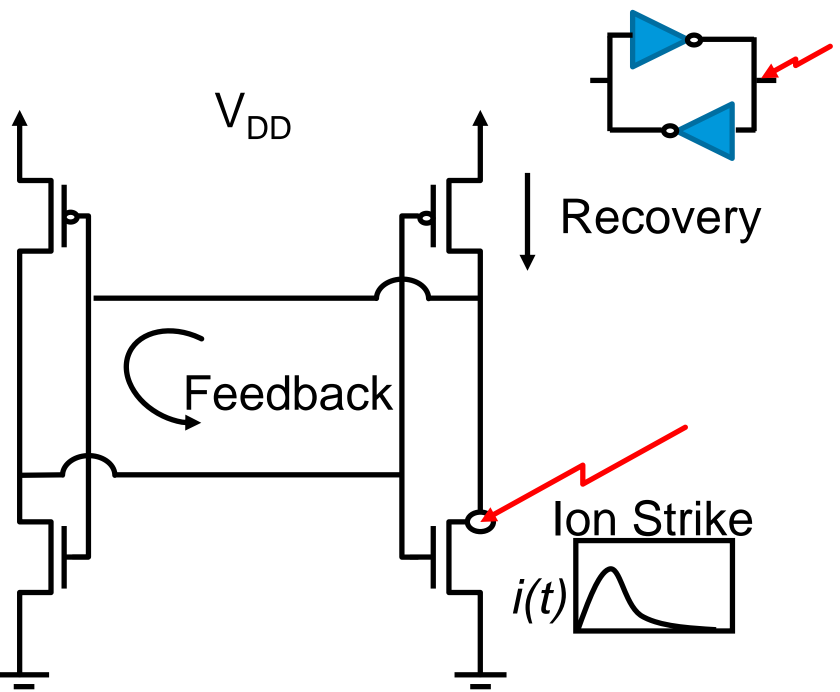
- SEU Single-Event Upset
- MBU, MCU Multiple Bit (or Cell) Upset
- ASET Analog Single Event Transient
- DSET Digital Single Event Transient
- SEFI Single Event Functional Interrupt

Hard Errors (permanent damage to device/circuit)

- SEL Single-Event Latchup
- SEHE Single-Event Hard Errors
- SEDR Single-Event Dielectric Rupture
- SEB Single-Event Burnout
- SEGR Single-Event Gate Rupture
- Destructive events

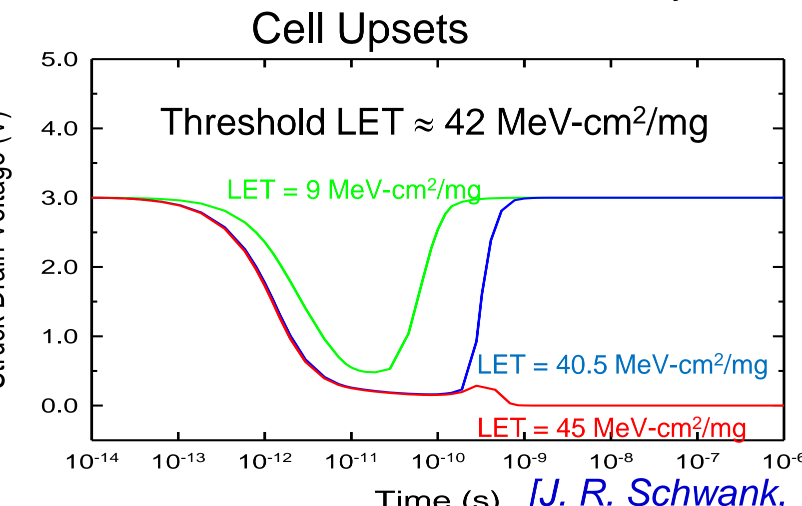
*This is not a complete listing of all possible single-event effects!!*

# Single-Event Upset in SRAMs: The Feedback Mechanism




## Race Condition

Recovery occurs before feedback:
No Upset
Feedback occurs before recovery:
Cell Upsets




*[J. R. Schwank, P. E. Dodd, 2001]*

*SEU is a circuit effect initiated at the device level.*

# Multiple Cell Upset (MCU)

IT#64 zoom 1

IT#64

IT#64 zoom 2 (2 MCUs)

IT#64 zoom3 Other MCU example

40nm SRAM
Tilt=0, Roll=90,
Xenon, UCL

smaller cells
=> more MCUs

*[ESTEC contract 18799/04/NL/AG*
*Hirex SEE test report, HRX/SEE/0288*
*STMicroelectronics 40nm SRAM]*

*One ion strike can induce more than 100 cell upsets*

# SEU sensitivity for low energy protons (1)

Memory Devices with very low LET thresholds are sensitive to proton-induced SEU set by **direct ionization**.

Bulk 65nm SRAM

GSFC
LBNL
UC Davis
IU
Bendel

Cross Section ($cm^2$/bit)

Proton Energy (MeV)

[B. Sierawski, TNS 2009]

**Proton Sensitivity 65-90nm SRAMs**

CY 90nm QDR
CY 65nm QDR
TI 65nm eSRAM
BAE 90nm eSRAM
IBM 90nm eSRAM

Proton Bit X-section [$cm^2$]

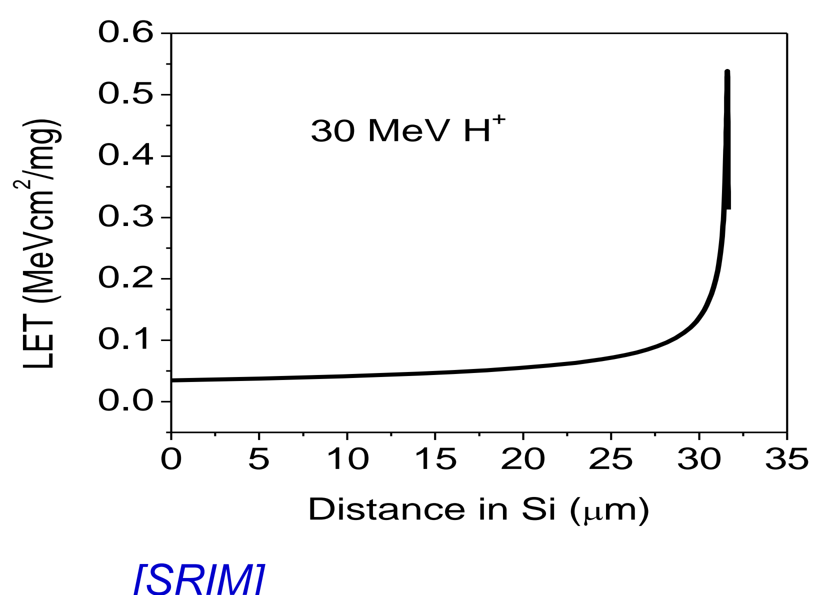
Proton Energy [MeV]

[H. Puchner, REDW 2011]

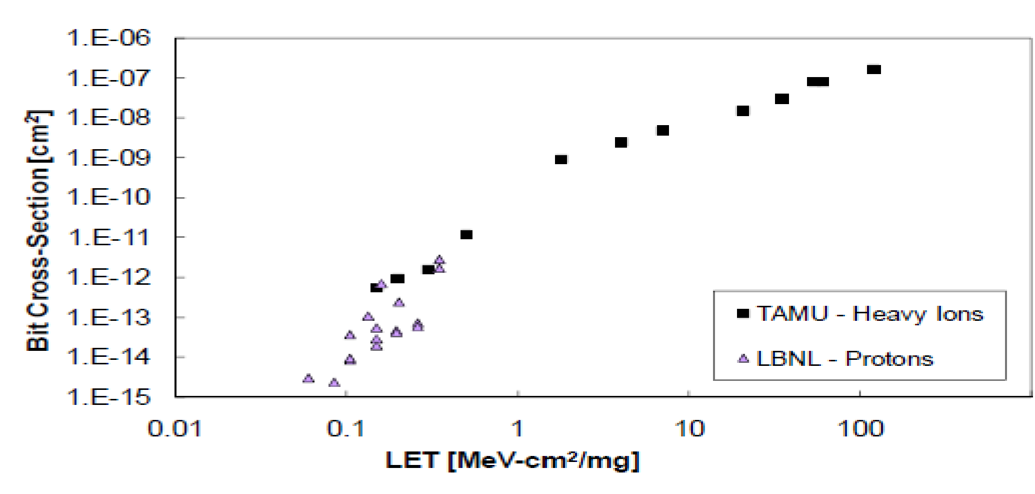
State of the art memories (Higly scaled devices) have very low LETth and can be prone to proton direct ionization.

# SEU sensitivity for low energy protons (2)

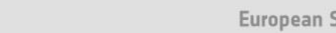
*Protons have a low LET and relative low penetration compared to heavier ions but can be very abundant depending on the orbit or during solar flares.*



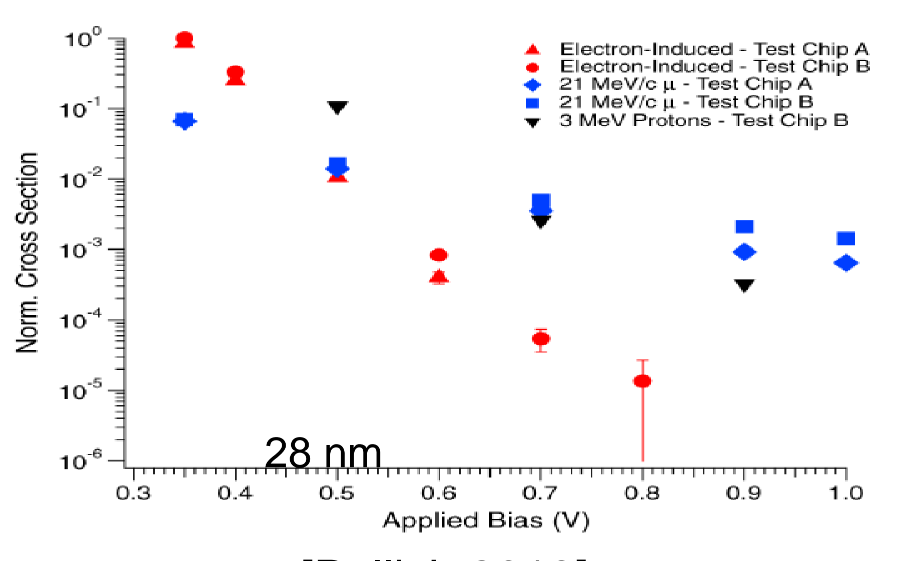

*[SRIM]*



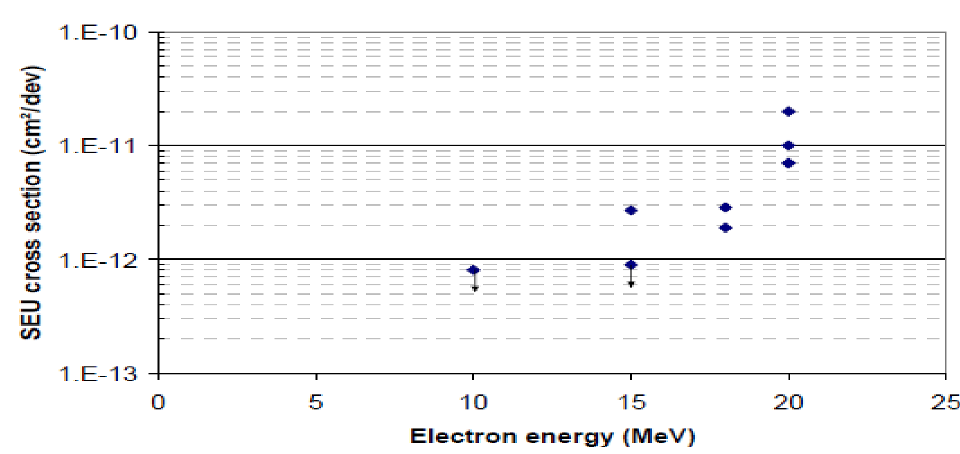

*[H. Puchner, REDW 2011]*



# SEU sensitivity for high energy electrons




[Pellish 2013]




[Samaras 2014]

*New highly integrated technologies may be sensitive to electron induced SEE. This could be an issue in Jupiter environment. Technology evolution may even lead to direct ionization by low energy electrons.*

# Single-Event Transients in Digital Logic Circuits (DSETs)

Ion Strike

v(t)

Data

Clock

1

2

3

4

Inverters (combinational)

D-Latch (sequential)

*[Buchner, TNS Dec.1997]*

*A strike on the inverter shortly before a clock edge can pass bogus data into the D-latch.*

# DSET propagation increases with frequency

esa

Error Rate (Arb. Units)

100
10
1
0.1

Sum
Combinatorial Logic
Sequential Logic

1
10
100

Frequency (Arb. Units)

Propagated SETs from inverter strikes

D-Latch errors

*[Buchner, 1997]*

*As clock edges come more frequently, the probability of a transient being captured and propagated to subsequent circuitry increases.*

Trend in new technologies: combinatorial SET pulses are becoming larger than gate transition times and can propagate. Single event rates in combinatorial logic are becoming comparable to those in latches.

# Example of DSETs measured at the output of a chain of logic cells

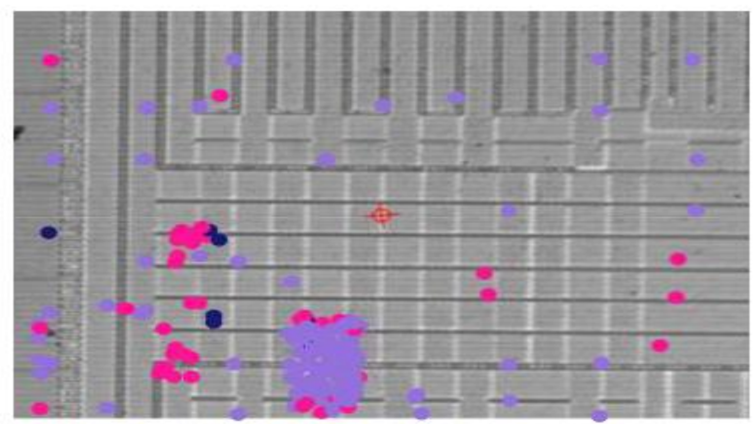
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
Voltage (V)
-1 0 1 2 3 4
Time (ns)
130nm logic

*[Ferlet-Cavrois07]*

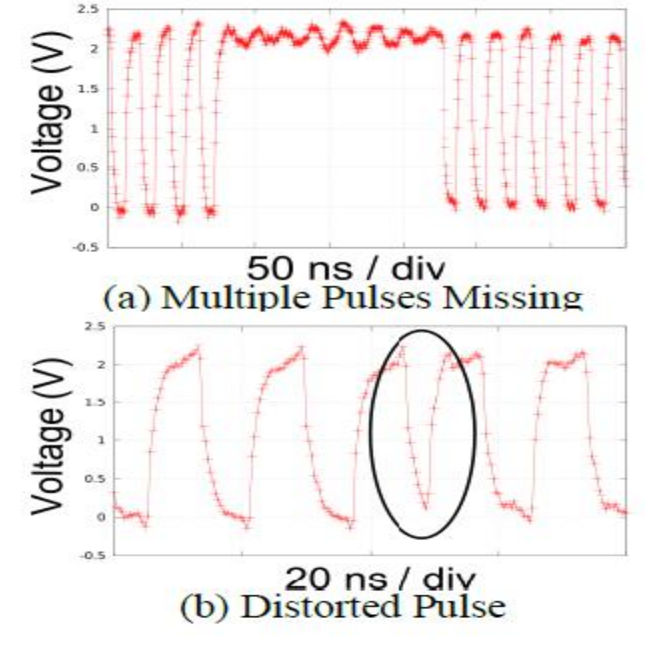
- "Rail-to-rail" transients
- Large variety of SET duration, depending on the ion strike location within the logic path
- The modelling of SET propagation is layout dependant
- New generation technologies are particularly prone to DSETs

# SET glitches in PLL built in ProASIC3 FPGA

*[A. Evans, iRoC Tech., IRPS 2015]*



Micro-beam experiment
PLL sensitive region
Au ions, 144 µm × 144 µm




Sample glitches

# SETs in Complex Circuits

Cross Section ($cm^2$)

1.0e-07
1.0e-08
1.0e-09
1.0e-10
1.0e-11
1.0e-12
1.0e-13

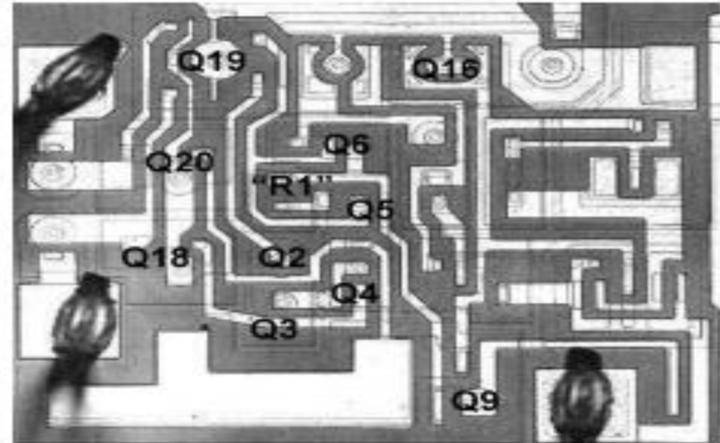
Ne
Ar
Kr

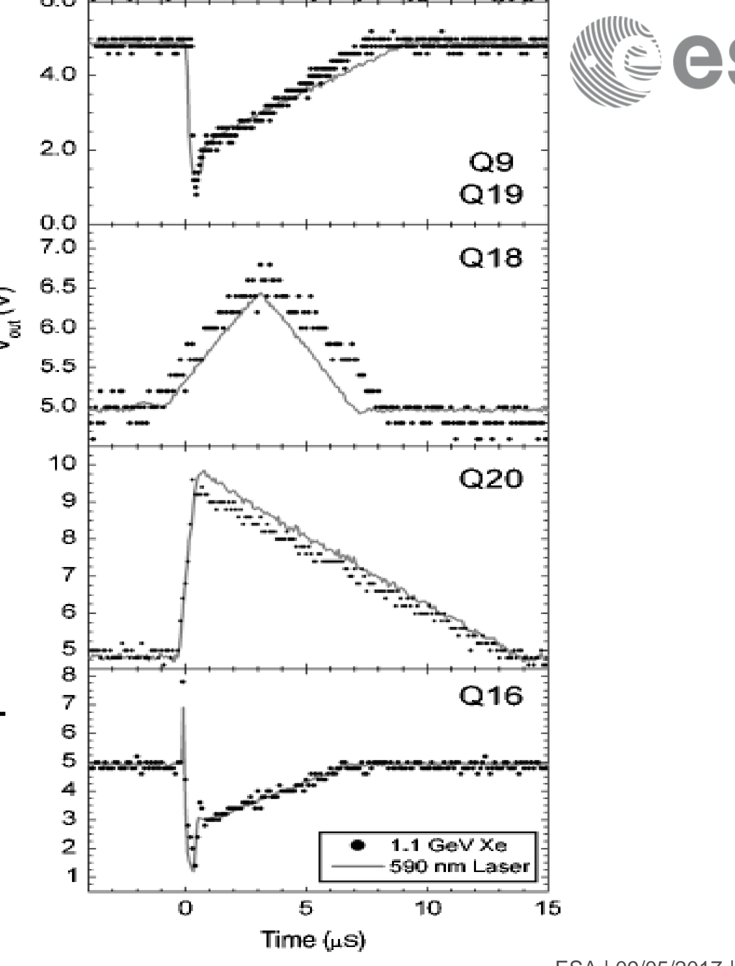
ADDER A
ADDER B
ECC DECODER
ECC ENCODER
MAG COMPARE
MUX8
PRI ENCODER32
SM LOGIC

- Cross section normalized per-gate
- 50 MHz operation
- Significant variation (close 10x) depending on circuit function

# Analog SET - ASET: Example in lm124

*[Buchner, 2004]*

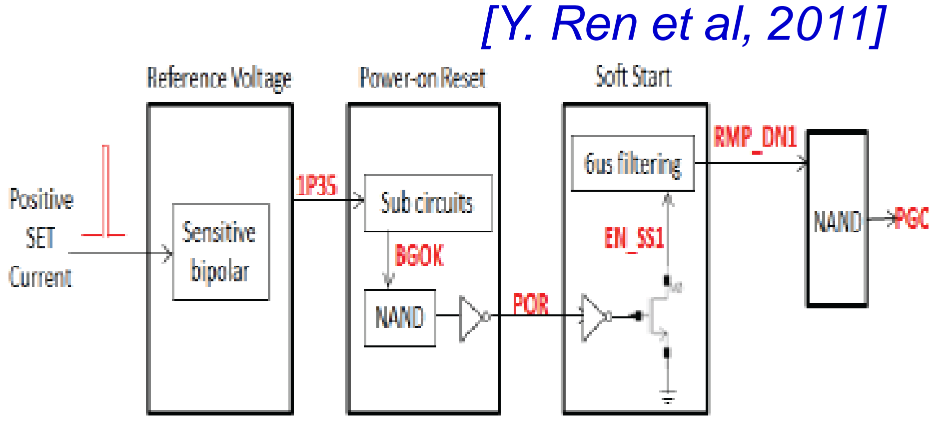


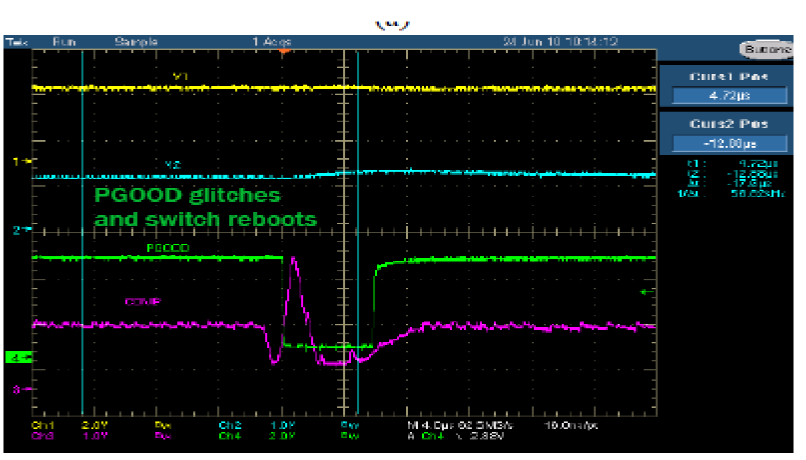




- The output signal displays different ASET shapes depending on the strike position,
- May affect subsequent circuits if not well filtered in the design

# ASET on a DC-DC converter

*[Y. Ren et al, 2011]*

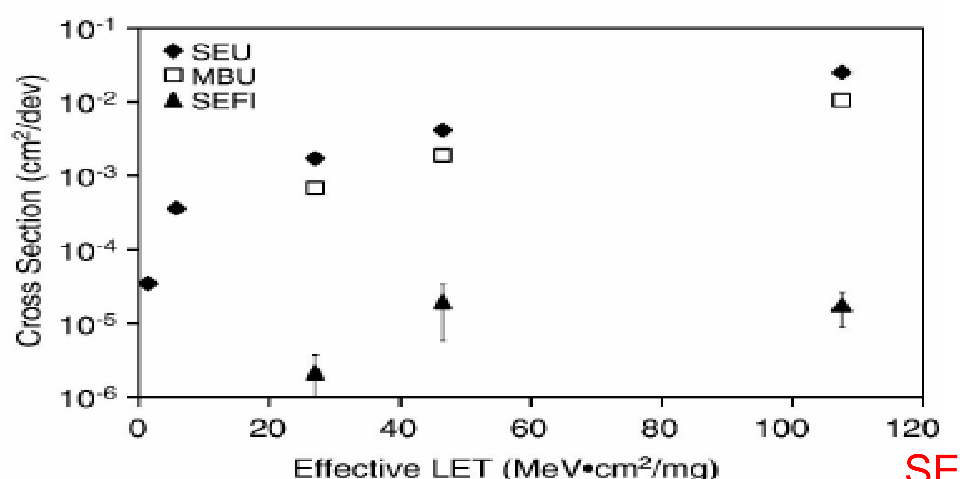


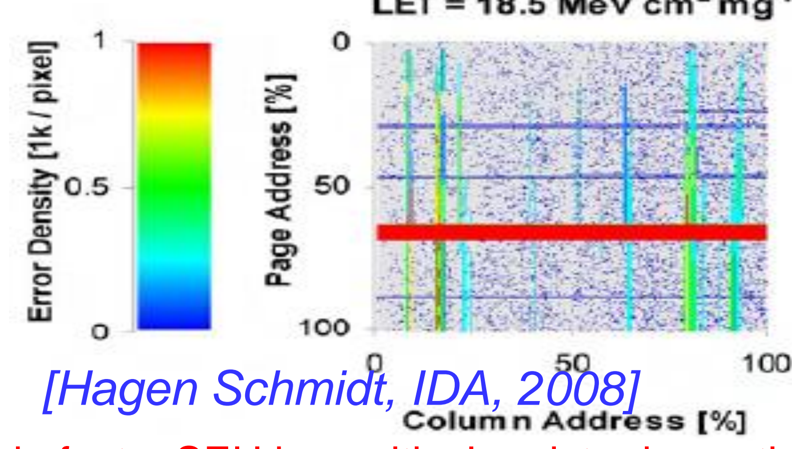




The single event transient (SET) pulses on the internal reference voltages (band gap references) propagate to the soft start circuits which falsely triggers a short alert signal to the system. This results in a reset and thus an output power drop that will last the required time to discharge and charge the soft start capacitor.

# SEFI, may appear in complex digital sequential devices, for example in SDRAM, CPU, ADC, DAC, FPGA, POL, memories …

8-Gbits NAND-Flash, Samsung




*[Hagen Schmidt, IDA, 2008]*

SEFI is in fact a SEU in a critical register impacting the device’s functionality.

SEFI in a memory:

- Rows, columns, blocks are in error;
- Need reset or power cycling
- Mitigated by decreasing the refresh time

SEU-MBU-SEFI-SEL:

Effect of die revision: x$10^2$ SEE rate

Lot-to-lot variations

*[Ladbury 2006]*

# Single Event Latch-up, SEL

Integrated devices contain parasitic structures due to the proximity of their transistors.

Substrate Contact
V
Well Contact
p + n + n + p + p + n +
$r_{bv}$ $r_{sv}$ n-well
$r_{sl}$ $r_{bl}$ $r_s$
p-substrate

I
$I_H$
$I_L$
$V_H$ $V_L$ V

An ion strike can trigger the PNPN parasitic structures present in CMOS devices,
This may create a low resistance path between power and ground.

# SEL Facts

- Self-sustained current, only recovered by power cycle
- SEL increases with temperature
- Modern devices may have different latchup paths
  - Both high current and low current SELs can occur
- Characterization of SEL requires long range ions
- *SEL is a critical effect with potential catastrophic impact on spacecraft systems*
  - *SEL sensitive components shall as far as possible be avoided*

# SEL increases at high temperature

Temperature Dependence of Basic Parameters

$V_{BE}$ drops from 0.7 to 0.5V at 125 °C
Well resistance doubles at 125 °C
compared to room temperature

125°C
60°C
20°C

***Saturation cross section increases with temperature***

***Threshold LET decreases with temperature***

Latchup Cross Section ($cm^2$)

$10^{-2}$
$10^{-3}$
$10^{-4}$
$10^{-5}$
$10^{-6}$

0 5 10 15 20 25 30 35

LET (MeV-$cm^2$/mg)

*[JPL course by L.Scheick]*

# Single Event Hard Errors: stuck bits

## Samsung 1Gbits DDR1 SDRAM

Large part to part variations
*[Edmonds 2001]*

## Hyundai 64-Mb SDRAM

Due to Micro-dose or displacement damage
*[Edmonds 2008]*

Bit Cells that can not be wrote any more, their content is stuck.

They may recover with time, or not.

Can beat EDAC, in the past they appeared at EOL, now may occur at BOL

# DDR3 results – Stuck bits

Hard SEUs: can not be removed by rewriting

*[M. Herrmann, IDA, 2014]*

Cross section [cm² / bit]
1E-11
1E-13
1E-15
1E-17
1E-19

0 10 20 30 40 50 60 70 80

LET [MeV cm² / mg]

Cross section [cm² / device]
4E+0
4E-2
4E-4
4E-6
4E-8
4E-10

4 Gbit Samsung - SEU
4 Gbit Samsung - hard SEU
4 Gbit Elpida - SEU
4 Gbit Elpida - hard SEU

# Stuck bits in NAND-flash

1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
1.E-15
1.E-16
1.E-17

0 10 20 30 40 50 60

LET [MeV mg⁻¹ cm²]

$\sigma_{SEU}$ [cm² bit⁻¹]

Chip Area / bit [cm² bit⁻¹]

16-G Micron

significant soft SEU Annealing only at Nitrogen

SEU = soft SEU + hard SEU

SEU, Micron 16-Gb
soft SEU after 20 days, Micron 16-Gb
hard SEU, Micron 16-Gb
hard SEU after 20 days, Micron 16-Gb

Page Address

60 50 40 30 20 10 0

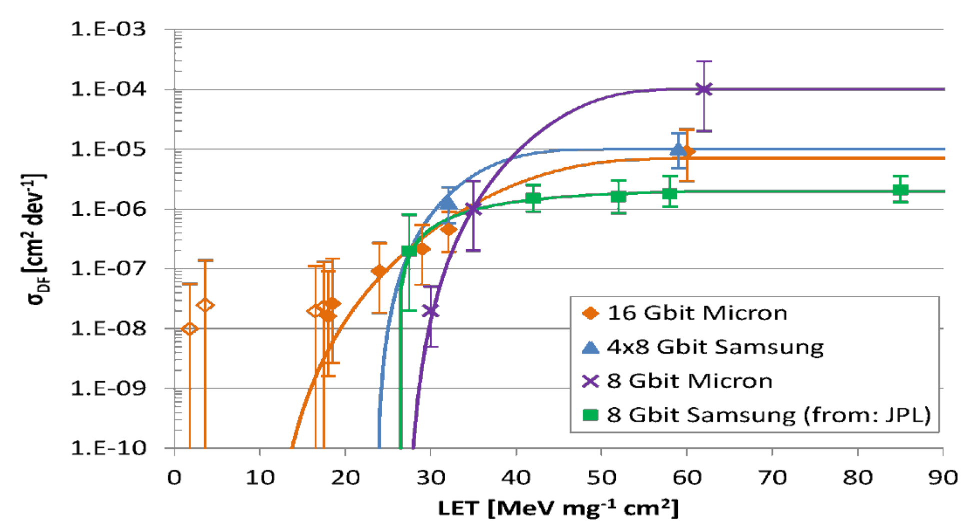
0 200 400 600 800 1000 1200 1400

Byte Address

soft SEU
hard SEU

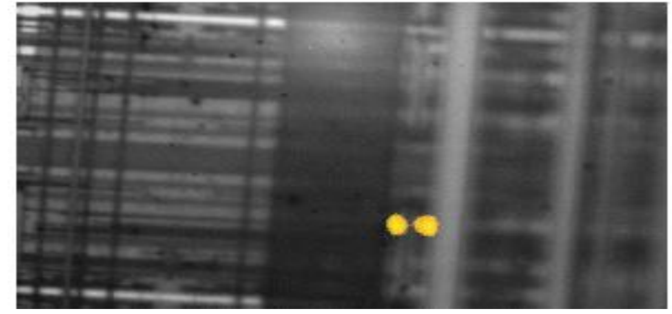
*[K. Grürmann, IDA, 2012]*

# Destructive events in NAND-Flash




*[K. Grürmann, IDA, 2012]*

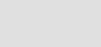
Samsung 8Gb NAND-Flash



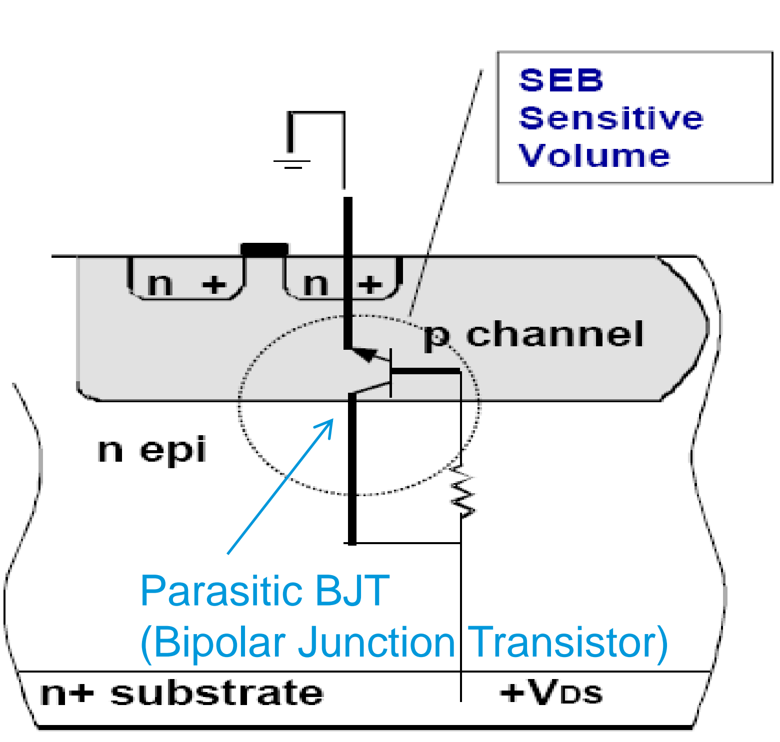
Thermal picture charge pump region

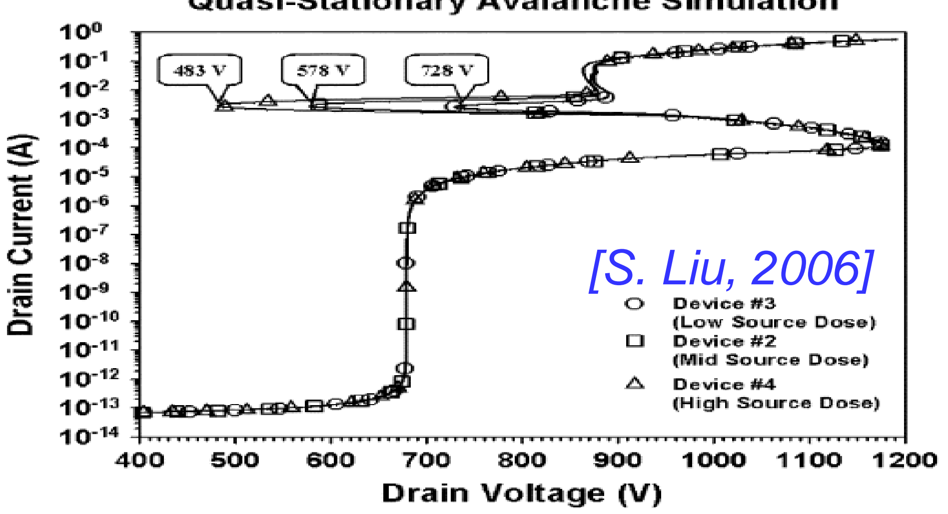
*[F. Irom, TNS Feb. 2010]*

- Permanent damage with indefinite data loss
- 16 Gbit Micron shows also other failure types affecting the on-chip microcontroller



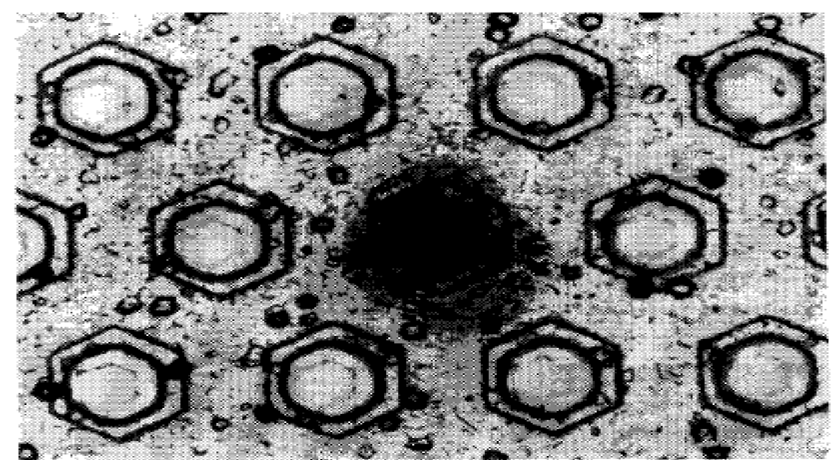
# Single Event Burnout SEB

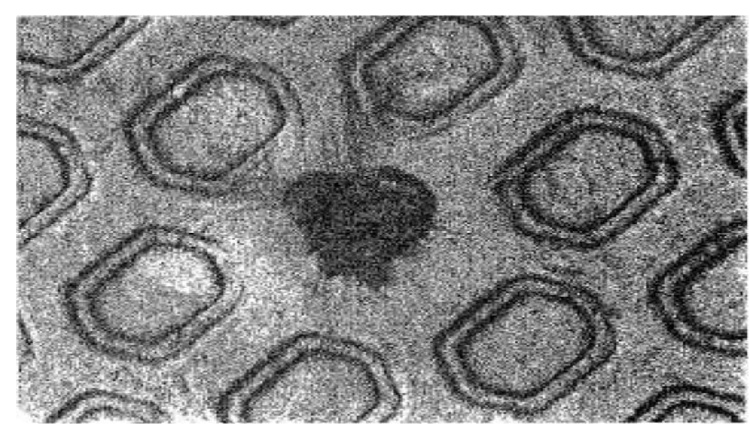



- Triggered by heavy ions, and possibly by protons and neutrons
- Always destructive
- power BJTs, FETs, MOSFETs are sensitive to SEB

# SEB damage in MOSFETs, IGBT





IGBT damage

*[E. Lorfèvre, 1998]*

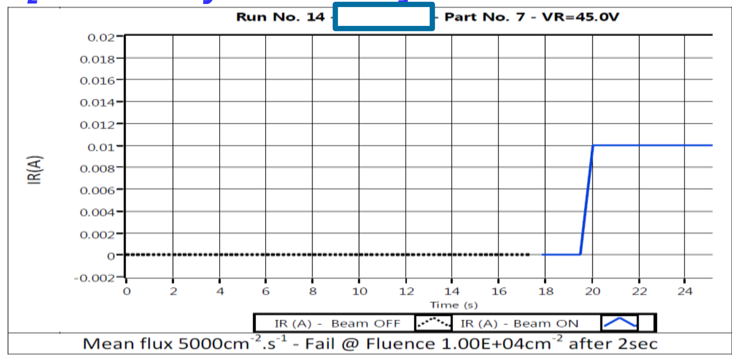
Power MOSFET

*[E. G. Stassinopoulos, 1992]*

# SEB damage in Schottky diodes

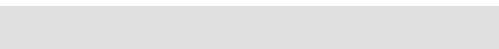
200V Schottky diodes
*[J. S. George, 2013]*

Also observed in low voltage Schottky diodes (35V – 45V)
*[M. O'Bryan 2012]*




$I_R$ at reverse Voltage of 45V
*[TRAD SEE test report 2015]*





# Single Event Gate Rupture SEGR

Gate

Gate oxide

Source

Ion Track

N+

P

N+

P+

(Body)

Neck

P+

Electron Current

Hole Current

N⁻ epilayer

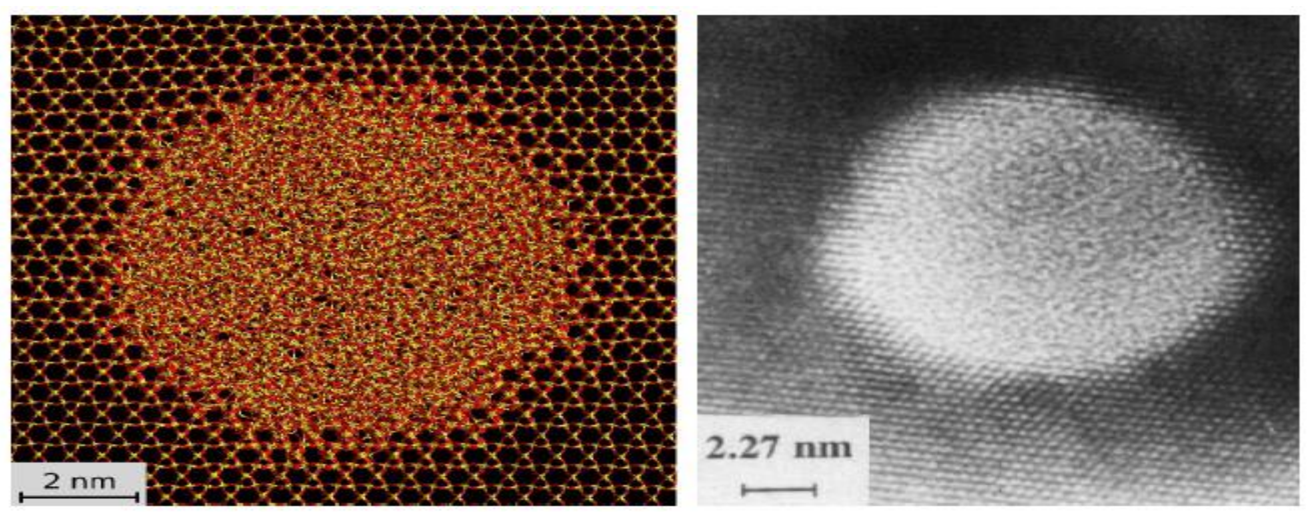
N+substrate

Drain

The charge deposited by the incident ion increases the electric field already present at he gate, exceeding the oxide breakdown field.

- Always destructive
- Decreases with angle of incidence
- Increases with electric field
- Power MOSFETs most susceptible
- MIM capacitor structures

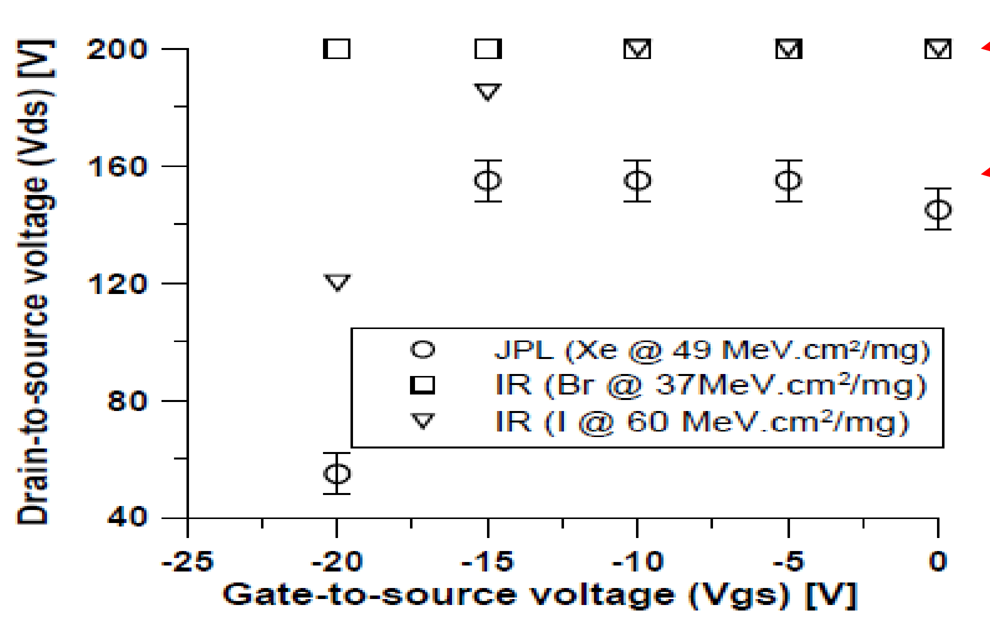
# SEGR damage




*[O.H. Pakarinen, NIM B 2009]* *[A. Mefteh, Phys. Rev. B, 1994]*

- The initial ion track damage is ≤ 10nm in diameter

# Safe Operation Area (SOA): issue of ion range (energy) used for testing




Manufacturer's data with short range ions

Data with long range ions

- IRHMB57260SE 200V NMOSFET.
- SEE were SEB and SEGR

*[L. Scheick, DW 2009]*
*[L. Scheick, JPL 2008 http://nepp.nasa.gov]*

# Single Event Dielectric Rupture (SEDR) in linear devices

Bromine Ion, 36.7 MeVcm²/mg

SEGR Cross Section [cm²]

$10^2$
$10^3$
$10^4$
$10^5$
$10^6$
$10^7$
$10^8$

C3 capacitor area = $1.2 \times 10^{-3}$ cm²

Absolute
operating limit

Lot Date Code 9736
Lot Date Code 9544

20
25
30

Supply Voltages [+/-V]

OP27 Low Noise Operational Amplifier.

*[G. Lum 2000, N. Boruta 2001]*

These events often occur at the output capacitor of linear operational amplifiers when supply and output voltage bias is close to the maximum limit.

# Single Event Effects - Summary

| | | |
|---|---|---|
| Single Event Upset (SEU) | corruption of the information stored in a memory element | Memories, latches in logic devices |
| Multiple Bit Upset (MBU) | several memory elements corrupted by a single strike | Memories, latches in logic devices |
| Single Event Functional Interrupt (SEFI) | corruption of a data path leading to loss of normal operation | Complex devices with built-in state machine/control sections |
| Single Hard Error (SHE) | unalterable change of state in a memory element | Memories, latches in logic devices |
| Single Event Transient (SET) | Impulse response of certain amplitude and duration | Analog and Mixed Signal circuits, Photonics |
| Single Event Disturb (SED) | Momentary corruption of the information stored in a bit | combinational logic, latches in logic devices |
| Single Event Latchup (SEL) | high-current conditions | CMOS, BiCMOS devices |
| Single Event Snapback (SESB) | high-current conditions | N-channel MOSFET, SOI devices |
| Single Event Burnout (SEB) | Destructive burnout due to high-current conditions | BJT, N-channel Power MOSFET |
| Single Event Gate Rupture (SEGR) | Rupture of gate dielectric due to high electrical field conditions | Power MOSFETs, Non-volatile NMOS structures, VLSIs, linear devices … |

***Non Exhaustive list, more in ECSS E-ST-10-12C***

# Complex devices may be sensitive to many different SEE types

Example: mixed signal ASICs, SEEs may propagate to other blocks / subsystems

Temperature Sensor

SET, SEB, SEGR, SEFI
Power Control /Regulator

SET, SEFI, SEDR
Voltage Regulator

SET
Frequency Generator /Timer

SET, SEDR

SET, SEDR

Analogue multiplexer
SET

Analogue filter /signal conditioning
SET

ADC
SEU
SEFI

SEU
SEFI
Converter control interface
SEU
SEFI

Micro Controller /DSP
SEU
SEFI

SRAM
SEU
SEFI
SHE

Flash
SEU
SEFI
SHE
SEGR?

SEU
SEFI
Peripheral interface

RF transceiver
SEB
SET

CAN/LIN bus interface
SEU
SEFI

Serial comms port
SEU
SEFI

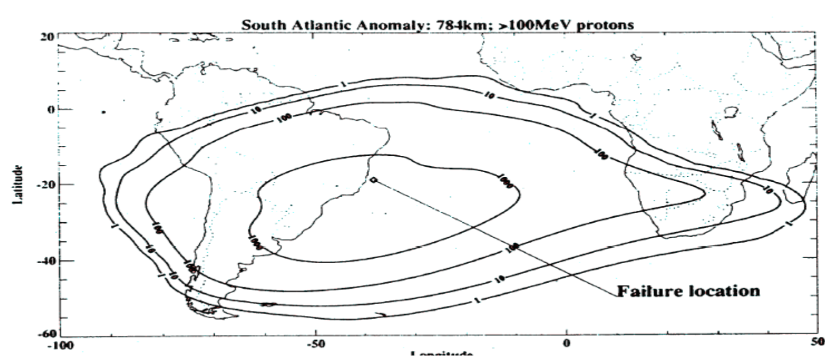
SET, SEDR
Analogue Driver

SET
Analogue filter /signal conditioning

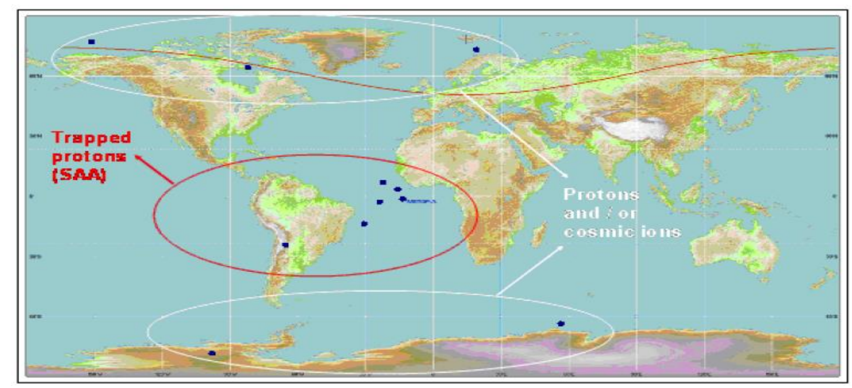
SET
SEFI
DAC

*SEL in CMOS technology* *[www.swindonsilicon.co.uk]*

# Examples of SEE anomalies




**PRARE on ERS-1**. A 64-kbit CMOS SRAM failed due to SEL. PRARE only lasted operational for 5 days




**IAISI on METOP**. About half the SEUs are located in the SAA. Those upsets may be related to the emerging issue of high-Z recoils within the radiation hardened device (HX6228 memory).

*[R. Ecoffet TNS 2012]*

**ISS**. SETs on optocoupler 6N134 are held responsible of unexpected reset on a reset circuit that was designed only to be used for ground testing.

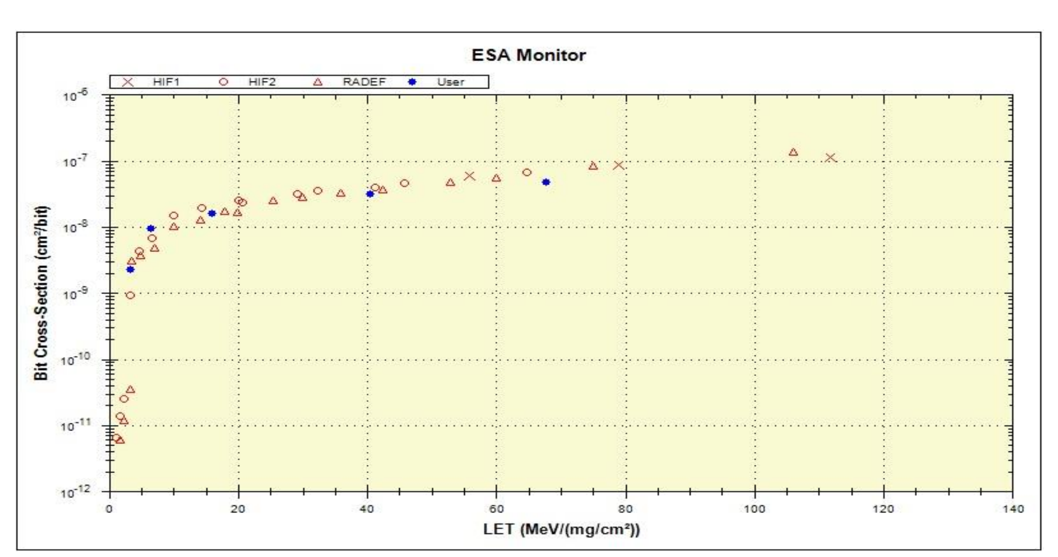
# Outline

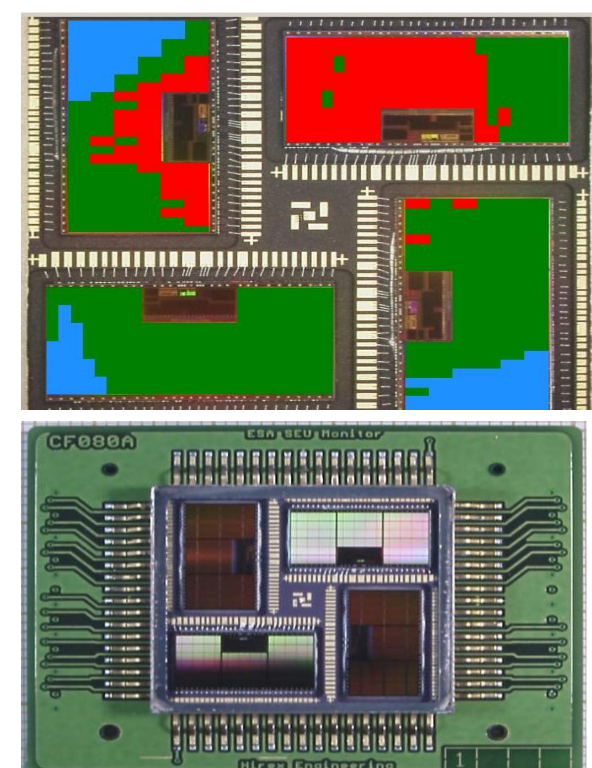
- SEE basic mechanisms
  - Beam: LET, range, energy
  - Counting events, cross-section

- Different types of SEEs
  - SEU, SET SEL SEB SEGR
  - New effects: MBUs, proton and electron direct ionization

- Practical aspects of SEE testing
  - Checking the beam
    - PIN diode, SEU monitor, RPUM
  - Statistics, Uncertainties, Error Bars
  - Lot-to-lot variations

# Checking the beam: the ESA SEU monitor



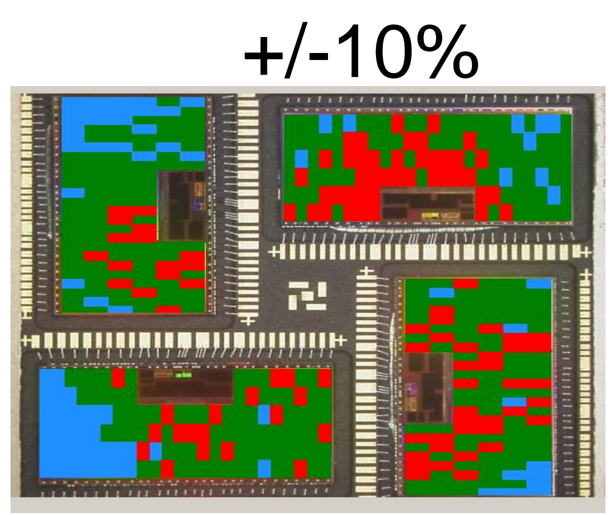

*[F-X Guerre, HIREX, 2013]*

4 dies module of the 0.25um ATMEL AT60142F 4Mbit SRAM

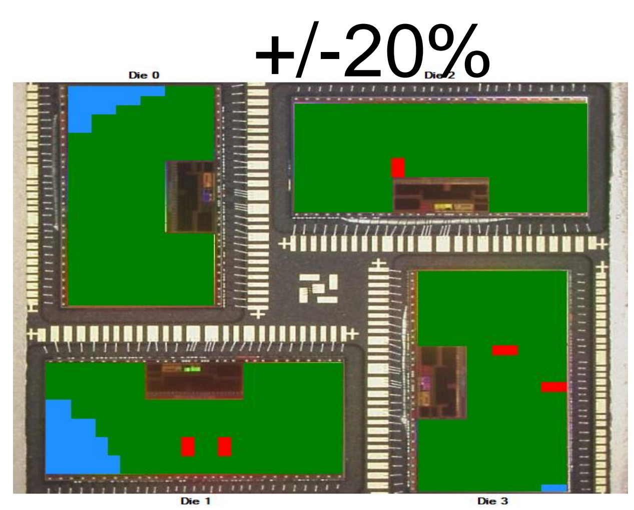
# Uniformity of beam flux

Kr, 305 MeV

+/-10%



+/-20%



# Checking the beam: the ESA calibrated PIN diode system

Relative distribution

$10^0$ $10^{-1}$ $10^{-2}$ $10^{-3}$ $10^{-4}$

N Ne Ar Fe Kr Xe

100 1000

Energy deposited in the PIN diode (MeV)

Charge collection

Measured Energy (MeV)

$y = 9.3126x$
$R^2 = 1$

Ion Atomic Mass Unit

9.3MeV/a
RADEF cocktail

# Statistics: counting events

Counting SEB events at GANIL (Xe)

LET [MeVcm²/mg]
27, 60

Number of events: 1, 10, 100

Fluence (cm⁻²): 10, 1000, 100000

run779
run780
run784
run785

*In this case*
*For a fluence of 1E5 particles/cm2*
*The number of SEB detected is proportional to fluence.*

*[Binois, Carvalho, 2013]*

# Fluence of events follows Poisson, i.e. Weibull function with a shape factor of 1

SEGR in power MOSFET and capacitors



Observed for both planar large area capacitors and power MOSFETs

This statistical behaviour is expected for **all single event effects**

*[V. Ferlet-Cavrois, TNS 2012]*

# Suggested Error Bar Recipe, in the new version of the ESCC25100 (Oct. 2014)

$$\sigma_{SEE} = \frac{N_{events}}{Fluence}$$

$$\frac{\delta\sigma_{SEE}}{\sigma_{SEE}} = \sqrt{\left(\frac{\delta N_{events}}{N_{events}}\right)^2 + \left(\frac{\delta Fluence}{Fluence}\right)^2}$$

$$\frac{\delta Fluence}{Fluence}$$

- Uncertainty on the facility dosimetry
  - 10% [ESCC25100 ]

$$\frac{\delta N_{events}}{N_{events}}$$

- Follows a Poisson distribution
- Advised 95% confidence level
  - "Real" value will be within measured N events plus or minus error bar for 95% of data.

The accuracy of the X-section depends on the fluence deposited and the number of events detected.

# Upper and Lower limits of Error Bars

10000
1000
100
10
1
0.1
0.01

$\sigma \times F$

0 1 10 100 1000

$N_{events}$

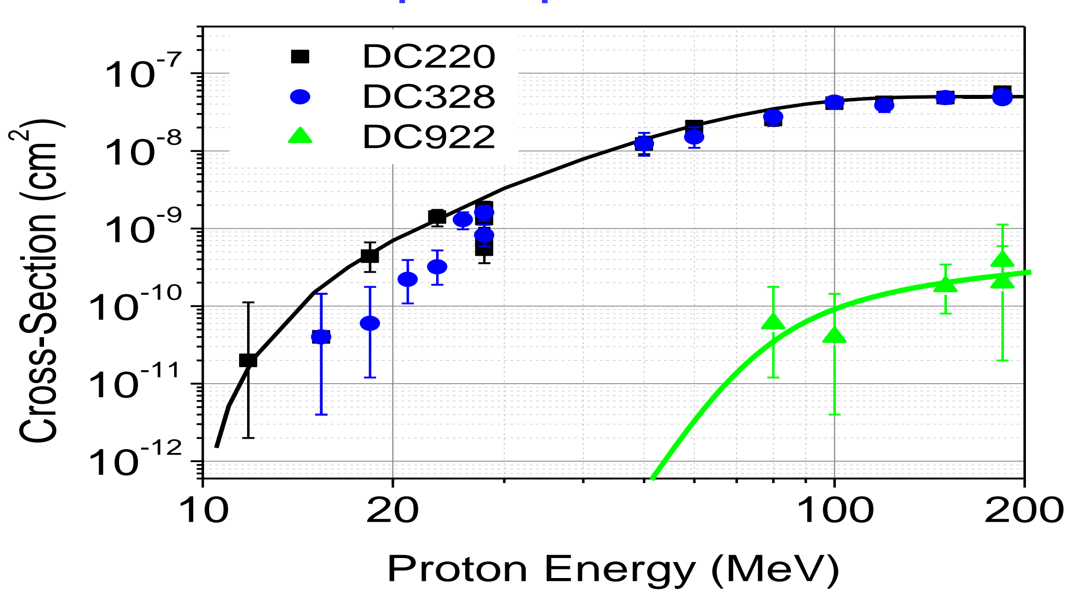
Confidence level

67% 90% 95%

*[ESCC 25100, Oct. 2014]*

# Test Example, use of Error Bars

## Same reference but different date codes: different latch-up response




256k x 16 SRAM
Samsung
K6R4016V1D

# Cumulated effects: TID + SEE

In some cases SEE sensitivity can vary with received TID.

SEL cross-section ($cm^2$)

$6x10^{-9}$
$5x10^{-9}$
$4x10^{-9}$
$3x10^{-9}$
$2x10^{-9}$
$1x10^{-9}$
0

DC220 #3
DC328 #1
DC328 #2

0 50 100 150 200

Total ionising dose TID (krad)

DC220 and DC328 were showing similar SEL response,

- Same process?

But their TID response is different

- Not really

# Same Example: with heavy ions

Manufacturer process changes also affect SEE sensitivity. Test the LOT that you want to fly. Always test your lot if you are using COTS.

## 256k x 16 SRAM Samsung K6R4016V1D

Cross Section (cm$^2$)

$10^{-1}$
$10^{-2}$
$10^{-3}$
$10^{-4}$
$10^{-5}$
$10^{-6}$
$10^{-7}$

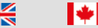
3 5 10 20 30 50 80

LET (MeV*cm$^2$/mg)

DC220
DC328
DC922
DC419 #81

ESA UNCLASSIFIED - For Official Use



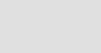


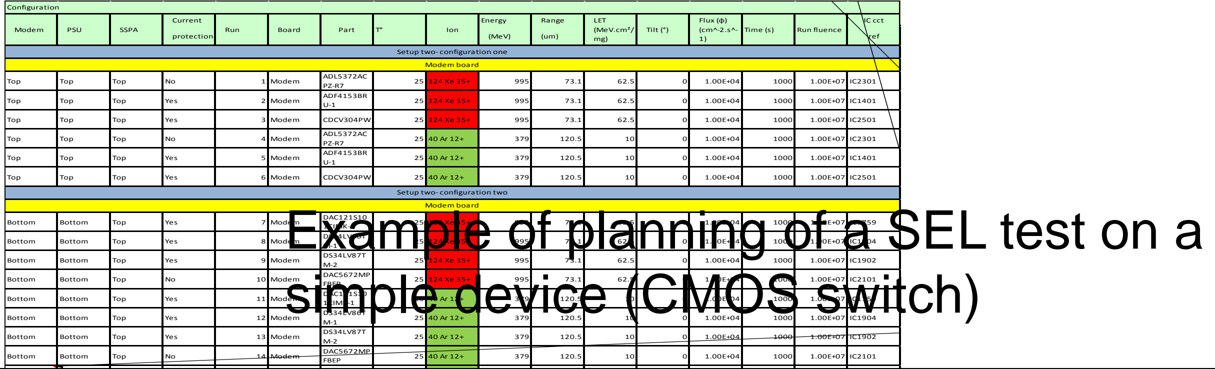
# SEE Test complexity (1)

- SEE tests can be very long and complex on devices like ASICs, FPGAs, μProcessors or new state of the art electronic devices, many different SEE types can appear at the same time.

- The presence of a radiation effects expert and a electronic design engineer is often required because real-time decision making is critical depending on test results. Repeating SEE test can be very costly in terms of planning and budget.

- SEE tests can be done at device level or at board / application level. The later are even more complex.





| Modem | PSU | SSPA | Current protection | Run | Board | Part | T° | Ion | Energy (MeV) | Range (um) | LET (MeV.cm²/mg) | Tilt (°) | Flux (ф) (cm^-2.s^-1) | Time (s) | Run fluence | IC cct ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Setup two- configuration one | | | | | | | | | | | | | | | | |
| Modem board | | | | | | | | | | | | | | | | |
| Top | Top | Top | No | 1 | Modem | ADL5372AC PZ-R7 | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC2301 |
| Top | Top | Top | Yes | 2 | Modem | ADF4153BR U-1 | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC1401 |
| Top | Top | Top | Yes | 3 | Modem | CDCV304PW | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC2501 |
| Top | Top | Top | No | 4 | Modem | ADL5372AC PZ-R7 | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC2301 |
| Top | Top | Top | Yes | 5 | Modem | ADF4153BR U-1 | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC1401 |
| Top | Top | Top | Yes | 6 | Modem | CDCV304PW | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC2501 |
| Setup two- configuration two | | | | | | | | | | | | | | | | |
| Modem board | | | | | | | | | | | | | | | | |
| Bottom | Bottom | Top | Yes | 7 | Modem | DAC121S10 [illegible] | 25 | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | 1000 | [illegible] | [illegible] |
| Bottom | Bottom | Top | Yes | 8 | Modem | [illegible] | 25 | [illegible] | 995 | [illegible] | [illegible] | 0 | [illegible] | 1000 | [illegible] | [illegible] |
| Bottom | Bottom | Top | Yes | 9 | Modem | DS34LV87T M-2 | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC1902 |
| Bottom | Bottom | Top | No | 10 | Modem | DAC5672MP FBEP | 25 | 124 Xe 35+ | 995 | 73.1 | [illegible] | [illegible] | [illegible] | [illegible] | 1.00E+07 | IC2101 |
| Bottom | Bottom | Top | Yes | 11 | Modem | [illegible] | 25 | [illegible] | [illegible] | 120.5 | [illegible] | [illegible] | [illegible] | 1000 | [illegible] | [illegible] |
| Bottom | Bottom | Top | Yes | 12 | Modem | DS34LV86T M-1 | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC1904 |
| Bottom | Bottom | Top | Yes | 13 | Modem | DS34LV87T M-2 | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC1902 |
| Bottom | Bottom | Top | No | 14 | Modem | DAC5672MP FBEP | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC2101 |

# Example of planning of a SEL test on a simple device (CMOS switch)

| Time | Run | DUT | Ion | Pentration | Energy MeV | LET | Angle (deg) | LETeff | TID (krad) | Vbias1 | Isb1 | Vbias2 | Isb2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11 | part #1 position A (Temp 72C) | Xe | 73um | 995 | 62.5 | 0 | 62.5 | 10.00 | 15V | not meas | - 15V | not meas |
| 16:05 | 12 | part #2 position B (Temp 81C) | Xe | 73um | 995 | 62.5 | 0 | 62.5 | 10.00 | 15V | not meas | - 15V | not meas |
| | | | | | | | | | | | | | |
| | | | | | | | | | | | | | |
| 16:50 | 13 | part #3 position A (63.5temp C) | Xe | 73um | 995 | 62.5 | 0 | 62.5 | 10.00 | 15V | not meas | - 15V | not meas |
| 17:05 | 14 | part #4 position B (81 temp C) | Xe | 73um | 995 | 62.5 | 0 | 62.5 | 10.00 | 15V | not meas | - 15V | not meas |

| Modem | PSU | SSPA | Current protection | Run | Board | Part | T° | Ion | Energy (MeV) | Range (um) | LET (MeV.cm²/mg) | Tilt (°) | Flux (ф) (cm^-2.s^-1) | Time (s) | Run fluence | IC cct ref |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bottom | Bottom | Top | No | 30 | PSU | TPS5420MD REP | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC5001 |
| Setup one- configuration one | | | | | | | | | | | | | | | | |
| SSPA board (To be performed at the end of the test) | | | | | | | | | | | | | | | | |
| Bottom | Bottom | Top | No | 31 | SSPA | CGH40025F | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | |
| Bottom | Bottom | Top | No | 32 | SSPA | CGH40025F | 25 | 84 Kr 25+ | 769 | 94.2 | 32.4 | TBD | 1.00E+04 | 1000 | 1.00E+07 | |
| Top | Top | Top | No | 33 | PSU | DVSA2812S/ H-G | 25 | 84 Kr 25+ | 769 | 94.2 | 32.4 | TBD | 1.00E+04 | 1000 | 1.00E+07 | IC4012 |
| Top | Top | Top | No | 34 | PSU | DVHF2818SF /H-G | 25 | 84 Kr 25+ | 769 | 94.2 | 32.4 | TBD | 1.00E+04 | 1000 | 1.00E+07 | IC4010 |
| Top | Top | Top | No | 35 | PSU | DVSA2812S/ H-G | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC4012 |
| Top | Top | Top | No | 36 | PSU | DVHF2818SF /H-G | 25 | 40 Ar 12+ | 379 | 120.5 | 10 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC4010 |
| Top | Top | Top | No | 37 | PSU | DVSA2812S/ H-G | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC4012 |
| Top | Top | Top | No | 38 | PSU | DVHF2818SF /H-G | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC4010 |
| Bottom | Bottom | Top | No | 39 | SSPA | CGH40025F | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | |
| Setup one- configuration two | | | | | | | | | | | | | | | | |
| PSU board | | | | | | | | | | | | | | | | |
| Bottom | Bottom | Top | No | 40 | PSU | TPS5410MD REP | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC8001 |
| Bottom | Bottom | Top | No | 41 | PSU | TPS5410MD REP | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC9001 |
| Bottom | Bottom | Top | No | 42 | PSU | TPS5420MD REP | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC1001 |
| Bottom | Bottom | Top | No | 43 | PSU | TPS5420MD REP | 25 | 124 Xe 35+ | 995 | 73.1 | 62.5 | 0 | 1.00E+04 | 1000 | 1.00E+07 | IC5001 |

example

# Conclusion

- Large variety of single event effects
- SEE are linked to the DUT technology
  - New SEEs arise in new technologies.
  - Highly scaled techs have higher SEE sensitivity
  - SEE tests can be very complex
  - Real-time decision making is a must.
- COTS issue
  - Test of the flight lot is mandatory
  - Secure procurement for an homogeneous lot
- For experimenters
  - Check your beam
  - Use error bars
- Ask a radiation effects expert in case of doubt