- TID Total Ionizing Dose

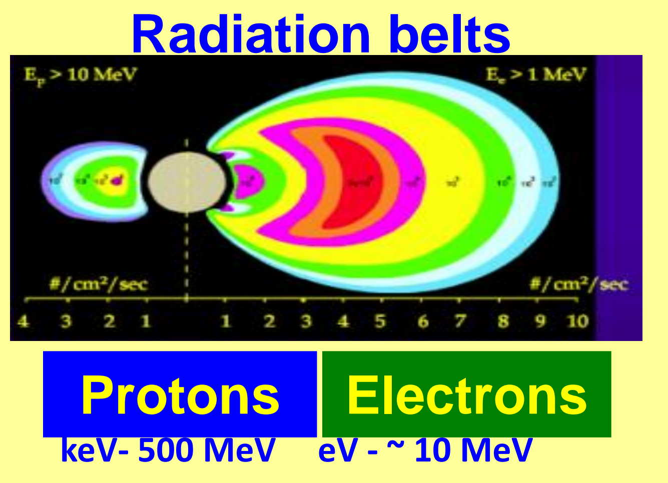
Radiation Environment and its Effects in EEE Components and Hardness Assurance for Space Applications

Presenter: Marc Poizat

ESA UNCLASSIFIED - For Official Use

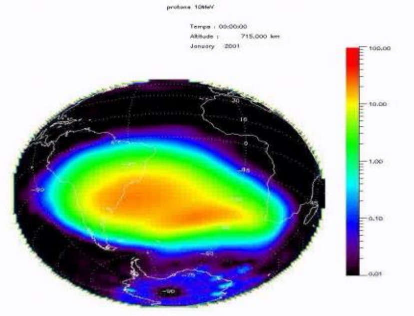
Space environment radiation sources

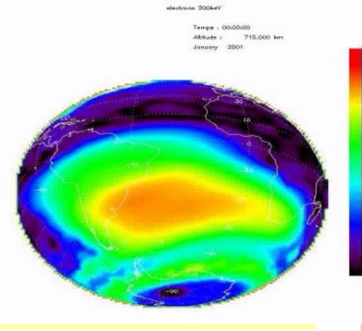
Radiation belts



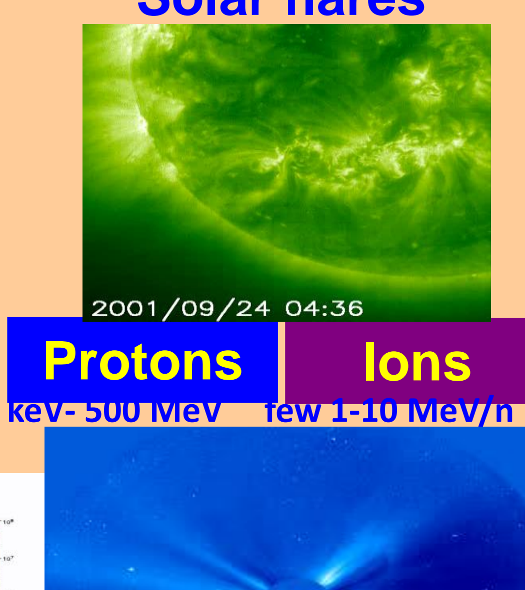
Protons keV- 500 MeV

Electrons eV - ~ 10 MeV





Solar flares

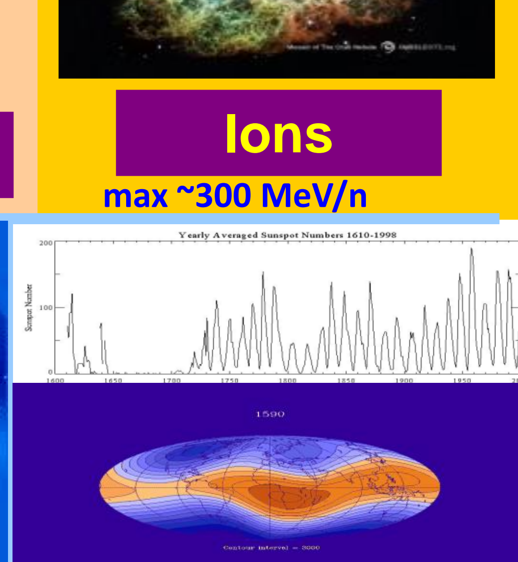


Protons keV- 500 MeV

Ions few 1-10 MeV/n

Cosmic rays

Ions max ~300 MeV/n



After Ecoffet & Gerardin, RADECS 2015

Main radiation effects in EEE components

Electrons

Protons

Heavier ions

p+
(e-)
Oxide
Interstitials
Silicon
Vacancies

Displacement Damage

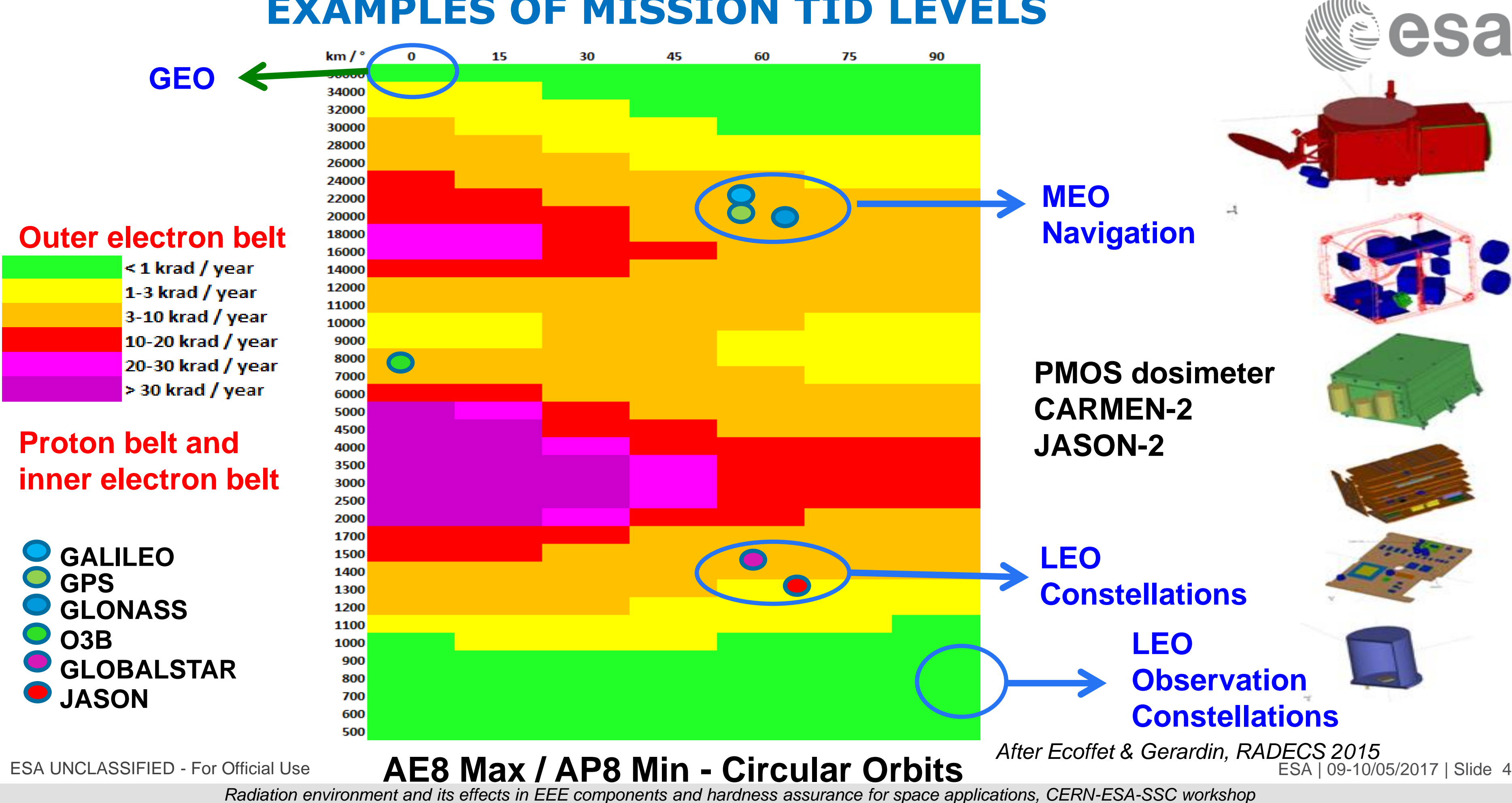
e-
p+
Trapped charges
Oxide
Interface traps
Silicon

Total Ionising Dose

Ion
p+
Oxide
Silicon
Ionisatio
n
Ion 2nd

Single Event Effects

EXAMPLES OF MISSION TID LEVELS



Radiation Units

TID: Deposited energy 1 Gray = 1 J/kg (International System Unit)

- Commonly used unit : **rad** (**R**adiation **A**bsorbed **D**ose)

1 Gy = 100 rad

~0.1% ΔE

$$\Delta E = \Delta E_{ionization} + \Delta E_{displacement}$$

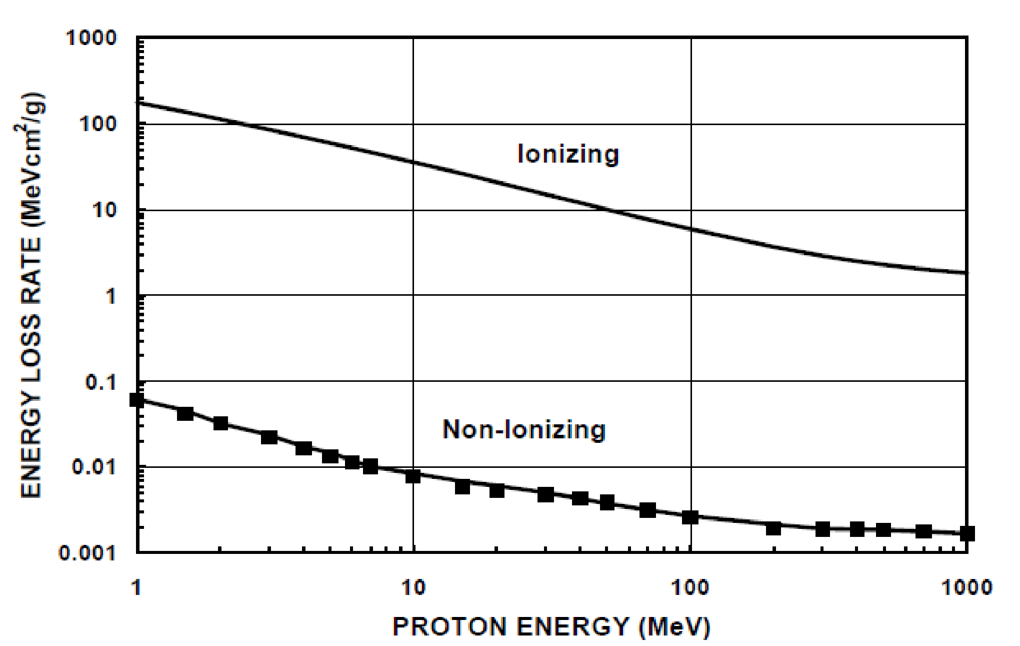
Energy to create one electron-hole pair:

- In SiO_2: ~17 eV => ~7.8 10^{12} e-/h pair per rad.cm^3
- In Si: 3.6 eV => 4 10^{13} e-/h pair per rad.cm^3

DD: Energy to create displacement damage

- In Si: 21 eV

Ionizing and Non-Ionizing Energy Loss

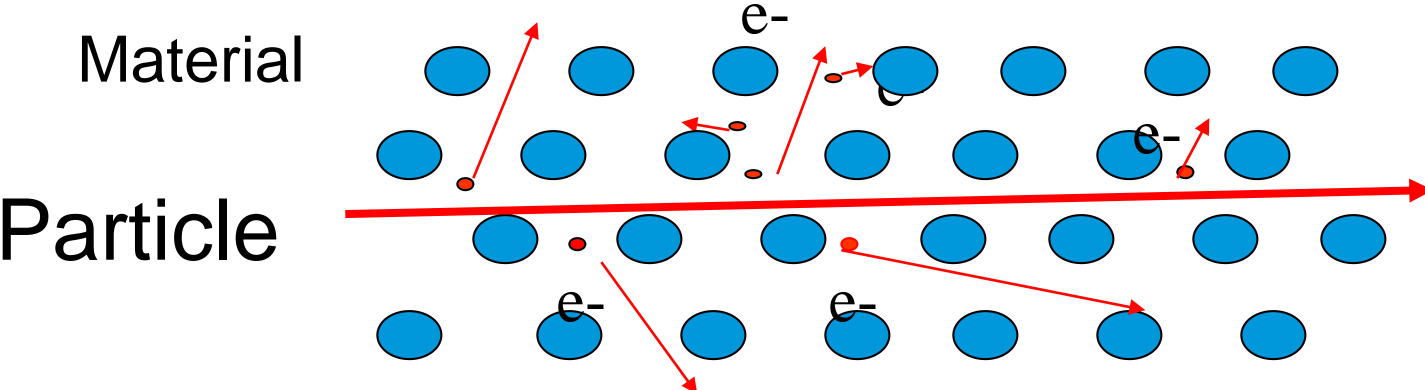


Ionizing Energy Loss (IEL)

NIEL: energy that goes into displacements, about 0.1% of total energy

[C. Marshall, Short-course notes, NSREC 1999]

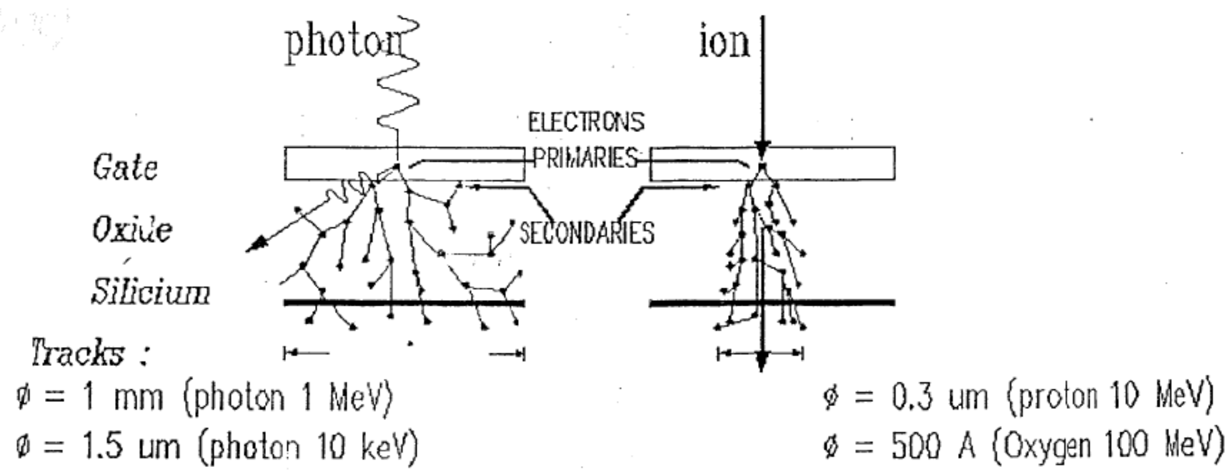
Ionization



- Creation of electron-hole pairs after thermalization of high-energy electrons (delta-rays)
- If Energy of generated electrons and holes > minimal energy required for electron-hole pair creation then they can themselves generate supplementary pairs
- TID has a significant effect in insulators (SiO_2, NO, HfO_2…)

Energy deposited by photons or ions: uniformed or localized

- Ionising particles in space generate secondary electrons
- Generated electrons themselves are very energetic wrt energies of valence electrons and even core electrons of atoms



[J.L. Leray, NSREC short-course 1999]

Fraction of un-recombined holes (yield) decreases at low electric fields

Fraction of Unrecombined Holes

1.0
0.8
0.6
0.4
0.2
0.0

Co-60
10-keV x-ray
700-keV protons
2-MeV α particles

0 1 2 3 4 5

Electric Field (MV/cm)

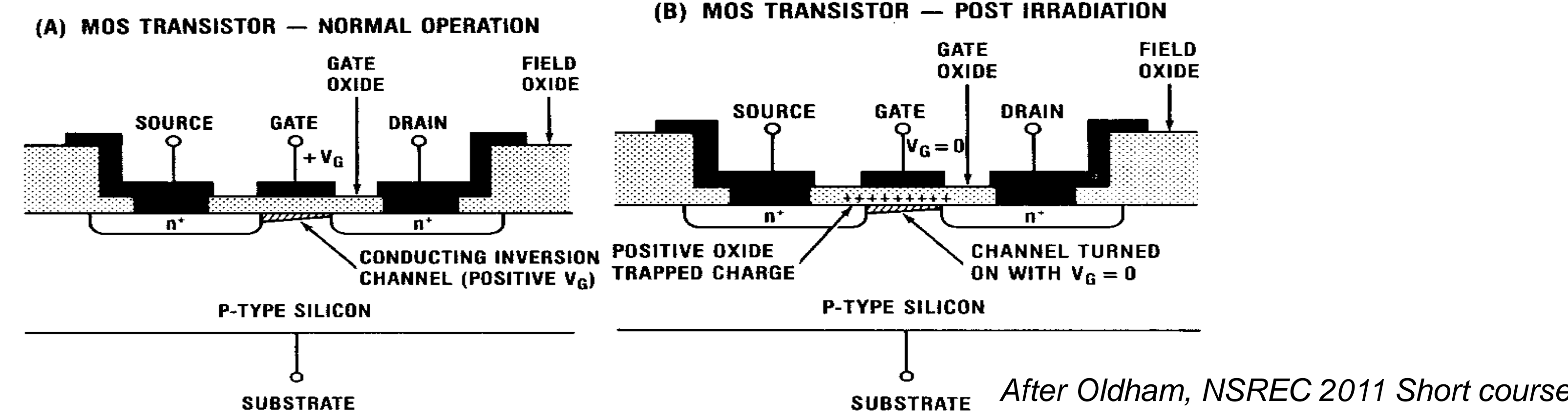
After F. B. McLean and T. R. Oldham, HDL Technical Report, No. HDL-TR-2129 (1987) and M. R. Shaneyfelt, et al., (1991)

Before radiation-generated electrons leave the oxide some fraction will recombine with holes

Fraction of unrecombined holes depends on ***oxide electric field, type*** and ***energy*** of incident particle

TOTAL DOSE EFFECTS IN MOS TECHNOLOGY

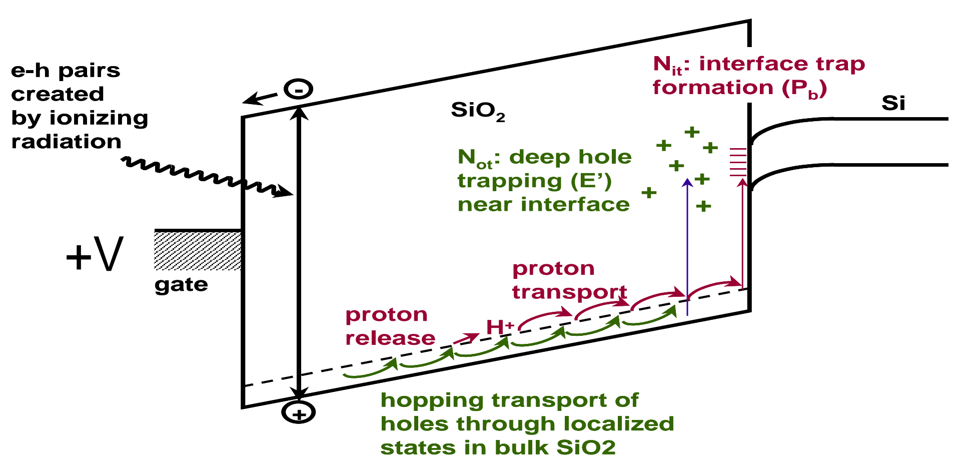
Radiation induced charging of gate oxide in N-Channel MOSFET



After Oldham, NSREC 2011 Short course

- (A) Applying adequate Vg on gate creates conducting channel between Source and Drain: the device is ON
- (B) Due to ionizing radiation, charges trapped in gate oxide cause shift in Vthreshold necessary to turn device ON. If shift significant enough then transistor cannot be turned OFF even at Vg = 0V -> failed transistor (depletion mode).

Ionizing Radiation induced charge trapping and interface state generation in MOS Structure



[McLean & Oldham, 2003]

With the application of a positive gate bias, holes transport to the Si/Si02 interface.
Close to the interface there are a large number of oxide vacancies due to the out-diffusion of oxygen in the oxide and lattice mismatch at the surface. These oxide vacancies can act as trapping centers. As holes approach the interface, some fraction of the holes will become trapped.

1. Generation of e/h pairs (17eV/pair in SiO2) by incoming ionising particles, followed by,
2. Prompt recombination (depends on radiation source and electrical field)
3. Transport of free carrier remaining in the oxide with application of positive gate bias to the Si/SiO2 interface. Close to the interface, large number of oxide vacancies due to out-diffusion of oxygen in the oxide and lattice mismatch
4. Formation of trapped charge via hole trapping in defect precursor sites OR formation of interface traps via reaction with hydrogen in SiO2

➔ All this results in an induced electric field added to the applied existing one in the functioning component which affects the electrical parameters.

➔ Thick oxides are particularly sensitive to TID.

Threshold-voltage shifts in MOS transistors: contribution of oxide traps and interface traps

Drain current

PMOS

NMOS

Vit

Vot

Vot

Vit

Gate voltage

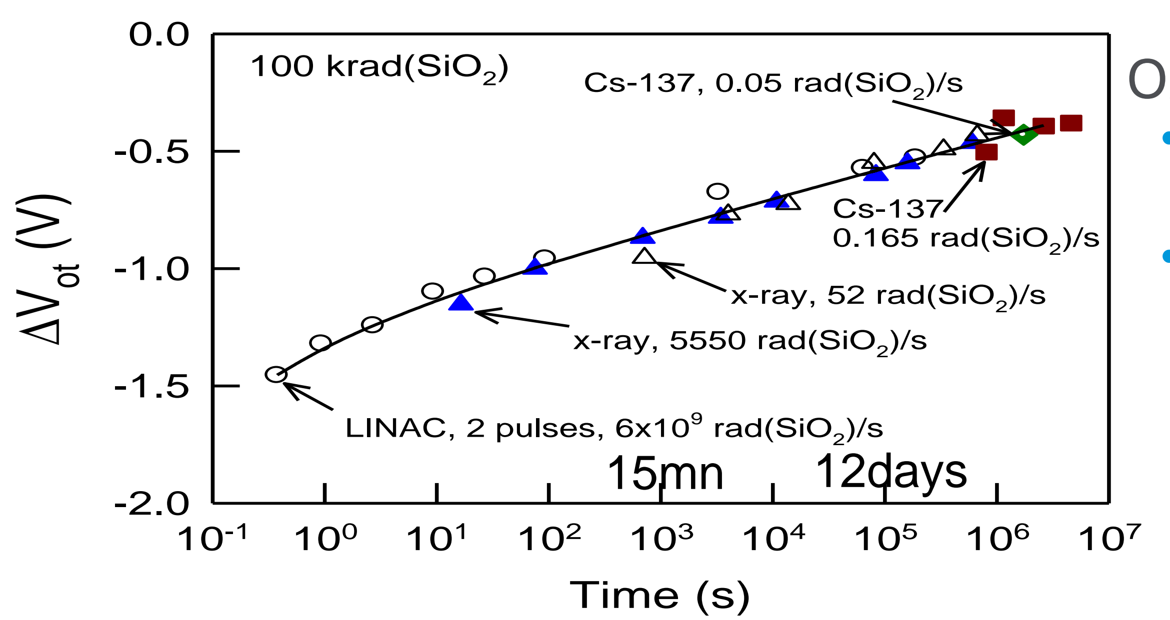
$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}$$

ΔV_{ot} leads to increases in supply leakage current

ΔV_{it} leads to degradation in timing parameters

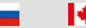
- For both p and n-channel transistors: trapped holes (+) in *oxide traps* induce negative Vth shift
- For p-channel transistors: interface traps are mostly + causing – Vt shifts
- For n-channel transistors: interface traps are mostly – causing + Vt shifts

Buildup of Oxide-Trapped Charge is Maximum Shortly after Irradiation



After D. M. Fleetwood, et al., IEEE Trans. Nucl. Sci. 35, 1497 (1988)

Oxide-trapped charge:
- Can neutralize in time after irradiation
- Neutralization follows a transient annealing curve which is independent of dose rate



Interface-Trap Buildup Can Take Thousands Of Seconds To Saturate

After M. R. Shaneyfelt, et al., IEEE Trans. Nucl. Sci. 39, 2244 (1992)

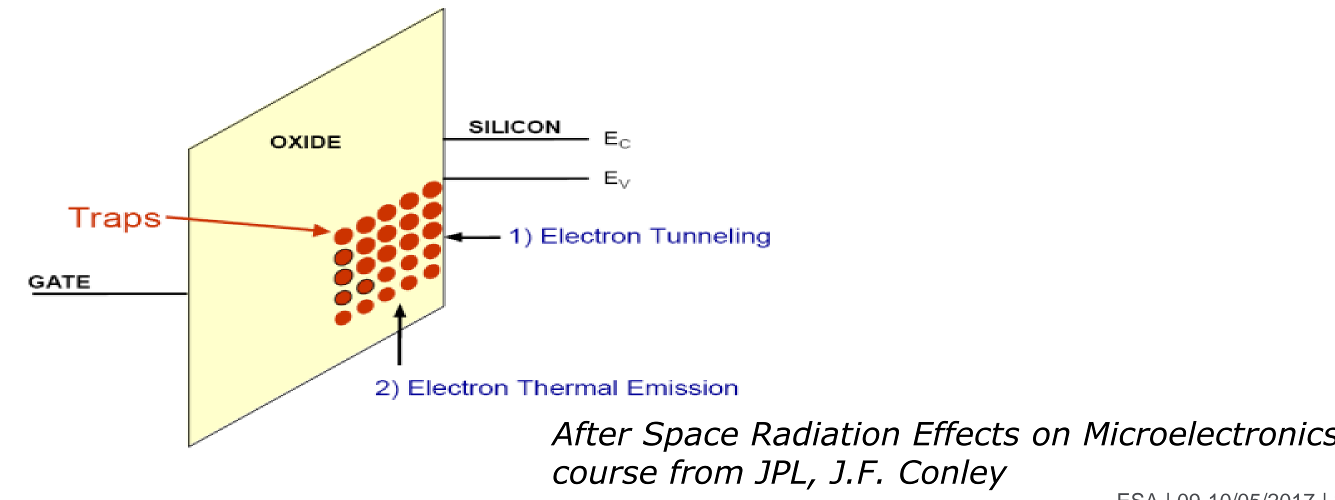
Interface traps:

- Do not normally anneal at room temperature
- Reduce carrier mobility
- Interface-Trap buildup follows a single response curve independent of the dose-rate of the radiation source

Annealing of the oxide trapped charge

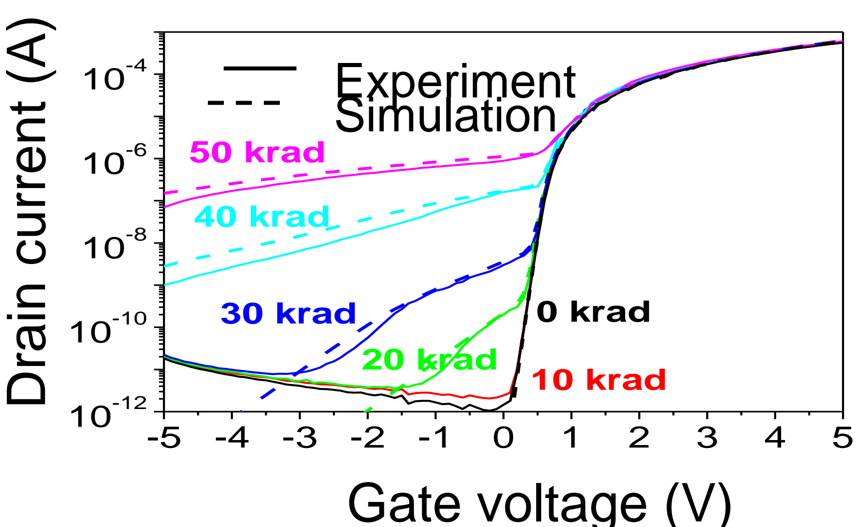
Tunnel annealing of electrons from Si to oxide traps (spatial and logtime dependence)

Thermal annealing by emission of electrons from oxide valence band into oxide traps (energy and temperature dependence)

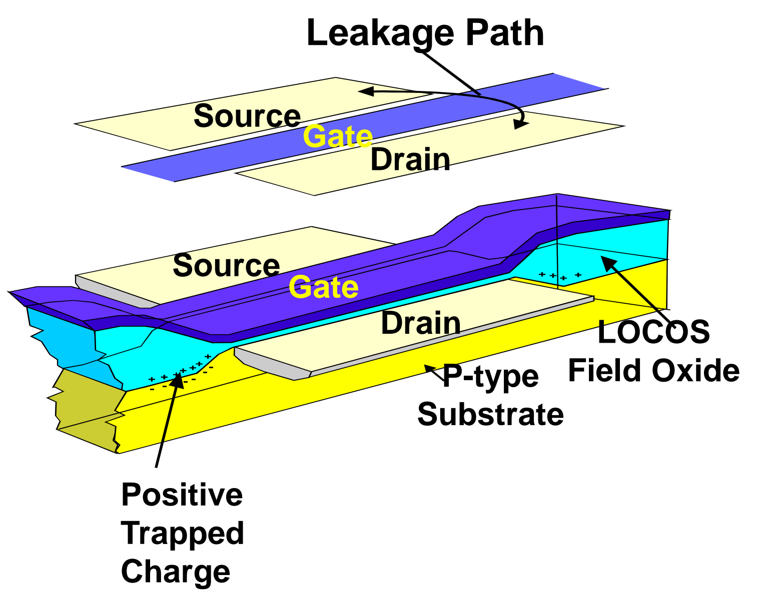


After Space Radiation Effects on Microelectronics course from JPL, J.F. Conley

Charge buildup in field oxides cause large increase of the lateral transistor leakage current



Ferlet HDR05



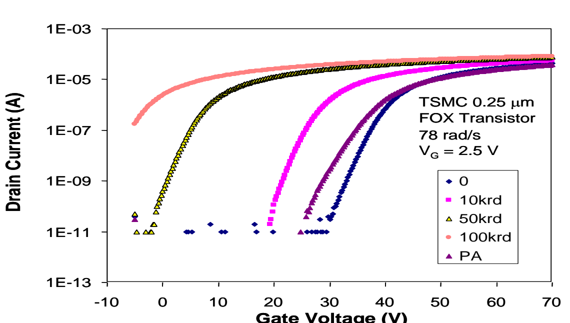
- Charge trapped in the isolation acts as lateral parasitic transistor
- Field oxide leakage current limits radiation hardness of most commercial ICs

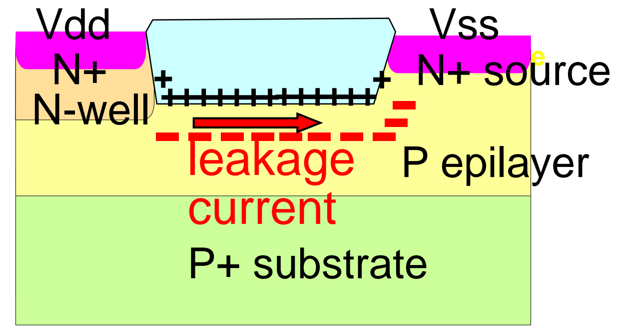
Technology hardening

Technology hardening is possible for example by doping under the field oxide but such trade-off is often at the expense of electrical performances

Technology hardening

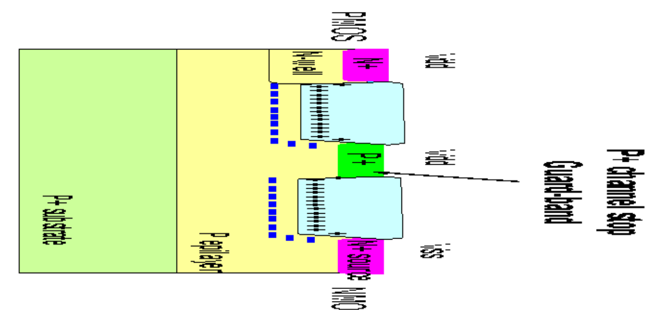
Another source of radiation-induced leakage current is the parasitic "inter-device" transistor





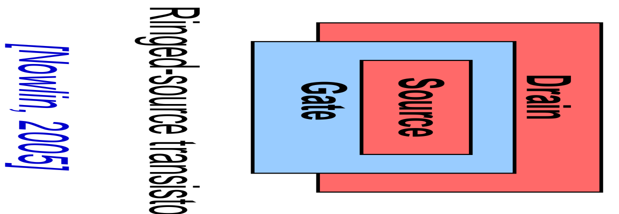
[R. C. Lacoe, et. al. TNS Dec. 2000]

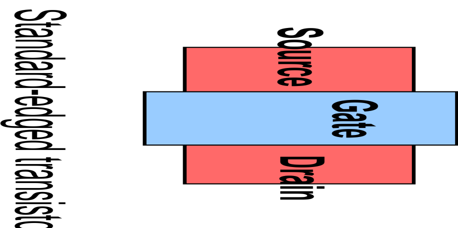
Inter-device leakage can be mitigated with p+ guard ring but at the expense of area

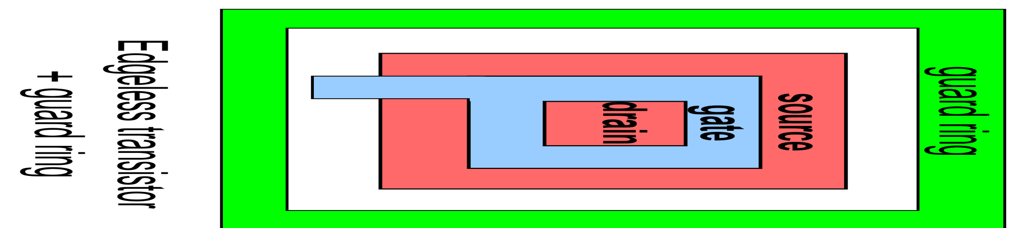


TID Hardening by design techniques (1)

Hardness by design methodology: examples of techniques for designing TID-hardened ICs

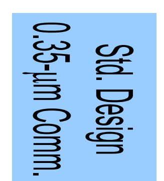


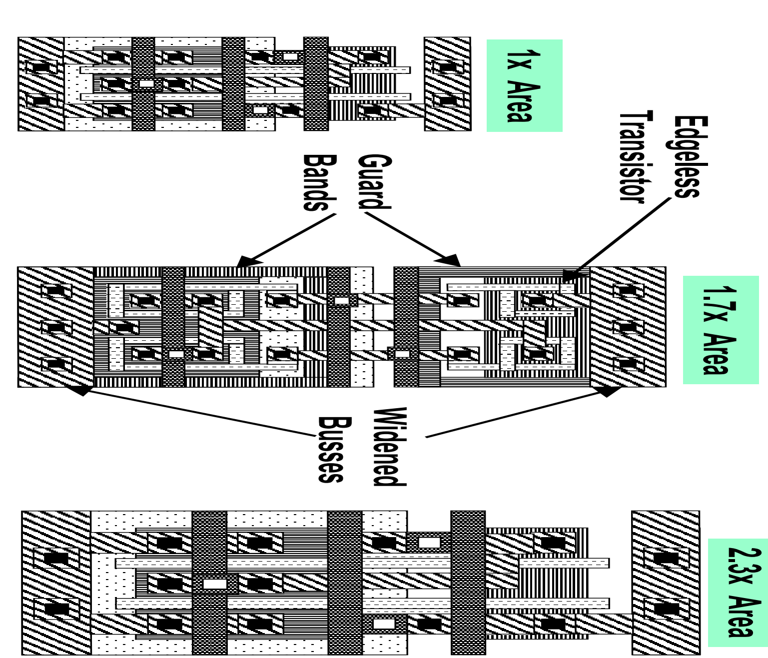




TID Hardening by design techniques (2)

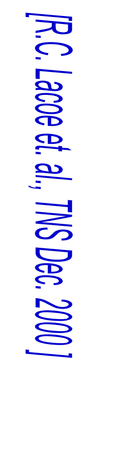
Area Comparison –
2NAND Logic Gate





Rad-Hard-By-Design
0.35-µm Comm.

Std. Design
0.50-µm 1 Gen
Behind

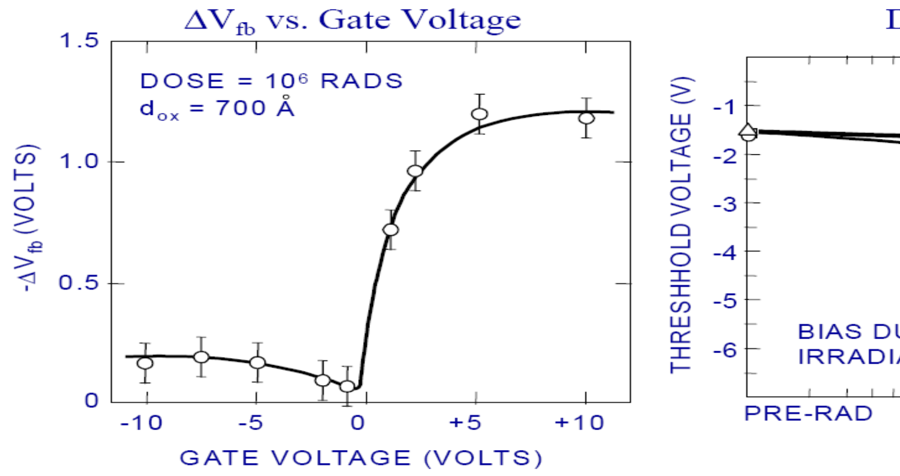


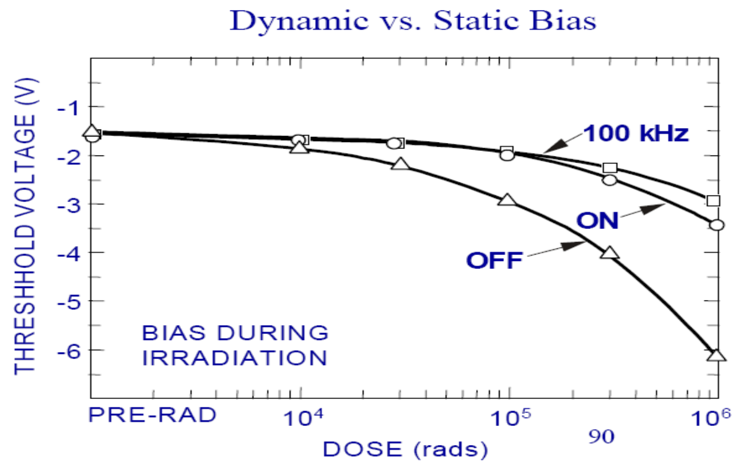
Effects of bias in MOS structures

Bias has a strong influence on the radiation response

Powering down a device can sometimes improve radiation response

Powered device is not always worst case





After Space Radiation Effects on Microelectronics course from JPL, J.F. Conley

Rebound effect

Irradiation
Anneal
Voltage Shift (V)
Time (h)
ΔV_{it}
ΔV_{th}
ΔV_{ot}
T = 25°C
4
2
0
-2
-4
0.01
0.1
1
10
100
1000

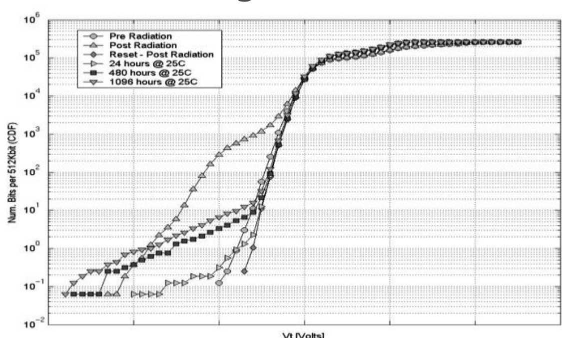
ICs that pass after irradiation may fail after a "rebound" anneal due to annealing of oxide-trap charge.

It is recommended not to use devices subject to "rebound" effects.

After J. R. Schwank, et al., IEEE Trans. Nucl. Sci. NS-31, 1453 (1984)

Micro-Dose Effects

- Microdose effects are caused by a single heavy ion
- First observed on SRAMs:
  - Charges deposited by incoming ion can cause Vt shift
  - Vt shift can result in leakage current > max current that can flow through drain junctions -> if so, a bit can be stuck
- Stuck bits can also be caused by gate rupture
- Lattice structure of insulators can be affected by single ion resulting in latent defects -> small leakage currents Soft Breakdown (SBD).



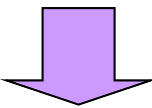
- SBDs reveal stuck bits after life tests
- SBDs affects e.g. floating gate NAND Flash resulting in increased retention failures (figure left following irradiation with Xe ion, LET=54MeV.cm^2/mg)

Oldham et. al., IEEE TNS, vol.52, no6, pp2366-72, (2005)

TOTAL DOSE EFFECTS IN BIPOLAR TECHNOLOGY

Effects in Bipolar devices (1)

The passivation oxide layer (protection) is thicker than in CMOS

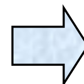


Process similar to MOS devices: Charge trapping + Interface States

$\beta = I_C / I_B$

Main effects

- Increase of I_B
- Gain degradation (β or h_{FE})
- Leakage

Lower-quality oxide  Greater Damage

-V_{BC} + V_{BE} -

Emitter n^+

Base p^- e^-

Collector n^-

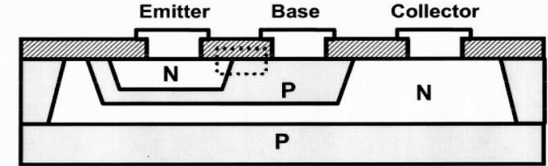
C

B

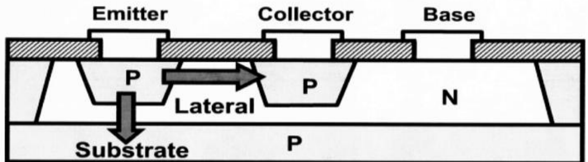
E

Effects in Bipolar devices (2)

- Charges trapped in base oxide partially invert the base leading to increased collector current (even when base unbiased)
- When base turned on, collector current increases less than expected therefore gain is reduced
- Mechanism similar for vertical NPN and lateral PNP but lateral PNP much more TID sensitive



Vertical NPN: trapped charge in base oxide causes reduced gain

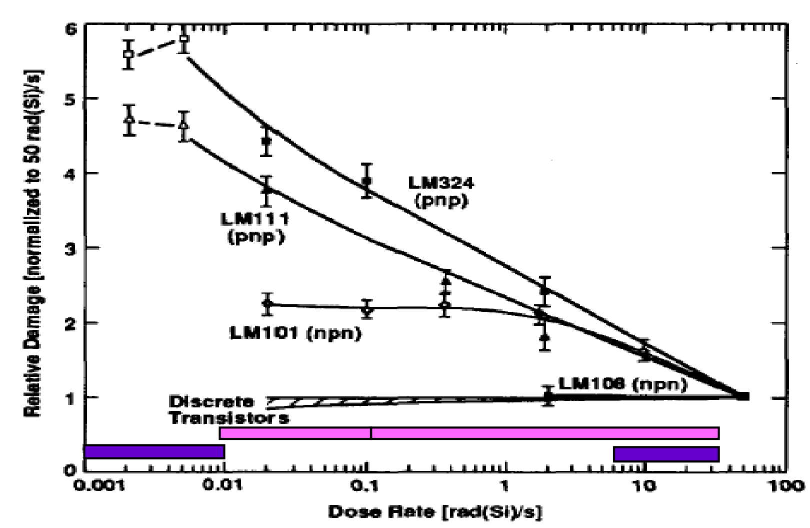


Lateral PNP: current base conduction along the surface under base oxide leading to greater effect because closer to oxide defects

After Schmidt et. al. IEEE TNS, NS-42,1541

Enhanced Low Dose Rate Sensitivity (ELDRS) – (1)

- ELDRS is complex phenomenon, depends on manufacturing process and technology
- Numerous models in the literature attempting to explain ELDRS:
  - could be due to charge build-up in space oxide above E-B junction
  - most models based on fact that main difference btw high and low dose rate caused by lower mobility of protons than holes, also indicating dependency on applied electric field
- Discrete transistors hardly affected by ELDRS
- PNP generally more ELDRS sensitive due to thicker oxide. Lateral PNP suffer higher degradation due to high current flowing near Si/SiO2 interface.



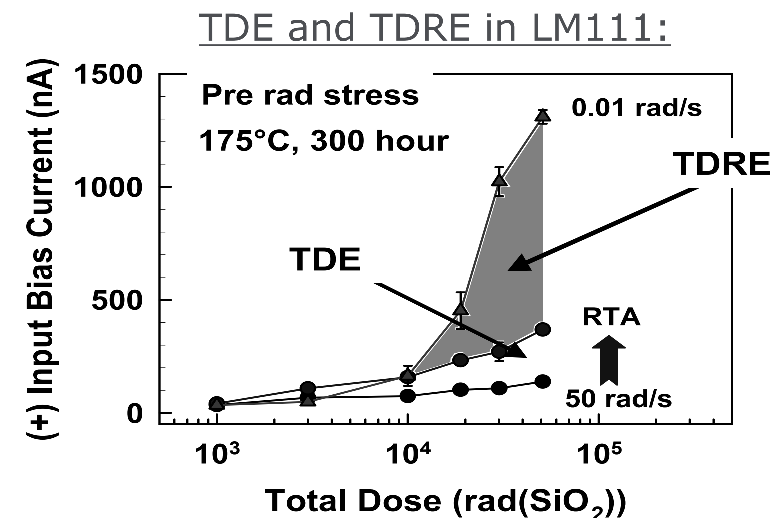
ESCC 22900
MIL-STD 883 1019.8

[Johnston 1994]

Enhanced Low Dose Rate Sensitivity (ELDRS) - 2

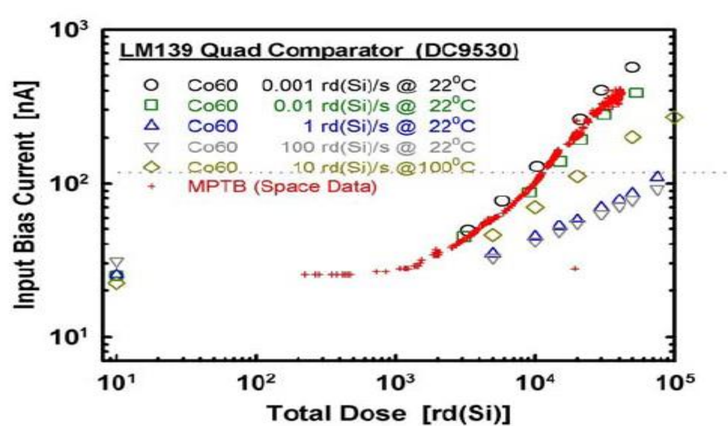
- ELDRS is a true dose rate effect (TDRE), not time dependent effect (TDE) as sometimes observed in CMOS devices.
- True dose rate effect: "A true dose rate effect is observed if, for a given total dose exposure, the degradation after irradiation at low dose rate is different than the degradation at a higher dose rate followed by a room temperature anneal period at least equivalent to the low dose rate exposure time." (ESCC22900)

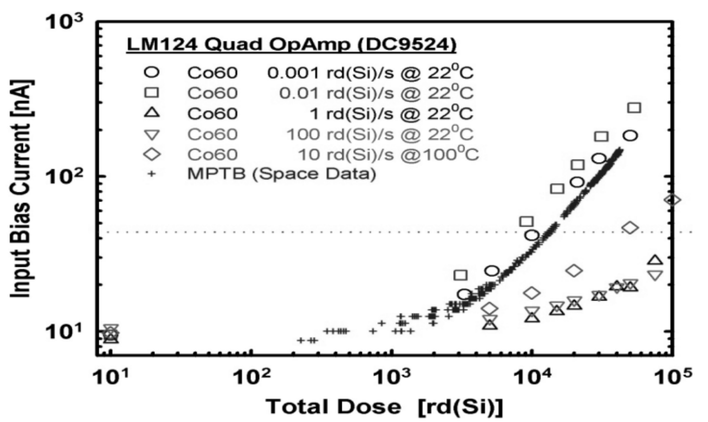
TDE and TDRE in LM111:



[Shaneyfelt et. al., IEEE TNS NS47, no6, 2539-45, Dec. 2000)]

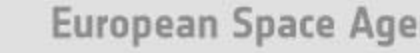
ELDRS in space





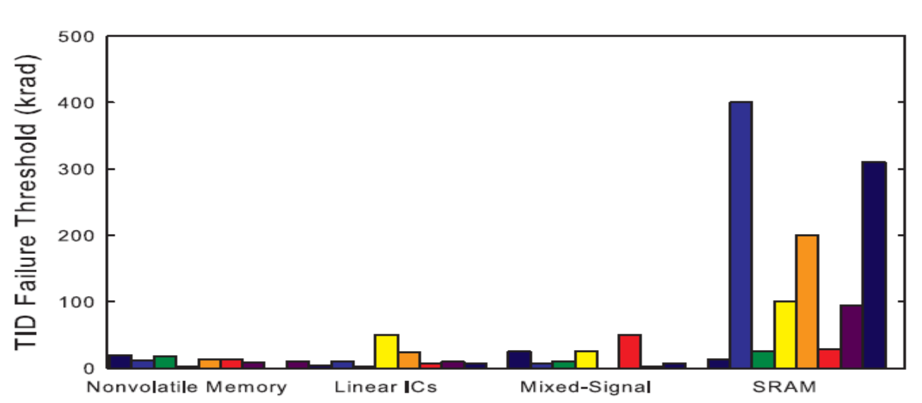
[J.L. Titus, 1999]

Input bias current vs total dose for NSC LM139 and LM124 in a space experiment and for various ground tests at different dose rates. This data is still valid!



Examples of TID effects on EEE components

Wide range in TID response



Compilation from Radiation Effect data workshops between 2002 and 2004

[P. E. Dodd, RADECS Short-course 2009]

- Real systems use variety of IC technology generations for which TID hardness is not guaranteed.
- Radiation response of parts in a system vary over a wide range
- Overall system response limited by its weakest component
- No generic behaviour per circuit family or technology node
- No scaling rule from one generation to the next
- Testing is required to assess TID hardness
- In-flight TID related anomalies are rare (Hipparcos but operated in geo transfer orbit instead of geo)

Example of TID induced degradation in a power MOSFET

^{60}Co gamma rays
FDD068AN03L
V_{gs} = 15V

Increasing Dose

I_{ds} (A)

10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}

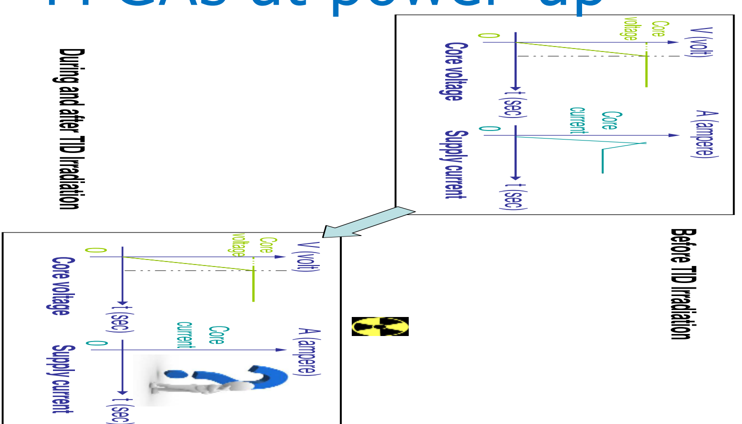
-3 -2 -1 0 1 2

V_{gs} (V)

pre
1 krad
2 krad
5 krad
10 krad
20 krad
50 krad

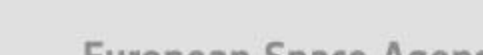
[Shaneyfelt et. al., TNS 2008]

Potential TID induced increase in rush current in FPGAs at power-up



Final presentation by TRAD (B. Vandevelde), ESA contract #4000102704/10/NL/EM

- Increase in surge currents at power-up of FPGAs with increasing TID levels have been observed (Actel and Xilinx) in some studies
- ESA activity on 4 FPGA types (Microsemi RTAX1000S, Xilinx XC4VFX40, ATMEL AT40 and ATF280F) with various startup profiles (fast and slow voltage ramps) showed no significant differences in power-up currents with increasing TID levels
- Nevertheless, such investigations are recommended when performing TID evaluation/qualification tests on FPGAs



TID in Flash memories (1)

Single-Level-Cell Flash memories: 16Gbit Micron MT29F16G08ABABA 34nm technology node. TID tolerance ~65krad.

SLC: Retention Errors

REtention Errors [bytes]
1.0E+07
9.0E+06
8.0E+06
7.0E+06
6.0E+06
5.0E+06
4.0E+06
3.0E+06
2.0E+06
1.0E+06
0.0E+00
0
20
40
60
80
100
Dose [krad]
MF42 low duty cycle
MF36 high duty cycle
MF37 high duty cycle
MF40 high duty cycle
MF39 low duty cycle
MF1 ref high duty cycle

SLC: Block Erase Fails

Errors [blocks]
300
250
200
150
100
50
0
0
20
40
60
80
100
Dose [krad]
MF42 low duty cycle
MF36 high duty cycle
MF37 high duty cycle
MF40 high duty cycle
MF39 low duty cycle

ESA Contract 2011-2012 RFQ3-13074/10/NL/PA
M. Bagatin, S. Gerardin, A. Paccagnella, Università di Padova

Multi-Level-Cell (two bit per cell), 32Gbit Micron MT29F32G08CBACA (25nm technology) do not behave as well: TID tolerance ~20krad

MLC: Retention Errors

Retention Errors [bytes]: 0.0E+00, 5.0E+07, 1.0E+08, 1.5E+08, 2.0E+08, 2.5E+08, 3.0E+08

Dose [krad]: 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100

MG17 high duty cycle
MG18 high duty cycle
MG21 high duty cycle
MG19 low duty cycle
MG43 low duty cycle

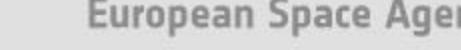
MLC: Block Erase Fails

Errors [blocks]: 0, 50, 100, 150, 200, 250, 300

Dose [krad]: 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100

MG17 high duty cycle
MG18 high duty cycle
MG21 high duty cycle
MG19 low duty cycle
MG43 low duty cycle
MG1 ref high duty cycle

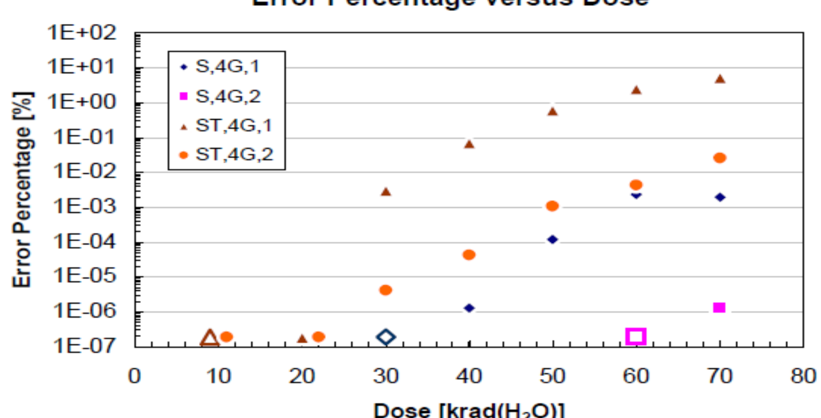
ESA Contract 2011-2012 RFQ3-13074/10/NL/PA
M. Bagatin, S. Gerardin, A. Paccagnella, Università di Padova



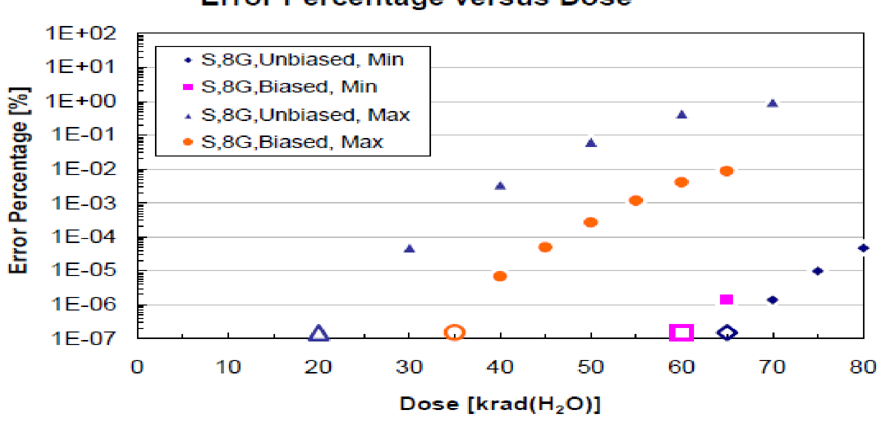
TID in Flash memories (3)

Significant sample-to-sample variation is observed on the TID sensitivity, for the same procurement batch between tested samples (applies to all COTS as well)

8-Gbits NAND-Flash, Samsung & ST



[Schmidt, et al. IDA, 2008] under ESA contract



Min and max shifts for biased vs unbiased tests: 10 + 8 samples

Synergy: Influence of TID on SEE sensitivity? (1)

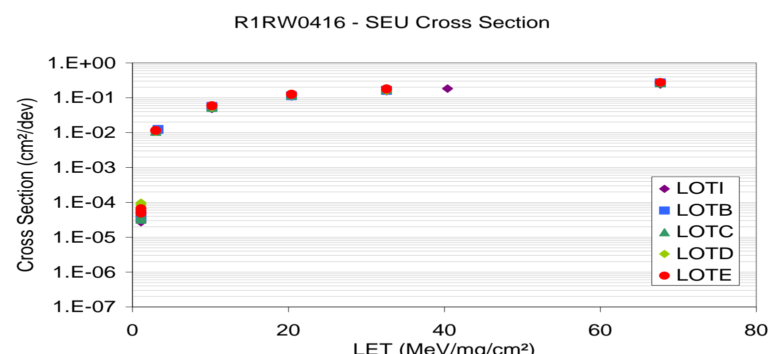
- Synergistic effect of TID on SEE sensitivity reported by some US teams on memory devices
- An ESA study on this potential synergistic effect in the frame of the JUICE mission where expected TID levels >> Earth orbiting or interplanetary missions on 4 test vehicles initiated in 2011

	AD9042	AD558	MT29F4G08AAC	R1RW0416
Manufacturer	Analog Device	Analog Device	Micron	Renesas
Date code	1314	1116	1346	1350
Type	ADC 12bit	DAC 8bit	NAND flash	SRAM 16Mb 8bit
Effects	SEU, SET, SEL	SET, SEL	SEU, MBU, SEL, SEFI	SEU, MBU, SEL

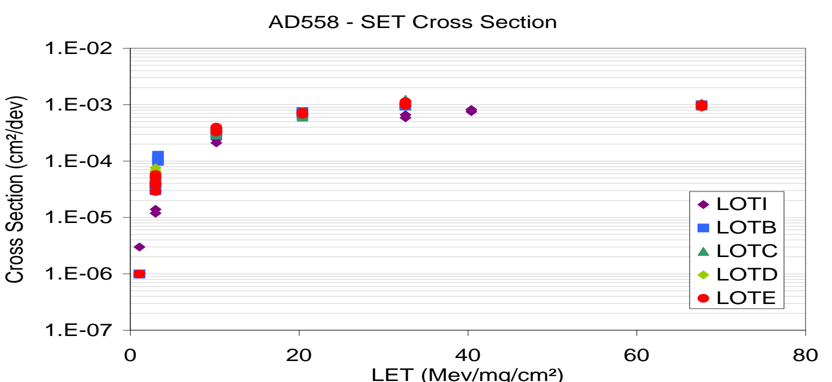
Synergy: Influence of TID on SEE sensitivity? (2)

- No measurable impact of increasing TID (> 100krad) on SEE sensitivity (saturated cross section and LETthreshold) observed on any of the 4 reference types, regardless of biasing conditions during TID tests.

Results on SRAM R1RW0416 from Renesas:



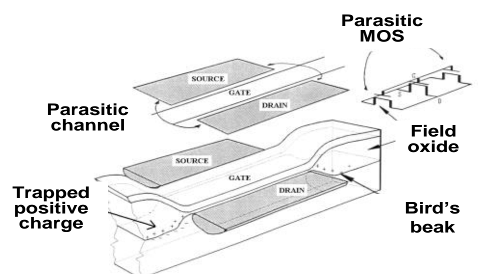
Results on AD558 from Analog device:

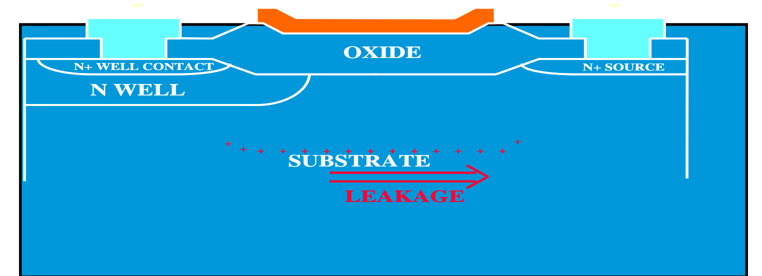


Final presentation by TRAD, TID influence on the SEE sensitivity of active EEE components, ESA contract #4000111336/14/NL/SW

Technological Trends (1)

- Moore's law scaling mostly beneficial: highly scaled CMOS technologies (with standard design) tend to be less sensitive to TID:
- Downscaling implies thinner gate oxides:
  - ➢ Improves TID hardness (less oxide traps)
  - ➢ Lower gate leakage with TID
  - ➢ But possible rising concern with defects and DD effects
- Junction temperature is often high (~100° C) ➔ auto-annealing
- Reduction in spacing may bring other mechanisms such as parasitic channel (source – drain leakage)
- Beware of I/O elements such as ESD protection

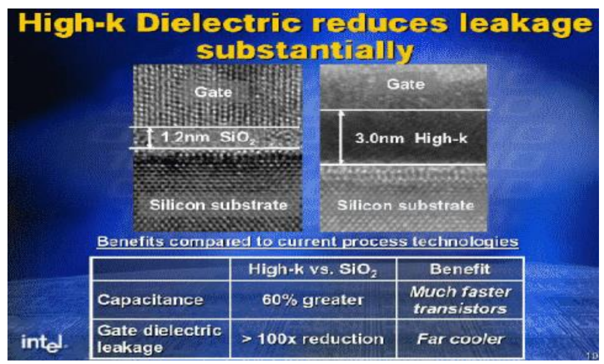




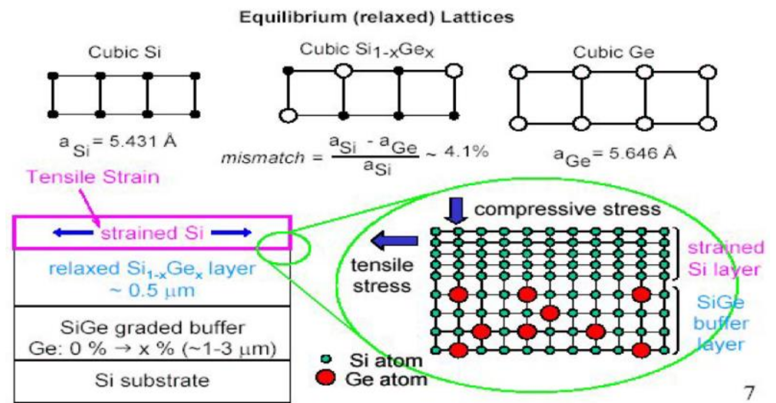
After Gerardin, RADECS 2015

Technological Trends (2)

- Available results (rare) on high-k dielectric and strained silicon technologies do not show to date a negative impact of these features on TID performance.



	High-k vs. SiO2	Benefit
Capacitance	60% greater	Much faster transistors
Gate dielectric leakage	> 100x reduction	Far cooler



After Gerardin, RADECS 2015

Technological trend: FINFETs

FIN

GATE

After Gerardin, RADECS 2015

(a) narrow fin

Si fin

Buried oxide

(b) wide fin

Si fin

Buried oxide

200nm

Source

Gate

Drain

Courtesy of IMEC 2011

- Narrow FinFETs less susceptible to TID due to lower impact of traps in BOX

Summary: Technologies susceptible to TID effects

Technology category	Sub categories	Effects
MOS	NMOS PMOS CMOS CMOS/SOS/SOI	Threshold voltage shift Decrease in drive current Decrease in switching speed Increased leakage current
BJT		hFE degradation, particularly for low-current conditions
JFET		Enhanced source-drain leakage currents
Analogue microelectronics (general)		Changes in offset voltage and offset current Changes in bias-current Gain degradation
Digital microelectronics (general)		Enhanced transistor leakage Logic failure from (1) reduced gain (BJT), or (2) threshold voltage shift and reduced switching speeds (CMOS)
CCDs		Increased dark currents Effects on MOS transistor elements (described above) Some effects on CTE
APS		Changes to MOS-based circuitry of imager (as described above) – including changes in pixel amplifier gain
MEMS		Shift in response due to charge build-up in dielectric layers near to moving parts
Quartz resonant crystals		Frequency shifts
Optical materials	Cover glasses Fibre optics Optical components, coatings, instruments and scintillators	Increased absorption Variation in absorption spectrum (coloration)

[ECSS-E-10-12]

Bibliography

IEEE NSREC 2011 short course notes

Tim Oldham, Basic Mechanisms of TID and DDD response in MOS and Bipolar Microelectronics

SOI conference short course notes

J. R. Schwank and P. E. Dodd, "Radiation Effects in SOI Microelectronics."

RADECS 2015 short course notes

Simone Gerardin, "Space radiation effects in modern and advanced electronics devices."

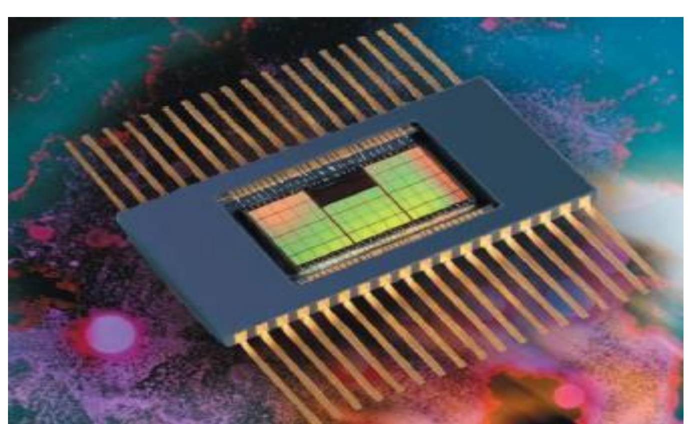
ECSS E-ST-10-12C, "*Methods for the calculation of radiation received and its effects, and a policy for design margins*", http://www.ecss.nl/

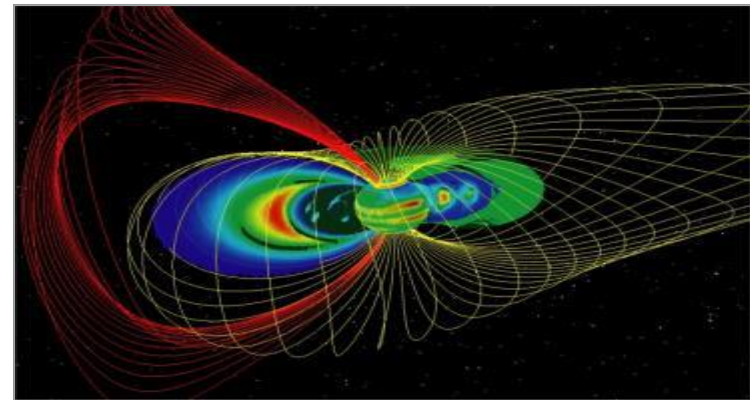
A. Holmes-Siedle, L. Adams. "*Handbook of Radiation Effects*", Oxford University Press

Total Ionising Dose Testing

Irradiation testing (introduction 1)

Irradiation testing is performed to identify whether a component meets specification / application requirements when exposed to desired / application radiation doses.



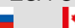


Irradiation testing (introduction 2)

- Irradiation testing is performed for a variety of reasons
  - Testing carried out as part of component manufacturing / radiation hardening; terrestrial and space applications (e.g. by ASIC manufacturer)
  - Testing carried out as part of evaluation / qualification activities (e.g. ESCC22900)
  - Testing carried out as part of space project activity (e.g. Lot Acceptance Testing (LAT)).
  - Testing performed as part of standardisation activities (e.g. to develop irradiation test methods, Radiation Hardness Assurance requirements)

Irradiation Test Principles (1)

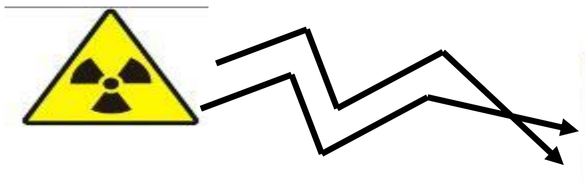
- Irradiation tests are performed to characterise all radiation effect types
- Test principals are the same
- However, each radiation effect has its particularity, for example:
    - TID testing (cumulative effect) may require extended time (months) at irradiation test facilities (in particular for ELDRS testing). Material activation not a problem if testing with photons (e.g. Co60 source)



Irradiation Test Principles (2)

- **Personnel safety**

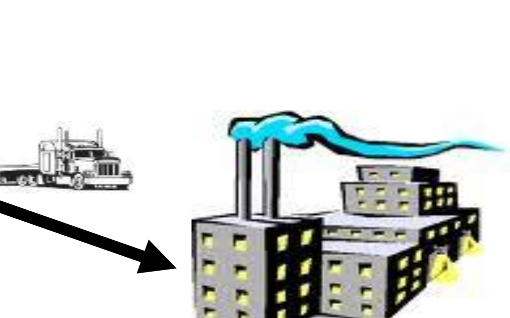
- Can not use devices for flight following irradiation testing. TID is a **destructive** test.



Device under test

Testing at facility, Test Equipment

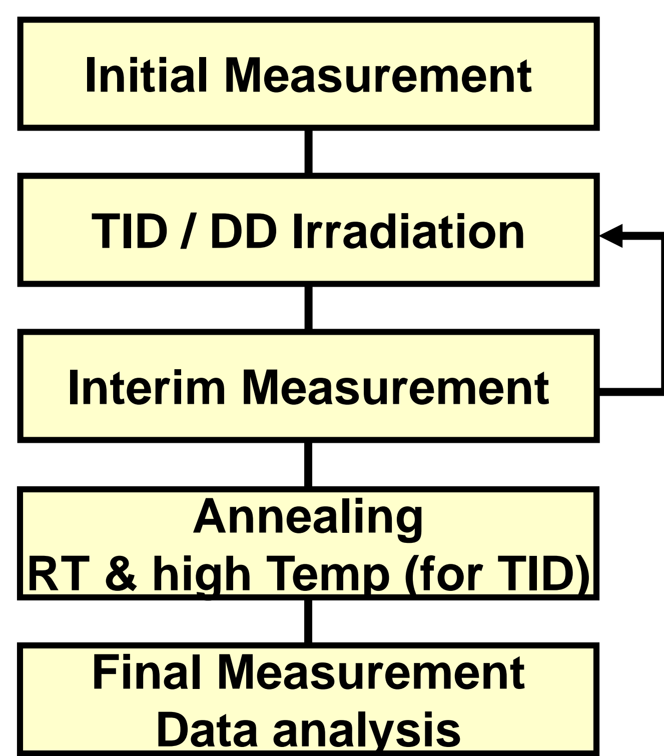
- Radiation Exposure
  - Heavy Ions, protons, neutrons, gammas, electrons, X-rays



Measure dose / fluence, dose rate / flux

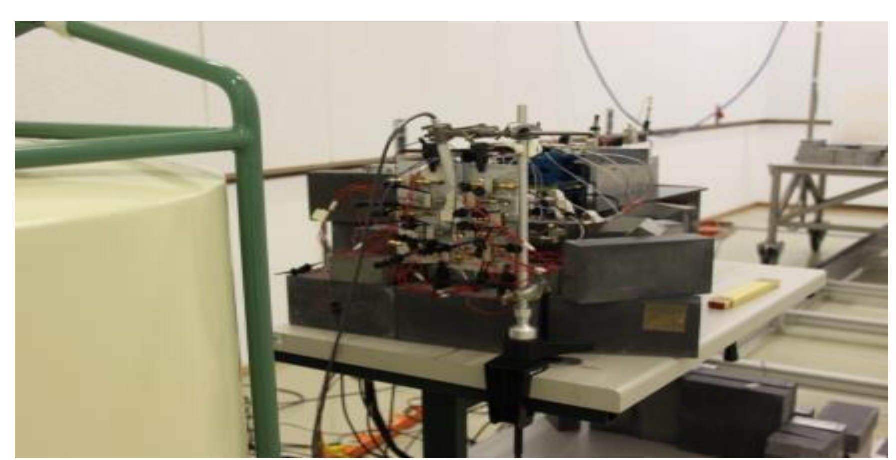
Transport from / to laboratory

Irradiation Test Principles (3)



TID test complexity

- The complexity of TID testing varies with the complexity of the tested device and the application / environmental condition for which the device shall be tested at.
- Thus, TID testing may be as simple as testing a bipolar transistor or more complex such as testing a high speed ADC or ASICs.
- For complex devices, electrical characterisations at each intermediate measurement (e.g 10krad step) can be long -> the 2hr window allowed by the ESCC22900 btw 2 irradiation sequences can be an issue (use several test benches, dry ice etc to alleviate)



Parameter influence on TID sensitivity

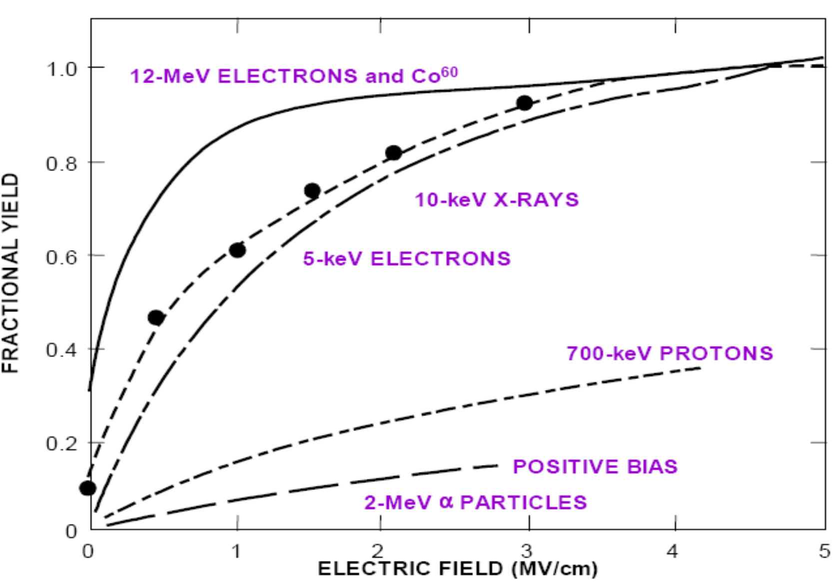
- TID testing is performed to recreate the physical mechanisms involved when devices are exposed to the space environment. We are typically concerned about:
  - Oxide trapping
  - Interface trapping
  - Radiation induced leakage current
  - Gain degradation
  - Modification of timing characteristics, etc
- All these effects are dependent on conditions such as
  - Temperature (testing in flight conditions can be challenging for e.g. sensors operated at cryogenic temperatures)
  - Electrical fields across oxides (magnitude and polarity, thus biasing conditions)
  - Dose rates (Industry not always in agreement with ESA on dose rate in particular for ELDRS testing)
  - Process and technology
  - Application conditions, etc.
  - Aim at “Test as you fly, fly as you test”

Radiation sources applied

- TID testing employing ^{60}Co facilities (gamma source) has over the years become the de-facto standard test method.
- In some cases electrons, protons and x-rays are also used to perform TD testing.
- Care has to be shown when employing other sources than ^{60}Co (dosimetry and dose rate).
- We are not concerned with gammas in space. However, empirically it has been shown that 60Co testing is conservative compared to testing with protons or electrons.
- This is due to the electron-hole pair generation (ionisation) yield (recombination efficiency) in matter that varies with particle species, energy and field across oxide.

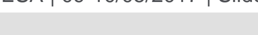
Recombination and yield

- Depends on radiation source and field over oxide

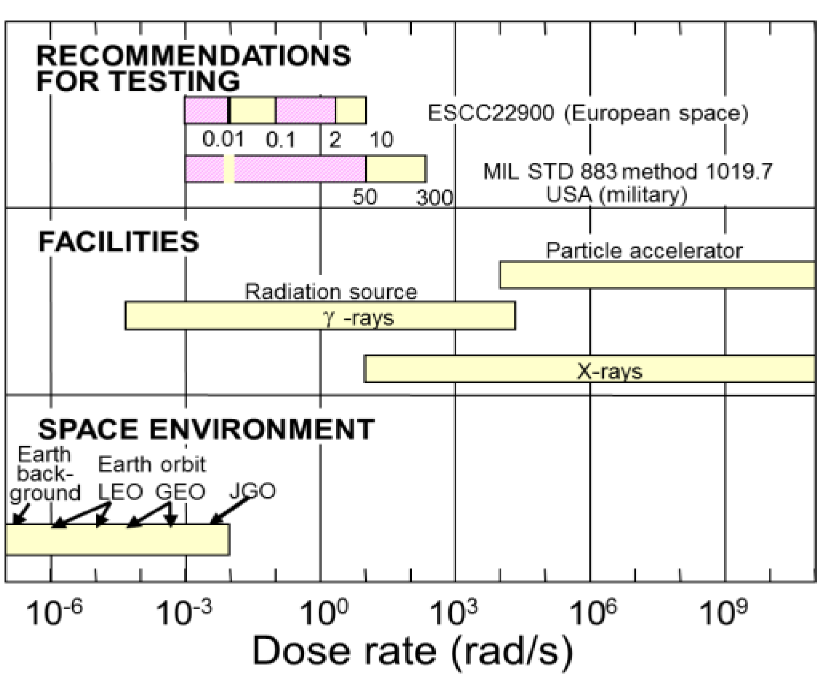


After: JPL course by J.Conley

^{60}Co irradiation is considered **worst case** and has become a **standard** for TID testing.



TID - Radiation Sources and Dose Rates

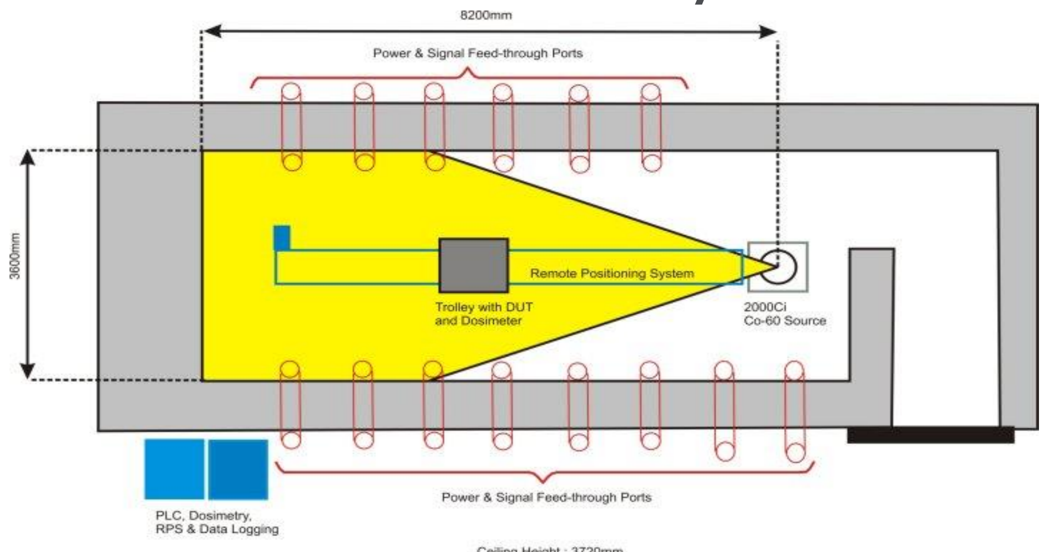


- The laboratory dose rates are significantly higher than the actual space dose rates, testing according to test standards gives conservative estimates of CMOS devices TID sensitivity

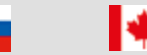
After A Holmes Siedle and L Adams, Oxford Un. Press, 1993

^{60}Co Test Facilities

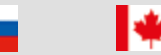
- **ESTEC ^{60}Co Facility (https://escies.org/)**
  - **Dose rates:**
    - **6 krad/h (next to source) down to 36 rad/h (at the end wall)**
    - **ISO17025 certified dosimetry chain**



^{60}Co source



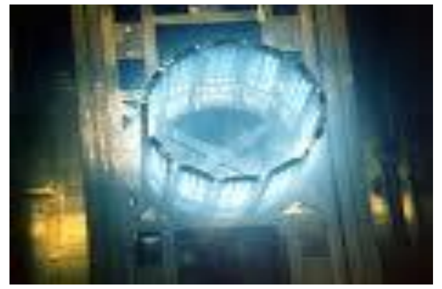
ESTEC's ^{60}Co Test Facility "live footage"



^{60}Co Test Facilities

- A number of other facilities in Europe
  - Medical application
  - Sterilization (food, medical equipment)
  - Research (e.g. biology)
  - Dedicated component radiation facilities

Medical facility (Cancer therapy)



^{60}Co pool facility

Shepherd facility (self standing, shielded room not required)

Standard, test methods (1)

- ESCC 22900
  - Total Dose Steady-State Irradiation Test Method. Issue 5 released in 2016.
- Others
  - MIL-STD883G Method 1019.9 “*Ionizing Radiation (Total Dose) Test Procedure*”
  - MIL-STD750E Method 1019.5 “*Steady-state Total Dose Irradiation Procedure*”
  - ASTM F 1892-06 “*Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor*”

Standard, test methods (2)

- ESCC 22900 splits into three domains
  - **Evaluation**
    - Main objectives to establish worst case conditions for TID qualification (specific for device/technology).
      - Dose level
      - Dose rate effects
      - Bias dependency
      - Critical parameters
      - Annealing effects
      - Etc.
  - **Qualification**
    - Main objectives to qualify or verify a specific device and/or diffusion lot
    - Test conditions defined in TID evaluation testing
  - **Testing outside of an ESCC context**
    - New section introduced when ESCC qualification is not targeted
    - Same test flow as for the the ESCC evaluation/qualification but:
    - No hard requirements in terms of sample size, dose rates, pass/fail criteria (can be project and/or application specific not just related to the datasheet).

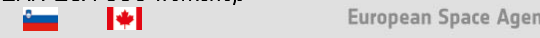
ESCC22900 highlights, sample size

- ESCC evaluation: A minimum of 11 samples at random from two different wafer lots. Making a minimum of 22 samples.
- ESCC qualification: A minimum of 11 samples at random per wafer lot
- The requirements above are meant for component manufacturers seeking ESCC qualification
- Equipment manufacturers loosely employ 11 devices for their Radiation Verification Testing (RVT) or Radiation Lot Acceptance Testing (RADLAT).
- Equipment manufacturers modify this requirement to typically irradiate test 3 to 5 devices per radiation condition.
- However, in some cases equipment manufacturers may use lower sample numbers (e.g. for bipolar based ICs 3 samples in biased mode and 1 sample in unbiased mode). Not recommended as gives low statistical confidence.
- In some cases for very expensive parts, number of samples may be reduced.

ESCC22900 highlights, dose rate

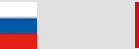
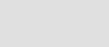
- Dose rate windows modified in latest version of ESCC22900:
  - Window 1: 360(Si)rad/h to 180(Si)krad/h
  - Window 2: 36(Si)rad/h to 360(Si)rad/h
- Window 1 has been extended in support of European component manufacturers (enabling them to apply MIL-STD dose rates) and suppress the gap between the 2 windows (lower rate of Window 1 was 3.6krad(Si)/h).

- For bipolar based devices and for some ESA missions the Agency requirement states 36rad(Si)/h. However, this has in many cases been strongly contested by industry who prefer to use 360rad(Si)/h.

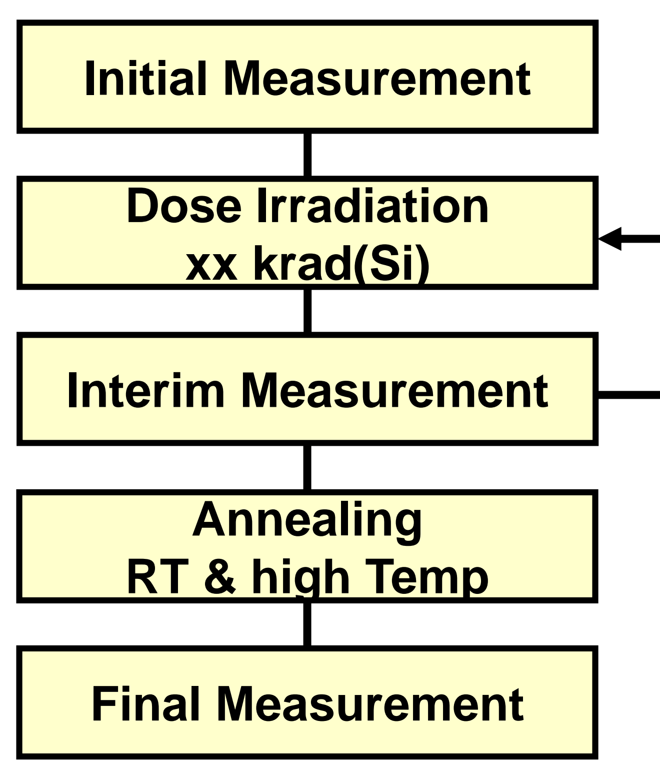


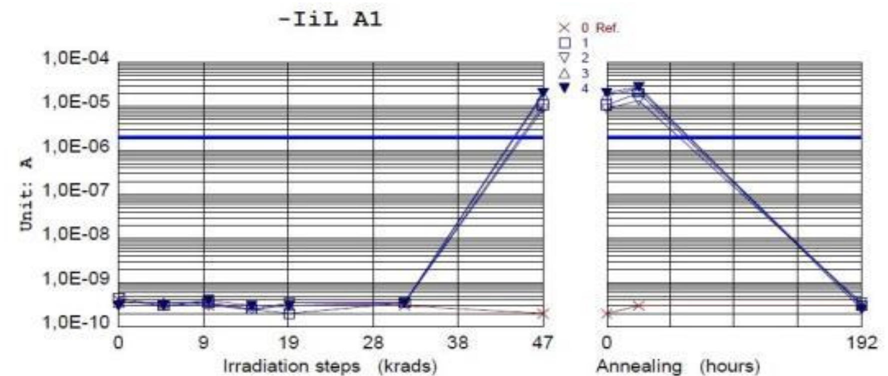
TID testing practical considerations

- Skip Evaluation testing and go directly to Radiation Verification Testing (RVT) (section 7 in the ESCC22900 “Outside of an ESCC context”)
- Select Dose level from design needs rather than device capability
- Sample number is often reduced by industry (employ statistical method to calculate associated margin)
- Select Bias- and test condition based on application conditions (“Test as you fly, fly as you test”!)
- Might need to split test into more than one bias case
- Critical electrical parameters selected from design requirements
- Previous knowledge for similar technologies. Some examples
    - Bipolar, low dose rate (ELDRS) is worst case
    - MOS, high dose rate is worst case (mostly)
    - Bipolar devices may be more sensitive un-biased
    - => in all cases split test, biased and un-biased

Typical test method





Parameter: Negative input current low level

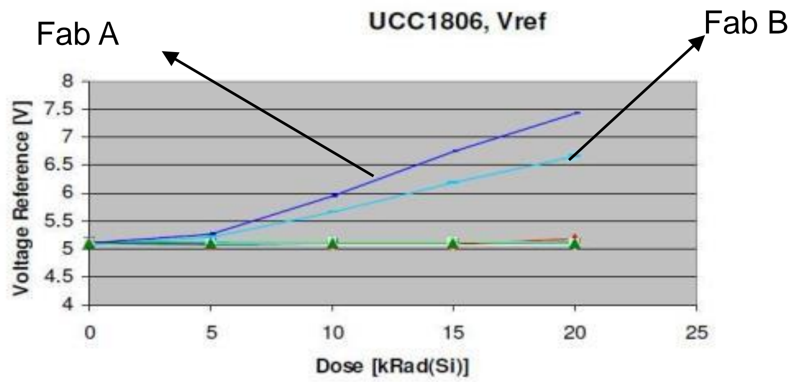
TID characterisation of Hitachi HM6216255H 4Mb static RAM. CMOS technology

Dose rate: 200rad/h

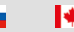
Out of specified limits between 32 and 47 krad.

Following annealing parameter return to pre-irradiation levels

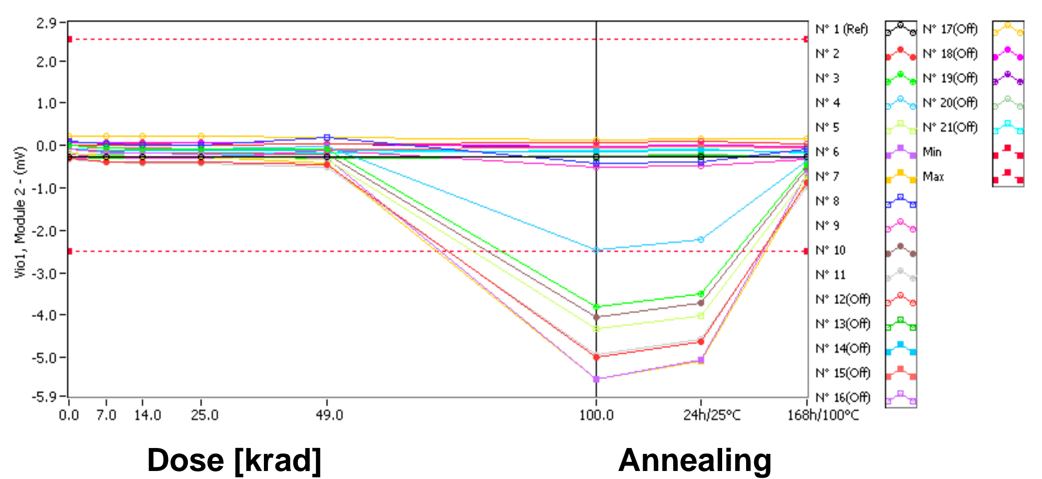
ELDRS testing (example 1)



- Two irradiation tests of TI UCC1806 (different lot and fab)
- Dose rate: 36 rad/h in both cases
- Fab B performs better than Fab A
- At the time of testing TI claimed 30krad tolerance (based on old data)
- ELDRS testing usually large spread in results. Sample size important. Small sample size results in large margins.



ELDRS testing (example 2)



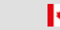
- ELDRS testing usually large spread in results. Sample size important. Small sample size results in large margins.
- As opposed to CMOS unbiased testing of bipolar based devices ICs in some cases more damaging.
- Annealing of bipolar based ICs do not always provide useful information of device performance (although rare case of rebound effect reported).

Before Going to a Radiation Test Facility

(also to a large extent applicable to DD and SEE testing)

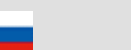
- Ensure that a comprehensive test plan is in place
- The test plans shall include all information necessary to ensure a successful irradiation test campaign and as a minimum shall:
    - identify test standard employed
    - **identify test samples (labeling), date code, lot number**
    - **identify the parameters to be tested**
    - **Identify pass/fail criteria**
    - define the test environment
        - Operational conditions
        - Thermal environment
        - Other environmental requirements
    - identify the irradiation source
    - **define dose rate and dose steps**
    - measurement sequence including timing requirements (e.g. time between testing and initiation of irradiation tests)
    - annealing sequence
- More information may be found in the ESCC22900

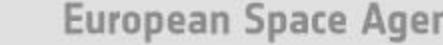
- Before coming to the facility ensure that test system is compliant with facility requirements.



At the Facility

- **Ensure that facility is compliant with your requirements**
  - Need to be able to cater intermediate parametric measurements within required time (less than 1 to 2 hours).
  - Possibly maintain equipment for annealing tests
- **Dosimetry usually done by facility staff and accurate to ~ ±5% to ±10%**
  - ion chambers (TID, DD)
  - silicon surface barrier detectors (TID)
  - Geiger-müller, (TID)
  - Termo-luminescent dosimeters (TID)
- **Dosimetry is important and human errors can occur!**
  - Take care
  - Possibly dosimetry performed by customer (bring reference dosimeter)
  - Spare devices can be useful if re-test needed
- **Time required at facility (test to 100krad).**
  - For CMOS testing at high dose rate: approximately 3 (at 36krad/h) to 27 (at 3.6krad/h) hours
  - For bipolar based devices: Approximately 12 (at 360rad/h) to 120 (at 36 rad/h) days
- **Plan for transportation**
  - It may be better to perform intermediate measurements at your laboratory (test equipment not mobile). Require shipping devices back and forth to irradiation facility. But beware of annealing (dry ice an option to mitigate)
  - Alternatively, use more devices at the irradiation facility to cover a number of dose steps prior to intermediate measurements at your laboratory





To remember for TID testing

- Usually employ **^{60}Co facility**
- Test sample may be used as is, **no de-lidding necessary** (no range issues with gamma-rays)
- Irradiation in **air** (no vacuum), **no material activation**.
- Minimum **5 samples** per irradiation condition is recommended
- Biasing conditions:
  - Bipolar based ICs, irradiated both biased and unbiased **at low dose rates**
  - CMOS typically irradiated biased and unbiased **at high dose rates**
- Beam time **cheaper** than proton and heavy ion testing

TID Irradiation Test Facilities

- Isotron UK: providing 60Co, electron beam and protons up to 10MeV. http://www.isotron.com/
- ENEA-Casaccia (Rome , Italy) Calliope 60Co gamma ray facility (in pool) http://www.casaccia.enea.it/
- Náyade-CIEMAT (Madrid, Spain) 60Co irradiation test facility (in a pool) http://www.ciemat.es
- UCL (Louvain-la-Neuve, Belgium) 60Co facility, http://www.uclouvain.be/en-universite.html
- CEA (Saclay, France) 60Co facility http://www.cea.fr/le_cea/les_centres_cea/saclay
- ONERA DESP (Toulouse, France) 60 Co facility, http://www.onera.fr/desp-en/facilities.php
- ESTEC (Noordwijk, The Netherlands) 60Co facility, https://escies.org/ReadArticle?docId=251
- TRAD GAMRAY (Toulouse, France) 60Co facility, http://www.trad.fr/GAMRAY-Co60-Irradiation-Facility-118.html
- ALTER RADLAB (Seville, Spain) 60Co facility, http://www.altertechnology.com/atn/en

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