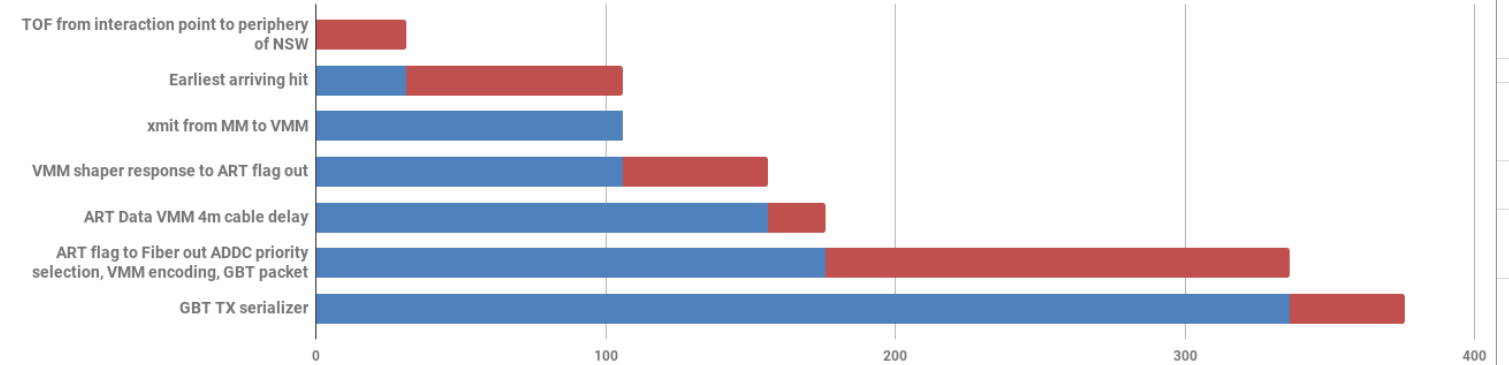


MM Trigger latency

item #	Component	Responsible	Start	End	Min	Latency	status	Comment
						6.84	PCB trace propagation speed (ns/m)	
						5.0	twinax propagation speed (ns/m)	
						320	3.125	pad trigger clock period (ns)
						320	3.125	trigger processor clock period (ns)
UX15								
	0.00	TOF from interaction point to periphery of NSW	0	31		31.0	calc	To outer radius of NSW QL3P @R=4.596m Update for MM?
	1.00	Earliest arriving hit	31	106		75	estim	Is this worst case Ionization statistics? should it also include a separate transmit to VMM latency?
VMM	2.00	xmit from MM to VMM	106	106		0		
	3.00	VMM shaper response to ART flag out	106	156		50	simul	Peaking time, could be up to 200.
ADDC	4.00	ART Data VMM 4m cable delay	156	176		20	calc	
	5.00	ART flag to Fiber out ADDC priority selection, VMM encoding, GBT packet formatting	176	336		160	meas	Lin measured the ADDC latency from "miniSAS connector to fiber out" to be 200ns. I assume this included the TX serializer, check this point
	7	GBT TX serializer	336	376		40	meas	start point is the rising edge of Tx Frame Clk which samples the labeled Tx frame data. End point of the whole TX side is when the first serial bit of the last word W6 is transmitted out from the FPGA transceiver
USA15								
	8	FIBER: ADDC to TP	376	701		325	model	Should this be expanded into different fiber segments?
Trigger Processor	9	Trigger processor GBT deserializer. (BNL latency ptimized version)	701	745		43.9	meas	The RX start point of the transceiver is when the first serial bit of W6 is received; the stop point is when the 20-bit parallel data RxWordData changes from W5 to W6 $LAT_{rxW B} = 2 \cdot Cycle + (3 \cdot Cycle + 110.5 \cdot U I) \cdot 1 UI$ (Unit Interval) means 1/4.8GHz, 1 Cycle = 1/240MHz
	10	Allign 32 fibers	745	770		25	estim	not sure how misaligned the ADDC fibers will be
	11	GBT packet decoding	770	795		25	meas	includes hit map decoding
	12	Finder from decoded hit to first coincidence trigger	795	826		31.25	meas	Assumes we integrate hits for 2 BC. Each additional BC will add 25ns (8 TP clocks)
	13	Fitter critical path	826	864		37.5	meas	MX Local 8 TP clocks, dTheta 4 TP clocks.
	14	Collect Fitter data	864	889		25		
	15	Format track candidate data	889	895		6.25	estim	Collect fitter data and format into a track candidate
	16	xmit MM candidate data to sTGC FPGA	895	907		12.5	estim	
	17	Merge MM and sTGC segments	907	932		25	estim	
	18	Re-synch to 320 MHz clock driving output serializer	932	957		25	estim	
	19	Serializer parallel in to 1st bit out to Sector Logic	957	975		17.8	estim	Value taken from sTGC latency spreadsheet
		20	Fiber delay: Trigger Proc to Sector Logic 4m	975	995		20	estim
			budget 1075					

NSW trigger latency -- UX15



NSW trigger latency -- USA15

