Silicon Epitaxy
Production, challenges, trends

November 2017
Presentation overview

- Epitaxial silicon deposition
  - Growth methods, doping and auto-doping
  - Reactor types and capabilities
  - Effect of epitaxial deposition on wafer flatness
- Epitaxial defects
  - Structural epi-defects
  - Slip and misfit dislocations
- Epitaxial layer metrology
- Epitaxy for CMOS Image Sensor
  - Requirements for CIS applications
  - Improvements in metal contamination and resistivity
  - Multiple layers design, SOI
- Silicon wafers and EPI wafers market
- Conclusions
Epitaxial silicon deposition

• “Epitaxy” is a general term that refers to a deposition of a crystalline layer on a crystalline substrate
• Epitaxy can be
  – homo-epitaxy, where the layer deposited is of the same material as the layer underneath or
  – hetero-epitaxy, where the layer deposited is from a different material than the substrate
• The precursors can be in liquid phase (LPE), solid (MBE) or in the gas phase (CVD)
• Silicon epitaxy is a CVD process
  – CVD started in the prehistoric age with paintings drawn with soot on cave walls
  – CVD is also used in a nice test to detect As in forensic toxicology also described by Agatha Christie...
Epitaxy growth methods

• Silicon CVD epitaxy is widely used in the semiconductor industry for several reasons:
  – It provides a more consistent doping than standard CZ material.
  – It is used for vertical doping profiles for bipolar technologies or drift regions in MOSFET and IGBTs.
  – As advanced solution for logic and memories due to low defect layer (no oxygen and oxygen-related defects) and suppression of latch-up using heavily doped substrates.

• The process involves reduction of chlorosilanes (SiCl4, SiHCl3, SiH2Cl2, SiH4) at high temperature (~ 900 °C - 1150 °C), e.g.:
  – SiHCl3 (v) + H2 (v) → Si (s) + 3HCl (v)
    • Hydrogen is used as reducing agent and carrier gas.
    • The reaction is surface catalyzed.
    • SiHCl3 (TCS) and SiH2Cl2 (DCS) are typical silicon sources.
    • Good balance between safety / process needs in atmospheric conditions.
    • TCS is the preferred source (liquid at RT and medium high deposition temperature).
    • SiH4 is used when a low transition region or no pattern shift is requested. Very low deposition temp (900 °C) but more difficult to manage than TCS.
    • SiCl4 requires too high deposition temperature.
Growth Mechanism

1) Transport of reactants to the deposition region
2) Transport of reactants from gas stream through boundary layer to the wafer surface
3) Adsorption of reactants on the wafer surface
4-6) Surface reactions: decomposition or reaction, migration and attachment at kink/ledge sites
7-9) Desorption and transport of byproducts
Deposition rate

• The deposition rate depends on temperature and gas flow

Doping and auto-doping

- The dopant is co-deposited with silicon
- Dopant used are B₂H₆, PH₃ and AsH₃
- Unintentional doping of the layers is due to auto-doping processes and influences the transition region and the radial resistivity uniformity

Gas-phase autodoping: Dopant from wafer backside and edges.

Solid-phase out-diffusion: Dopant diffusing up from substrate.

System autodoping: Dopant from other wafers, susceptor and reactor wall.

Highly doped substrate

Lightly doped epi
Doping and auto-doping

- To minimize the impact of auto-doping the wafer producer can
  - Add back-seal layer
    - Silicon dioxide layer in thickness range of 0.3-1um
    - Typically deposited in CVD furnace (WJ belt furnace)
    - Requires edge strip to avoid nodule / particle formation during epi growth
    - Epi layer deposition on back of wafer in thickness range 15-20um
  - Hardware modifications
    - Susceptor modifications
    - Applied to 200/300mm double side polished wafer products
EPI transition region

Metallurgical junction

Outdiffusion contribution
\[ f(\text{Temp}, \text{Time}, \text{dopant species}) \]

System autodoping
\[ f(\text{chamber conditions, presence of backsealing..}) \]

Intentional doping
Epi reactors schematics

- Heater power supply and temperature controls
- Gas flow controls
- Gas inputs: H₂, TCS, HCl, B₂H₆, PH₃, AsH₃
- RF or lamps
- Reactor chamber
- Wafer loader
- Gas scrubber
- Plant exhaust
- Reactor exhaust
- Batch
- Single Wafer
Single wafer reactors

Multiple Chamber reactor (AMAT Centura)

Single chamber
ASM Epsilon

Single chamber
ASM Epsilon
Pancake RF Reactors

Confidential and Proprietary Information
### Process and capability

**ADVANTAGES**
- Higher throughput for small diameters
- Easier diameter change
- Improved LPDs performances
- Improved thickness and resistivity performances
- Better transition region
- Same as SWR
- Higher productivity respect to SWR single chamber
- Lower COO

**DISADVANTAGES**
- Low throughput high diameter
- Poor capabilities for advanced 150 and 200mm
- Manual load/unload
- Diameter change more difficult respect to batch
- Not cost effective for high epi thickness
- Sometime reduced uptime for maintenance related to chamber interaction

**Diameter and Reactor**

<table>
<thead>
<tr>
<th>Diameter</th>
<th>Reactor</th>
<th>Thickness Uniformity</th>
<th>Resistivity Uniformity</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;=150mm</td>
<td>Batch Barrel</td>
<td>5%</td>
<td>7%</td>
</tr>
<tr>
<td>150mm</td>
<td>Single Wafer</td>
<td>2%</td>
<td>4%</td>
</tr>
<tr>
<td>200mm</td>
<td>Single Wafer</td>
<td>2%</td>
<td>5%</td>
</tr>
<tr>
<td>300mm</td>
<td>Single Wafer</td>
<td>2%</td>
<td>7%</td>
</tr>
<tr>
<td>150mm and 200mm</td>
<td>Pancake</td>
<td>2%</td>
<td>5%</td>
</tr>
</tbody>
</table>
Influence on wafer shape of epitaxy

- Wafer shape (bow and warp) is an important parameter during the fab processing for device formation
- Bow and warp are changed during the EPI process by
  - Stress induced by lattice mismatch between substrate and epitaxial layer (different dopant concentration)
  - Change in the densification of backside layers

Before EPI

After EPI

Final shape in between
Factors influencing wafer bow

\[
Bow = 3 \cdot \left( \frac{R}{h_s} \right)^2 \cdot h_f \cdot \varepsilon
\]

\[R = \text{wafer radius}\]
\[h_s = \text{substrate thickness}\]
\[h_f = \text{film thickness}\]
\[\varepsilon = \text{lattice mismatch}\]


\[
\varepsilon = \frac{1 - R_d}{N_{Si}} (N_d^s - N_d^f)
\]

\[a_d = \text{covalent radius of dopant}\]
\[a_{Si} = \text{covalent radius of silicon}\]
\[N_d = \text{Dopant concentration in substrate (S) and film (f)}\]

\[
R_d = \frac{a_d}{a_{Si}}
\]

\[
E_f \cdot \int_{T_{room}}^{T_{process}} (\alpha_f - \alpha_s) dT
\]

\[\sigma_f = \frac{T_{process}}{1 - \nu_f}
\]

\[\alpha: \text{Expansion coefficient of the film and of the substrate}\]
\[E_f = \text{young modulus of the oxide}\]
\[\nu_f = \text{Poisson ratio of the oxide.}\]

(Element) Radius [Å] Misfit ratio
<table>
<thead>
<tr>
<th>Element</th>
<th>Radius [Å]</th>
<th>Misfit ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>0.77</td>
<td>0.66</td>
</tr>
<tr>
<td>B</td>
<td>0.88</td>
<td>0.75</td>
</tr>
<tr>
<td>P</td>
<td>1.1</td>
<td>0.94</td>
</tr>
<tr>
<td>Si</td>
<td>1.17</td>
<td>1</td>
</tr>
<tr>
<td>As</td>
<td>1.18</td>
<td>1.01</td>
</tr>
<tr>
<td>Ge</td>
<td>1.22</td>
<td>1.04</td>
</tr>
<tr>
<td>Sb</td>
<td>1.36</td>
<td>1.16</td>
</tr>
</tbody>
</table>

(ref: W.R.Runyan, K.E. Bean “Semiconductor Integrated Circuit Processing Technology)
Defect in epitaxial layers

• Epitaxial defects are generated by a large variety of different sources (substrate, process gases, reactor, environment…)  
  – It is virtually impossible to get a perfect epi layer without any type of crystallographic defects at a reasonable cost therefore the presence of crystallographic defects should be considered part of the process

• The presence of crystallographic defects is detrimental for device performances for several reasons:
  – They could getter metals and therefore produce leakage
  – They could be electrically active and generate leakage
  – They could be large and in this case they could generate issues during photolithography steps.
Some examples

- Some clear effect of defects on devices
  - Dark current images on CCD devices due to stacking faults
  - Spinning defect caused by a large defect

Figure 1. Comparison of epi wafer defects observed optically (top) and electrically (bottom) as 55 °C dark-current images from completed CCD devices. a-c are 21-μm stacking faults, d is a 7-μm stacking fault, and e is a growth hillock. Contrasts among the dark-current images are adjusted to show particular features. All white pixels are not of equivalent brightness*.

Silicon Wafer Defect Self Characterization with CCD Image Sensors
Type of defects

Crystallographic
- Grown-in defects
  - Epi Stacking Faults (ESF)
  - Spike
  - Poly ESF
  - Hillocks
  - Buried particle
- Slip lines
- Misfits
- Crystal defects

Removable
- Particles
- Fibers
- Residue

Scratches
- Pre-epi
- Post-epi
- Work damage
Crystallographic defects

- Type of defects generated by the presence of something added or already present on the substrate surface prior the deposition which perturb the growth of the epi layer
  - 3D defects usually quite large but with variable vertical extension
  - Always visible after epi (no needs of chemical etching)
  - Their size is depending on the epitaxial thickness

- The base of these defects are the EPI stacking Fault
  - A stacking fault, as the word says, is a fault in the regular stacking of the different 111 planes
Crystallographic defects

- Epi stacking faults are generated due to a defect or a particle on the substrate, from which stacking faults are created. The dimension of the EPI stacking fault is proportional to the EPI thickness.

\[
\text{for (100) wafers - square ESFs:} \quad L = 2t \cot(54.7°) = 1.416t
\]

\[
\text{for (111) wafers - triangular ESFs:} \quad L = 2t \cot(70.5°) \csc(60°) = 0.818t
\]
Crystallographic defects

- The Epi stacking fault described before is an ideal situation. Depending on the size and type of defect or particle on the surface a lot of defect might form.
- All these defects can getter metals and be electrically active.

![Graph showing the relationship between substrate particle size and epitaxial thickness.](image)

- Graph legend:
  - Terrace (t: 5μm)
  - Terrace (t: 10μm)
  - Pyramid (t: 5μm)
  - Pyramid (t: 10μm)
  - Piled (t: 5μm)
  - Piled (t: 10μm)
  - Rock (t: 5μm)
  - Rock (t: 10μm)

- Equation: \( \frac{s}{t} = \frac{d}{t} + 1.41 \)
Crystallographic defects

RESULTING ESFs IN EPI LAYER

PARTICLES ON THE SUBSTRATE
Linear defects

• The most important linear defects that we see on Epi wafers are **slips** and **misfit dislocations**

• Slip is crystallographic shift of the (111) atomic layers (plastic deformation) caused by stress that exceeds the wafer’s yield stress
  
  – Stresses are induced by radial temperature gradients in the wafer during heat treatment. Surface damage can concentrate stresses, and exacerbate slip generation
  
  – P- material is more susceptible to slip than P+. (111) orientation is more sensitive than (100)

  – Hardware and process optimization for temperature uniformity. High quality substrates with no damaged areas.
• **Misfit** are linear dislocations that lay at the interface between epi and substrate and are generated when the *lattice mismatch* between substrate and EPI due to the different doping level higher than a certain limit.


Covalent Radius
- Si: 1.17 Å
- B: 0.88 Å
- P: 1.10 Å
- As: 1.18 Å
- Sb: 1.36 Å

If $\text{tepi} < X_{\text{cri}}$, then grow a strained layer.
If $\text{tepi} > X_{\text{cri}}$, then grow misfit dislocations (relaxed layer).
$f = \Delta a/a$ is the fractional lattice mismatch.
Epitaxial layer metrology

• Main metrological tools used in the EPI production
  – FTIR for Epi thickness
    • Reflection of the IR by heavily doped substrates
  – HgCV, SRP and 4PP for Epi resistivity
    • Different techniques for different EPI materials
  – Laser scattering tools for defects and slip detection
    • With PMTs signal elaboration to distinguish between removable defects, crystallographic defects and others
  – ICP/MS for surface metals
  – SPV, DLTS, uPCD for lifetime and deep level characterizations
  – Microscopes, AFM, SEM for defects characterizations
  – Non contact capacitance metrology tools for flatness measurements
Requirements for CIS applications

• CMOS Image sensors are devices with specific requirements for EPI substrates, not present for other applications
  – Low dark current; Low bright spots; High collection efficiency and pixel isolation; wafer usable for backside illuminated devices
• Dark current is mainly influenced by dissolved metals
• Bright spots are generated by epi defects, precipitates, slip and misfit
• The first requirement for CIS EPI are therefore:
  – low epi defect density
  – starting wafer free of slip
  – high quality edge to avoid slip in fab process
  – resistance to slip by optimizing wafer strength
  – no misfit dislocations
  – gettering of fast diffusing metals
  – low concentration of low diffusing metals
Gettering of metals

- Fast diffusing metals that might contaminate the surface during the wafer processing should be removed from the device active region
  - Oxygen precipitates present in the substrate are efficient gettering sites for fast diffusing metals
  - A polysilicon layer deposited on the backside of the wafer is also an efficient protection against metal contamination
- Slow diffusing metals, such as Mo, are more challenging to be gettered

BMD results after precipitation cycle + cleave & etch.

![P/P+](image1)
![P/P-](image2)
![P/P- with MDZ](image3)
![P/P- N-doped](image4)
Reduction of low diffusing metals

• Control of metals from the epi reactor is the key step to ensuring low metals in the epi layer
  – The Epi process is a potential source of metals as it is performed at high temperature in a reducing environment, reactors contain stainless steel components, chlorine by-products from gases combined with moisture can react with the stainless steel components, gas lines, and other reactor components
  – Reactor maintenance generally leads to elevated metals that require a recovery period
    • Epi process control is key to avoiding metal excursion
    • Routine SPV sampling supplemented by DLTS
    • SPV and DLTS qualification of chamber after maintenance and before product runs
    • Current requirements are metals detected with DLTS<1E11 at/cc, MCLT (uPCD)>610usec or SPV Fe<6E10 at/cc
Reduction of low diffusing metals

- DLTS typically detect Mo, Fe, Ti and W
- Detection limit is typically $10^{-5}$ to $10^{-4}$ times the boron concentration, in the range of $10^9$ - $10^{10}$ at/cm$^3$
- Typical distribution of some elements is reported below
Backside illuminated CIS

• The utilization of the backside illuminated sensors is an ideal solution to
  – Increase fill factor and quantum efficiency
  – Make easier the implementation of AR coatings
  – Improve the angular response
  – Enable the implementation of Cu interconnects and low-K dielectrics

• Challenges associated are
  – Accurate die or wafer thinning to as thin as a few microns
  – Back surface that is smooth and capable of being passivated to prevent back surface recombination
  – Incorporation of electric field elements, like a doping gradient, that directs carriers to the collection photodiode
  – Alignment of color filter to pixels
  – Cost sensitive solution
Backside illuminated CIS

- **Wafer design**
  - SOI wafer. Layer transfer and epi growth to create P/P+ stack. Use BOX as stop for the thinning process.
  - P/P+ with graded epi layer. Tune the end of thinning process to depend on boron concentration such as with acid etching where rate slows with decreasing boron. Leaves graded layer for built-in field. More applicable to thick final device layer.
  - P-Epi on P++ Epi on P- Substrate. Use the P++ layer as both an etch stop and source for the doping gradient into device layer.
Semiconductor and silicon wafer market
Semiconductor market

• Overall **semiconductor** industry trend
  – Gartner Q217 semi revenue forecast revised up significantly to nearly 17% growth in ‘17, cracking $400B for the first time in history
Semiconductor market

- Memory, Application-specific standard parts (ASSP) and micro-processors are more than half of the total semiconductor revenue and are using mainly 300mm wafers.
- 200mm wafers are used for ASICs, Analog, Discrete and Optoelectronics.

<table>
<thead>
<tr>
<th>2021 Revenue</th>
<th>Share</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASSP</td>
<td>111,079</td>
</tr>
<tr>
<td>Memory</td>
<td>107,977</td>
</tr>
<tr>
<td>Micro</td>
<td>71,210</td>
</tr>
<tr>
<td>Opto</td>
<td>35,172</td>
</tr>
<tr>
<td>ASIC</td>
<td>30,072</td>
</tr>
<tr>
<td>Analog</td>
<td>26,207</td>
</tr>
<tr>
<td>Discrete</td>
<td>22,181</td>
</tr>
<tr>
<td>NOS</td>
<td>14,912</td>
</tr>
<tr>
<td>GP Logic</td>
<td>13,884</td>
</tr>
<tr>
<td>Total Semi.</td>
<td>431,793</td>
</tr>
</tbody>
</table>

Some columns do not add to totals shown due to rounding. Revenue figures are in millions of dollars.

ASSP = application-specific standard product; ASIC= application-specific integrated circuit; CAGR = compound annual growth rate; GP = general purpose; NOS = non-optical sensor.

Source: “Semiconductor Forecast Database, Worldwide; 2017 Update” (G00036645)
Silicon wafers market

- For 200mm and 300mm wafers the demand is now exceeding the supply

<table>
<thead>
<tr>
<th>Year</th>
<th>12” Market Demand</th>
<th>8” Market Demand</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>4,658</td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>4,356</td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td>4,486</td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td>5,165</td>
<td></td>
</tr>
<tr>
<td>2018</td>
<td>5,500</td>
<td></td>
</tr>
</tbody>
</table>

- **12” supply**
- **8” supply**
Silicon wafers market

• Epi wafers are used mainly for micro-processors, discrete and analog products
• About 30% of the overall market consists of EPI wafers
Thank you