Future trends in sensor design

Stream winter school 2017
CERN
07/11/2017

Thanushan Kugathasan (CERN)
Hybrid pixels

Hybrid pixels are used as tracking devices in the innermost layers of LHC experiments

Sensor and ASIC are independent units

- Separate optimization of sensor and FE-chip
- Fine pitch bump bonding to connect each pixel in the sensor to a readout cell in the ASIC (additional cost and limitation in size)
- Large sensor capacitance (~ 100 fF)
- Thick detector modules: ~ 300 µm sensor + ~ 250 µm sensor
CMOS Image Sensors are standard for detection of visible light and imaging devices.

Can CMOS be used for High Energy Physics Applications?
Pixel sensors based on standard CMOS (Complementary Metal Oxide Semiconductor) process:
- technology used in industry for mass production (low cost per area)
- reduced feature size, multi-layer metal, more functionality per pixel

**Challenge:** integrate the sensors into the CMOS layer

**Hybrid pixels readout chips are based on CMOS**
Advantages of monolithic pixels in High Energy Physics:

- Detector assembly and production cost.
  - Standard CMOS processing (larger wafer diameter, low cost per area)
  - No need for cost intensive fine pitch bump bonding
- Better power-performance ratio (cabling and cooling material reduction)
- Thin detectors (O(50 μm Si)) and high granularity (small pixel sizes)

<table>
<thead>
<tr>
<th></th>
<th>STAR RICH</th>
<th>ALICE-LHC</th>
<th>ILC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required Time Res. [ns]</td>
<td>110</td>
<td>20 000</td>
<td>350</td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>4</td>
<td>10</td>
<td>250</td>
</tr>
<tr>
<td>Non Ionizing Energy Loss Fluence [n_{eq}/cm²]</td>
<td>&gt; 10^{12}</td>
<td>&gt; 10^{13}</td>
<td>10^{12}</td>
</tr>
<tr>
<td>Total Ionizing Dose [Mrad]</td>
<td>0.2</td>
<td>0.7</td>
<td>0.4</td>
</tr>
</tbody>
</table>

ALPIDE - 1.5 x 3.0 cm² 0.5 Mpix (28 um pitch)
In production

G. Aglieri et al,
DOI 10.1016/j.nima.2016.05.016
ALPIDE Sensor Technology

- TowerJazz 180nm CMOS imaging sensor process
- Electronics outside the collection electrode: small electrode, large circuit area, no signal coupling

- Small electrode radius 2-3 µm, small C (< 5 fF)
- NWELL – PWELL spacing
- Deep PWELL shielding NWELL allowing in-pixel PMOS
- Reverse bias to increase depletion volume (-6 V, the sensor is not fully depleted)

25 µm p-type epitaxial High resistivity (> 1kΩ cm)
Charge collection: diffusion vs drift

Minimum Ionizing Particle (MIP) creates $\sim 60$ e/h pairs per micron of silicon traversed (in case of thin silicon)

Example for 18 um thick layer: $1080 \text{ e/h } \Rightarrow 0.17 \text{ fC}$

Collection by drift advantages:

- Tolerance to non ionizing radiation (less trapping probability)
- Reduction of the cluster size (less charge sharing)

<table>
<thead>
<tr>
<th></th>
<th>Diffusion</th>
<th>Drift</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force</td>
<td>Charge carrier concentration gradient</td>
<td>Electric field</td>
</tr>
<tr>
<td>Collection time</td>
<td>$\sim100$ ns</td>
<td>$&lt; 10$ ns</td>
</tr>
<tr>
<td>Minority charge carrier path length</td>
<td>Long</td>
<td>Short</td>
</tr>
</tbody>
</table>

Minimum Ionizing Particle (MIP) creates $\sim 60$ e/h pairs per micron of silicon traversed (in case of thin silicon)

Example for 18 um thick layer: $1080 \text{ e/h } \Rightarrow 0.17 \text{ fC}$
Depletion width

Typical standard process resistivity:
(V_b=0, no additional reverse bias)

ρ ≈ 10 Ω·cm [N_a ≈ 10^{15} cm^{-3}]
⇒ w ≈ 1 µm

High resistivity:
ρ ≈ 1 kΩ·cm [N_a ≈ 10^{13} cm^{-3}]
⇒ w ≈ 10 µm

N_d ~ 10^{18} cm^{-3}
V_{bi} ~ 0.6 V

w ≈ x_p = \sqrt{\frac{2 e (V_b + V_{bi})}{e N_a}}

N_d ≫ N_a  \quad p-epi lowly doped

A larger depletion width (w) can be achieved with a:

• Higher resistivity epi-layer (lower doping)
• Higher reverse substrate bias

Reverse bias:

V_b ≫ V_{bi}

w ∝ \sqrt{V_b}

Larger w ⇒ smaller input capacitance.

note: planar junction calculation

E = 1.6 \times 10^{-19} C
\epsilon = 11.7 \times 8.85 \times 10^{-12} F·m^{-1}
The voltage signal on the collection electrode is the ratio between the collected charge $Q$ and input equivalent capacitance $C$.

$$S = \frac{Q}{C}$$

Signal distribution example

<table>
<thead>
<tr>
<th>Sector</th>
<th>nwell width</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>3 µm</td>
<td>0.00 µm</td>
</tr>
<tr>
<td>5</td>
<td>3 µm</td>
<td>0.60 µm</td>
</tr>
<tr>
<td>6</td>
<td>3 µm</td>
<td>1.04 µm</td>
</tr>
</tbody>
</table>
Consideration on read-out noise

Sensor leakage noise
Proportional to the integration time
Negligible for short integration time (1 μs)

Input transistor noise

\[ dv_{eq}^2 = \left( \frac{K_F}{WLC_{ox}f^\alpha} + \frac{2k_B Tn}{g_m} \right) df \]
for weak inversion

\[ dv_{eq}^2 = \left( \frac{K_F}{WLC_{ox}f^\alpha} + \frac{4k_B T\gamma}{g_m} \right) df \]
for strong inversion

\[ 1/f \text{ noise, thermal noise} \]

\[ N \propto \frac{1}{\sqrt{g_m}} \]

\( \alpha: 0 < \alpha < 2 \)
\( K_F: \) technology dependent constant,
\( W \) and \( L \) are transistor width and length,
\( C_{ox}: \) is the gate oxide capacitance per unit area
\( f: \) frequency
\( g_m: \) transistor transconductance
\( k_B: \) Boltzmann’s constant
\( T: \) absolute temperature
\( n: \) weak inversion slope
\( \gamma: \) a factor often around 2/3.

1/f noise can be reduced by filtering, the thermal noise is dominant.
The proportionality constant depend on the type of filter.
Fixing the S/N for a given bandwidth, lower C/Q allows for a lower power.

\[
N \propto \frac{1}{\sqrt{g_m}} \quad S = \frac{Q}{C}
\]

Assuming that main analog power dissipation comes from the input transistor bias:

\[
\frac{S}{N} \propto \frac{Q}{C} \sqrt{g_m} \propto \frac{Q}{C} \frac{2a}{\sqrt{I}}
\]

\[
g_m \propto I^{\frac{1}{a}}
\]

\[
P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2a}
\]

\[
N \propto \left(\frac{C}{Q}\right)^{2a}
\]

\(a = 2\) in strong inversion
\(a = 1\) in weak inversion
Pixel input capacitance evaluated from the pixel response to 5.9 keV X-rays from an $^{55}$Fe source as a function of the reverse bias voltage.

$C_d \sim 2.5$ fF at -6 V
## ITS Chip General Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Inner Barrel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip size (mm x mm)</td>
<td>15 x 30</td>
</tr>
<tr>
<td>Chip thickness (mm)</td>
<td>50</td>
</tr>
<tr>
<td>Spatial resolution (mm)</td>
<td>5</td>
</tr>
<tr>
<td>Detection efficiency</td>
<td>&gt; 99%</td>
</tr>
<tr>
<td>Fake hit rate</td>
<td>&lt;&lt; $10^{-6}$ evt$^{-1}$ pixel$^{-1}$</td>
</tr>
<tr>
<td>Integration time (ms)</td>
<td>&lt; 10</td>
</tr>
<tr>
<td>Power density (mW/cm$^2$)</td>
<td>~35</td>
</tr>
<tr>
<td>TID radiation hardness (krad) (*)</td>
<td>2700</td>
</tr>
<tr>
<td>NIEL radiation hardness (1 MeV $n_{eq}$/cm$^2$) (*)</td>
<td>$1.7 \times 10^{13}$</td>
</tr>
<tr>
<td>Readout rate, Pb-Pb interactions (kHz)</td>
<td>100</td>
</tr>
<tr>
<td>Hit Density, Pb-Pb interactions (cm$^{-2}$)</td>
<td>18.6</td>
</tr>
</tbody>
</table>

(*) In color: ALPIDE performance figure where better than requirements
(**): 10x radiation load integrated over approved program (~ 6 years of operation)

### Future trends in sensor design - T. Kugathasan - 07/11/2017
In pixel hit discrimination and storage

- Analog front-end continuously active, acts as an analogue delay line (~2 µs peaking time)
  - Power: 40 nW/pixel
- Global threshold for discrimination => binary pulse OUT_D
- Digital in-pixel circuitry with three hit storage registers (multi event buffer)
- Global shutter (STROBE) latches the discriminated hits in next available register
ALPIDE Architecture

512 rows

1024 pixel columns

Bias, Readout, Control

In pixel:
Amplification and discrimination

In matrix:
Zero suppression readout based on priority encoding:
sequential readout of hit pixels address

No free running clock over matrix. No activity if there are no hits
=> power and system noise reduction
ALPIDE pixel matrix cross section and layout

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ALPIDE chip

Matrix sensitive area (512 × 1024 pixels)

Analog DACs

Digital Periphery

Soldering pads

Regular Pads + Custom Blocks: LVDS, MLVDS, CMOS I/O, Bandgap, monitoring ADC

Sensitive area (4.12 cm²) power density 6.2 mW/cm²
Chip power density < 35 mW/cm² (20 mW/cm² with readout from parallel port)

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Large operational margin before and after irradiation up to 10 x lifetime NIEL

\(1.7 \times 10^{13} \text{ n}_{eq}/\text{cm}^2\)
Main challenges for improvement

Specifications for the ATLAS Inner Tracker Upgrade Phase 2 (HL-LHC)

<table>
<thead>
<tr>
<th></th>
<th>ALICE-LHC</th>
<th>ATLAS-HL-LHC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Outer</td>
</tr>
<tr>
<td>Required Time Res. [ns]</td>
<td>20 000</td>
<td>25</td>
</tr>
<tr>
<td>Particle Rate [kHz/mm²]</td>
<td>10</td>
<td>1000</td>
</tr>
<tr>
<td>Fluence [n_{eq}/cm²]</td>
<td>&gt;10^{13}</td>
<td>10^{15}</td>
</tr>
<tr>
<td>Ion. Dose [Mrad]</td>
<td>0.7</td>
<td>50</td>
</tr>
</tbody>
</table>

- **Time resolution**: fast collection by drift (∼ < 25 ns)  ➔ larger depletion
- **High particle rate**: short dead time (< 1 us)
- **Tolerance to non-ionizing radiation (displacement damage)**: fast collection by drift to decrease signal charge trapping probability  ➔ larger depletion
- **High Q/C for power optimization**:
  - **High Q**: less charge sharing (small cluster)  ➔ larger depletion
  - **Low C**: smaller junction capacitance  ➔ larger depletion
CMOS technology for high voltage switching electronics

- Deep n-well collection electrode, risk of coupling circuit signals into input
- Transistors isolated from the substrate (deep n-well)
- High reverse substrate voltage (~ 100 V)
- High resistivity p-substrate (> 2 kΩ cm)
- Charge is collected by drift, good for radiation tolerance
- Limited circuit area, large capacitance (C ~ 400 fF)
LF-Monopix is a demonstrator designed in LFoundry 150 nm HV-CMOS

- **Column-drain architecture:**
  - Time stamp distributed in pixel array
  - Hit information stored in the pixel
  - Hit read out following a priority scan

First measurements: \( Q_{th} \) 2500 e\(^-\), ENC 200 e\(^-\)
No significant loss after irradiation (NIEL \( 2 \cdot 10^{15} \) n\(_{eq}\)/cm\(^2\), TID 150 Mrad)
**TowerJazz Modified process**

- Novel modified process developed in collaboration with the foundry
- Adding a planar n-type layer significantly improves depletion under deep PWELL
  - Possibility to fully deplete sensing volume
  - No significant circuit or layout changes required

![Diagram of the TowerJazz Modified process](image)

25 µm p-type epitaxial layer
High resistivity (> 1kΩ cm)

W. Snoeys et al.
TowerJazz Investigator chip

- Sensor characterization device developed for the ALICE ITS upgrade
- Access to the sensor input signal (rising time ~ 15 ns)

Fit to extract rise time and amplitude

C. Gao et al.
DOI 10.1016/j.nima.2016.03.074
• 134 pixel sub-matrices of different designs (electrode size, PWELL spacing)
• Each sub-matrix contains 8x8 pixels surrounded by dummies
• Possibility of simultaneously measuring the analog signals on 64 pixels

<table>
<thead>
<tr>
<th>Mini-Matrix number</th>
<th>Pixel size</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 – 35</td>
<td>20 by 20 um²</td>
</tr>
<tr>
<td>36 – 57</td>
<td>22 by 22 um²</td>
</tr>
<tr>
<td>58 – 67</td>
<td>25 by 25 um²</td>
</tr>
<tr>
<td>68 – 103</td>
<td>28 by 28 um²</td>
</tr>
<tr>
<td>104 – 111</td>
<td>30 by 30 um²</td>
</tr>
<tr>
<td>112 – 123</td>
<td>40 by 40 um²</td>
</tr>
<tr>
<td>124 – 133</td>
<td>50 by 50 um²</td>
</tr>
</tbody>
</table>
TOWERJAZZ SIGNAL VS COLLECTION TIME

- Better timing with modified process (narrower collection time distribution)

- Modified process after irradiation maintains charge collection

Starting point for ATLAS development after first results of the process modification
Design of large-scale demonstrators

- Measurement results show improved non-ionizing radiation tolerance for sensors manufactured using the modified process

- Analog front-end optimized for timing, based on ALPIDE

- Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers

- The “MALTA” chip
  - Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix

- The “TJ-Monopix” chip
  - Synchronous readout architecture. Uses the well-established column drain readout architecture (experience from LF-Monopix design)
Front-end simulation performance

- Improvement for fast timing (< 25 ns) and hit rate capability by increasing current consumption (250-500 nA/pixel, < 1 μW/pixel)

Time-Walk

\[ P_{\text{analog}} = 0.9 \, \mu\text{W} \]

**Charge threshold** \( Q_{\text{th}} \) 300 e

**Equivalent Noise Charge** 7.1 e threshold/noise > 10

**Channel-to-channel RMS** 10.2 e good threshold uniformity, no need for in-pixel tuning
Power to transmit matrix data to the periphery

- Assumptions: Matrix 2 cm x 2 cm, pitch 36.4 μm
- CMOS signals in the matrix (no noise issues, no need to use power consuming differential transmission)
- Analog Power < 75 mW/cm²
- Power for clock distribution (not used in the asynchronous readout)
  - Energy per 1 cm toggled line at 1.8 V = 3.2 pF/cm x (1.8 V)² = 10.4 pJ
  - 137 lines per cm (1 per double column) for 36.4 μm pixel pitch:
    137 x 10.4 pJ x 40 MHz = 57 mW/cm²
- Matrix readout

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pixel hit rate</th>
<th>Power/bit/cm² (H=2 cm)</th>
<th>Matrix readout power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>hit/BC/mm²</td>
<td>Mhit/mm²</td>
<td>mW/cm²</td>
</tr>
<tr>
<td>0</td>
<td>0.68</td>
<td>27.2</td>
<td>17.7</td>
</tr>
<tr>
<td>1</td>
<td>0.21</td>
<td>8.4</td>
<td>5.5</td>
</tr>
<tr>
<td>2</td>
<td>0.043</td>
<td>1.72</td>
<td>1.1</td>
</tr>
<tr>
<td>3</td>
<td>0.029</td>
<td>1.16</td>
<td>0.8</td>
</tr>
<tr>
<td>4</td>
<td>0.021</td>
<td>0.84</td>
<td>0.5</td>
</tr>
</tbody>
</table>
TowerJazz MALTA chip

ACTIVE MATRIX
(512x512 pixels)

pixel size 36.4x36.4 µm

LVDS drivers

CMOS I/O pads + power pads

DACs for analog biases

digital periphery

I/O pads
4 CMOS chips (MALTA) chained to one CMOS Quad Module

Use direct die-to-die wire-bonding to interconnect data IO between chips

All high speed chip signals routed in silicon (and not on flex to reduce flex mass and maintain signal integrity at high speeds)
Wafer-scale integration possible due to stitching

Flexible nature of thin Si (limits still to be tested with CMOS on top)

• Can we take advantage of this for lower mass detectors?
Conclusion and outlook - 1

- **Hybrid pixels** are currently the default in High Energy Physics

- Advantages of **Monolithic in High Energy Physics**:
  - Detector assembly and production cost.
    - Standard CMOS processing (larger wafer diameter, low cost per area)
    - No need for cost intensive fine pitch bump bonding
  - Better power-performance ratio (cabling and cooling material reduction)
  - Thin detectors \(O(50 \, \mu m \, Si)\) and high granularity (small cell sizes \(< 50 \, \mu m\) )

- **Monolithic pixels** adopted for the ALICE ITS upgrade
  - ALPIDE pixel chip in TowerJazz
    - Low sensor input capacitance allows for low power operation
    - The sensor is not fully depleted (moderate radiation tolerance and speed)
Conclusion and outlook - 2

- Development of a CMOS pixel sensor for potential use in the ATLAS pixel detector outer layers
  - 25 ns bunch crossing time and
  - tolerance to NIEL fluence $> 10^{15}$ (1 MeV neq/cm²)
  - => Full depletion for radiation tolerance and fast charge collection

- LFoundry HVCMOS: Electronics in the collection electrode.
  - LF-Monopix is functional. Power penalty due to large sensor capacitance (400 fF) and robust design to avoid cross talk.

- TowerJazz process modification for full depletion combined with low C
  - Promising sensor characterization results (Investigator)
  - Design of two large-scale demonstrators
    - Low power front-end ($< 25$ ns, $< 1$ µW)
      - MALTA, asynchronous readout
      - TJ-Monopix, synchronous readout
Acknowledgements

- Walter Snoeys
- CERN microelectronics section
- ALICE collaboration
- ATLAS collaboration
- STREAM