Strip-line Kickers and Fast Pulsers R&D at HEPS

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HEPS/HEPS-TF Injection System

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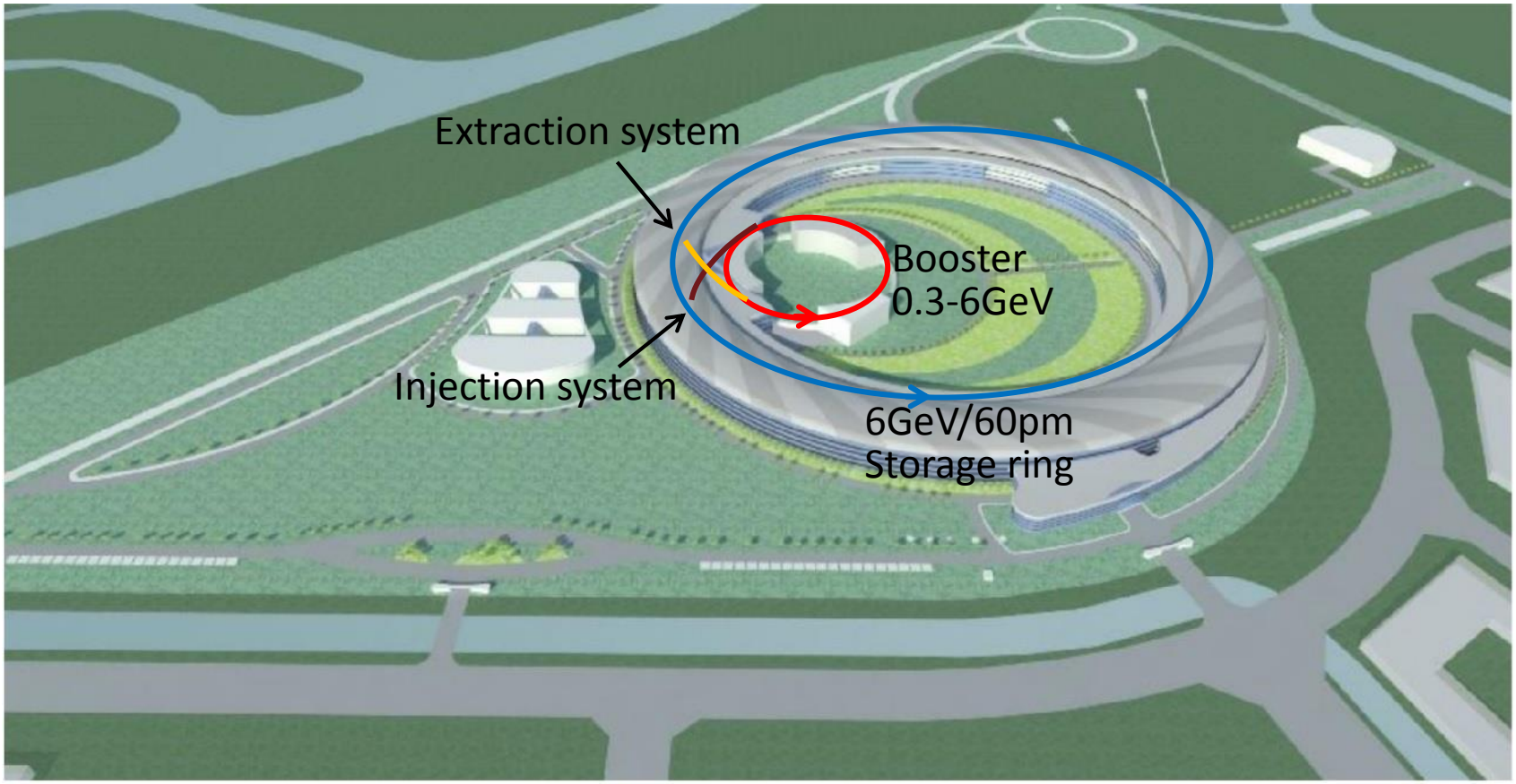
Outline

HEPS Injection and Injection Systems

High Energy Photon Source(HEPS)

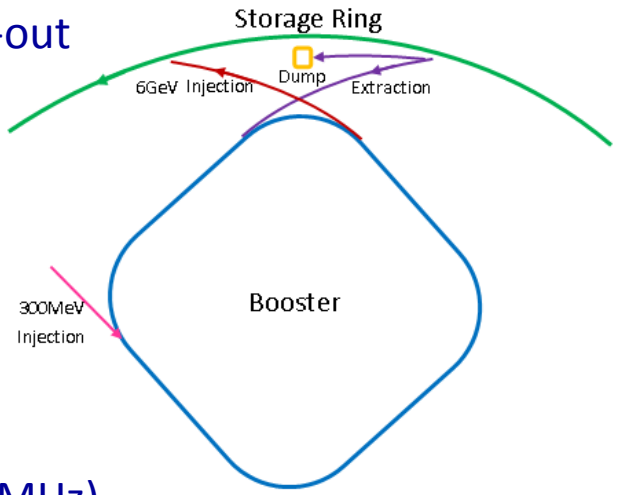


HEPS storage ring is a typical MBA LER, for it's baseline lattice design, the Dynamic Aperture(DA) is not large enough for off-axial injection. Only on-axial injection schemes are possible.

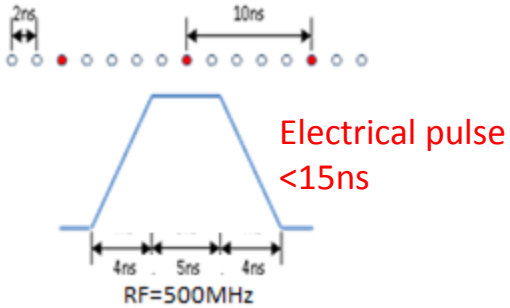
Challenges for HEPS Injection System

- The baseline injection scheme for HEPS : On-axial swap-out injection
  - Dumping mode
  - Recycling mode (for high bunch charge mode)

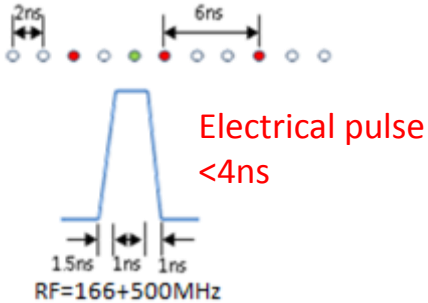
  (booster acts as an accumulating ring)



- The other potential scheme : On-axial longitudinal accumulating injection by 3rd harmonic RF system(166/500MHz)
- For both on-axial injection system, the biggest challenges : Super fast kicker and pulser.



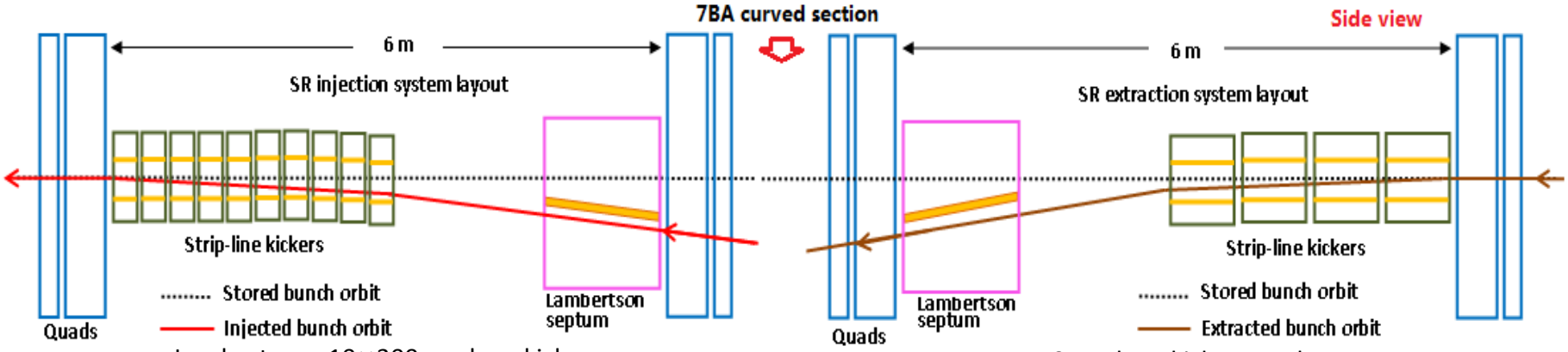
swap-out injection mode



longitudinal injection mode

Injection & Extraction Section Layout

- **Compatibility of both on-axial injection schemes**



Lambertson +10×300mm long kicker

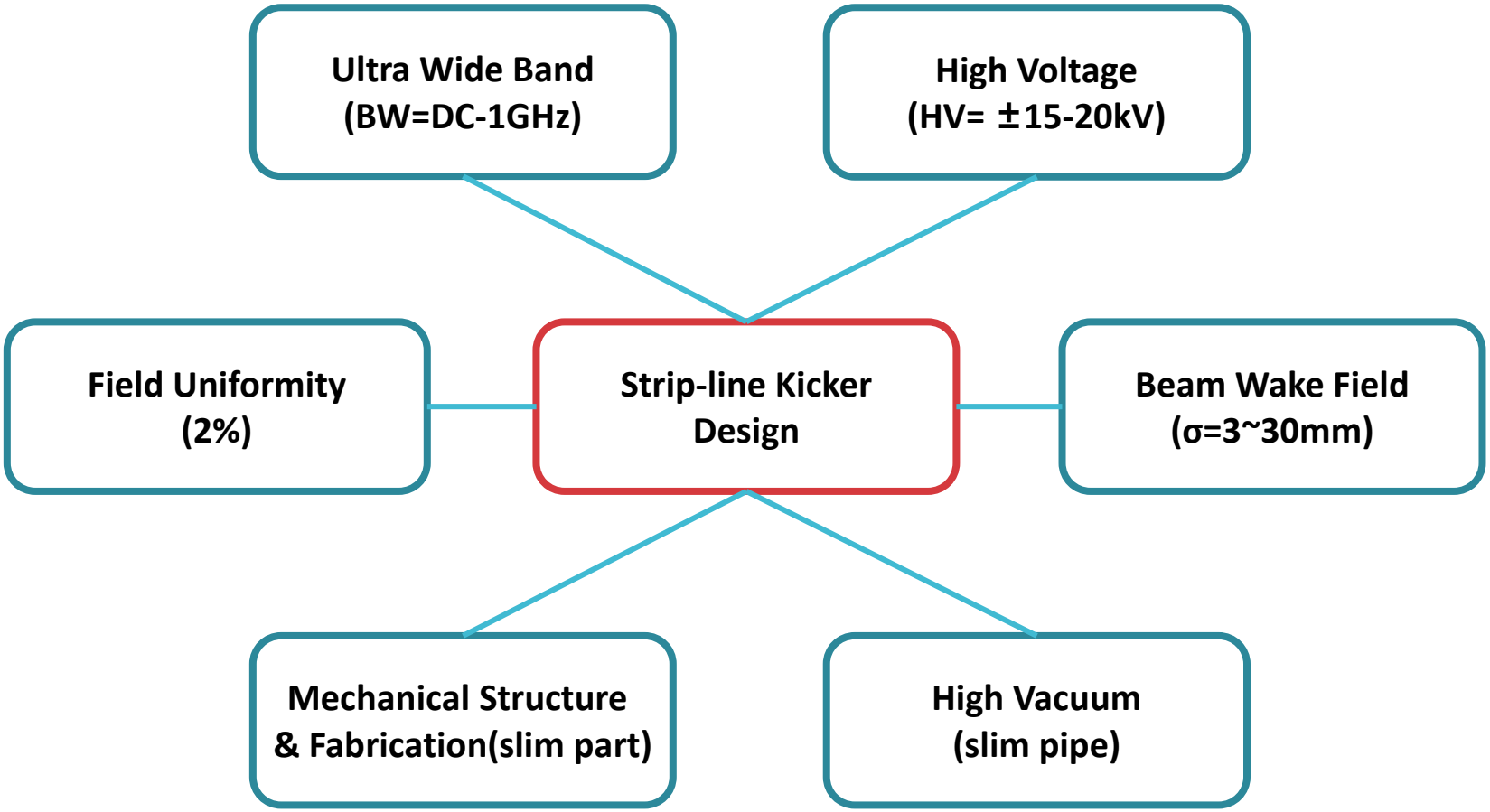
4×750mm long kicker+Lambertson

Main design Specification	Unit	injection	extraction
Straight section length	m	6	6
Kick angle	mrad	3	3
Kick direction	-	Vertical	Vertical
Length of Strip-line kicker electrode	mm	300	**750**
Gap of Strip-line kicker electrode	mm	10	10
Quantity of Strip-line kicker	-	10	4
Longitudinal space between strip-line kicker electrode	mm	**<30**	<75
Amplitude of electrical pulse	kV	±15	±15
Rise time of electrical pulse（10%-90%）	ns	**1.5**	4
Flat top of electrical pulse (90%)	ns	**1**	5
Fall time of electrical pulse(90%-10%）	ns	**1.5**	4

Progress of R&D on Strip-line Kicker

Strip-line Kicker Design Consideration

- Injection strip-line kicker is a kind of encounter travelling wave kicker



Strip-line Kicker Design Reference

- APS-U has been successful in Strip-line kicker design and its scheme looks best for us[1][2][3]
- Pros of APS-U type Strip-line kicker
  - "D" shaped blades are used to improve field-uniformity in the good field region.
  - An ellipse outer body with vanes geometry is adopted to ease common-mode impedance-matching
  - Tapered end sections for matching impedance to the feed-throughs.

PRELIMINARY TEST RESULTS OF A PROTOTYPE FAST KICKER FOR APS MBA UPGRADE*

Figure 5: The kicker installed in the BTX beamline.

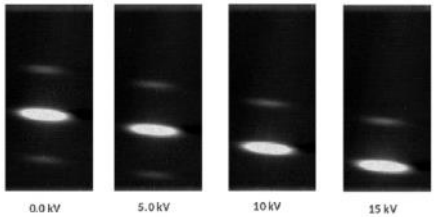


Figure 10: Beam spot movement when kicker amplitude varies from 0 to 15kV.

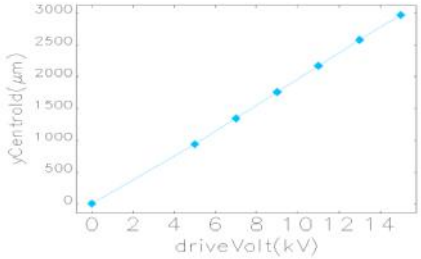
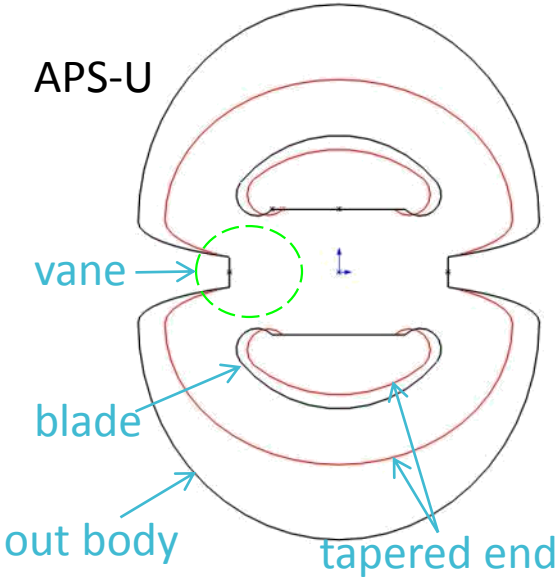
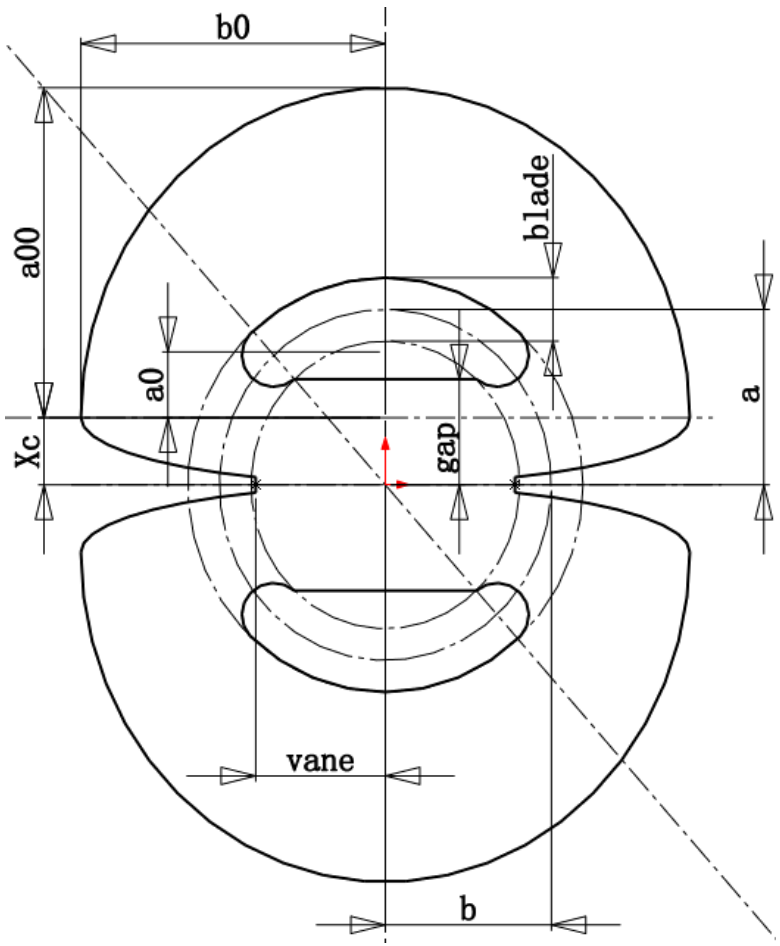


Figure 11: Measured y-centroid position vs kicker amplitude.



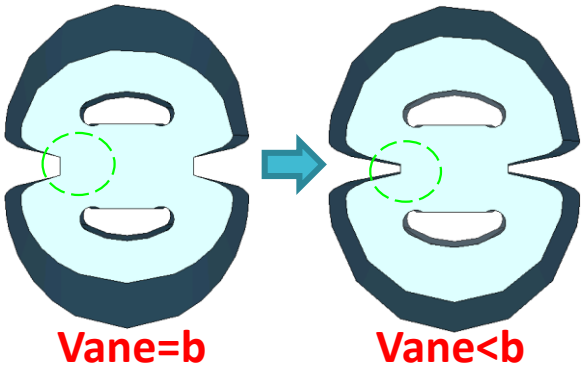
2-D Geometry Model for Optimization

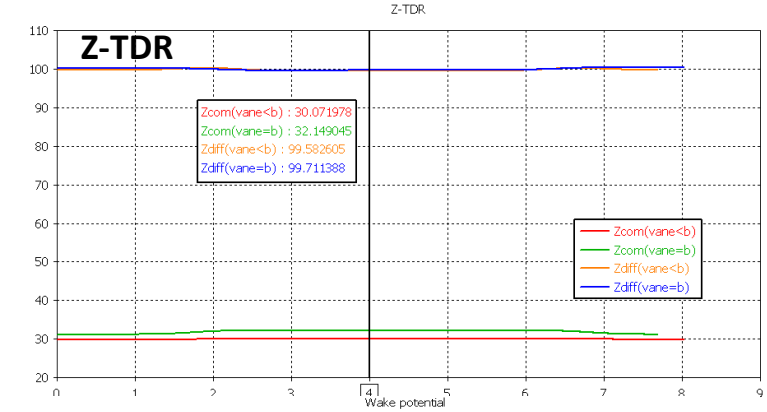


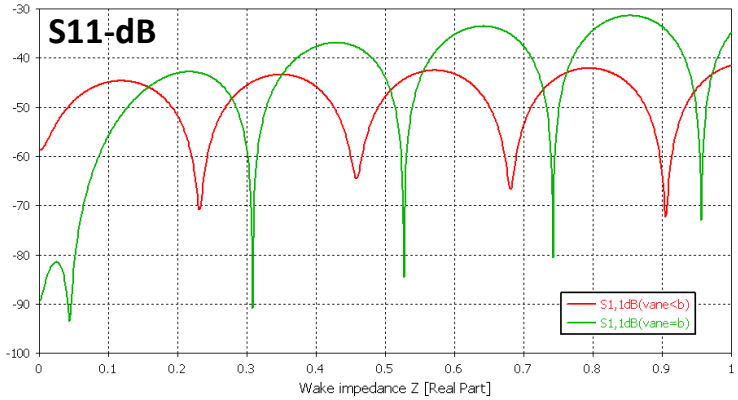
- **The strip-line blades are decided by:**
  - **a, b - axes of the center ellipse**
  - **gap=5mm – ½ distance between blades**
  - **blade=3mm – thickness of blades**
- **The outer body half shell consists of 2 half ellipses that defined by:**
  - **Center half: Xc, a0, b0**
  - **Outer half: Xc, a00, b0**
- **New parameter:**
  - **vane (>=<b)- ½ distance between Vanes**

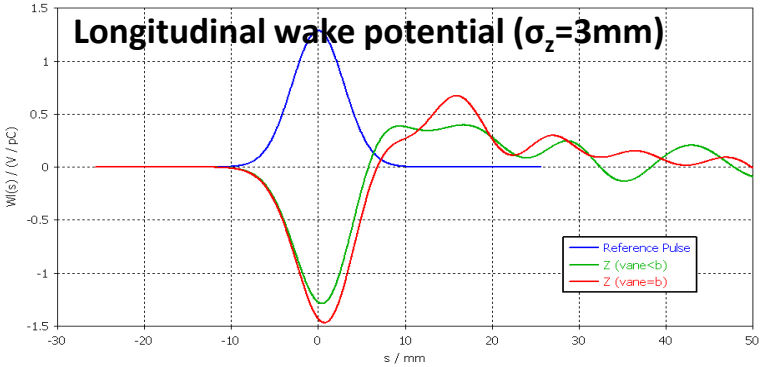
Strip-line Kicker Design Improvement 1

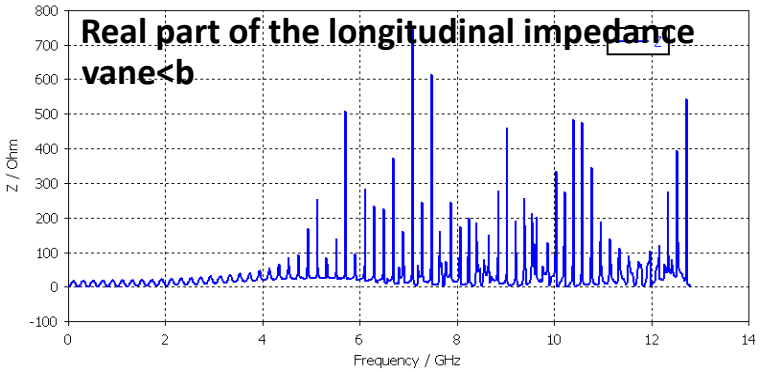
- Based on APS-U's design, further optimize was done
  - Extend the vanes to decouple 2 strip-lines, then achieve:
    - lower impedance mismatching in common-mode (<60.5 Ω),
    - lower reflection(S11<-40db),
    - lower beam impedance (loss factor=0.893V/pC, ↓15%)





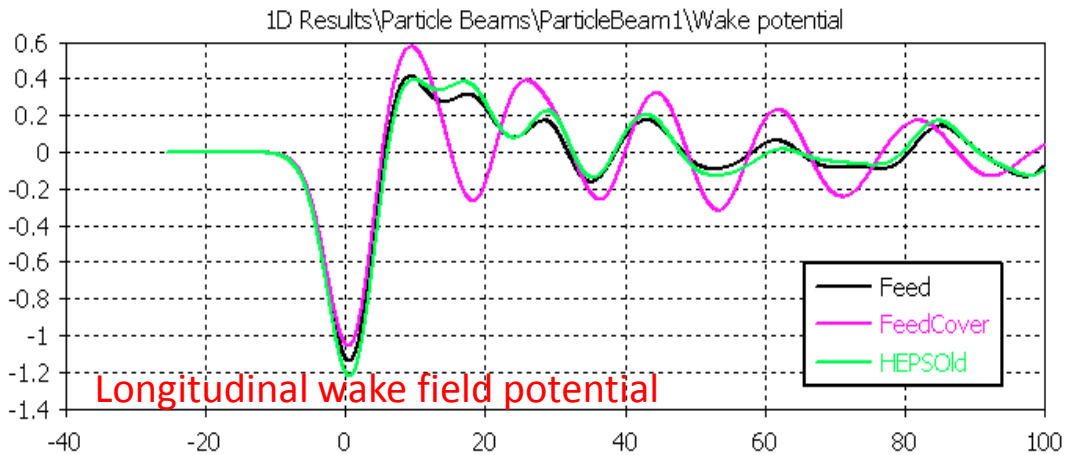


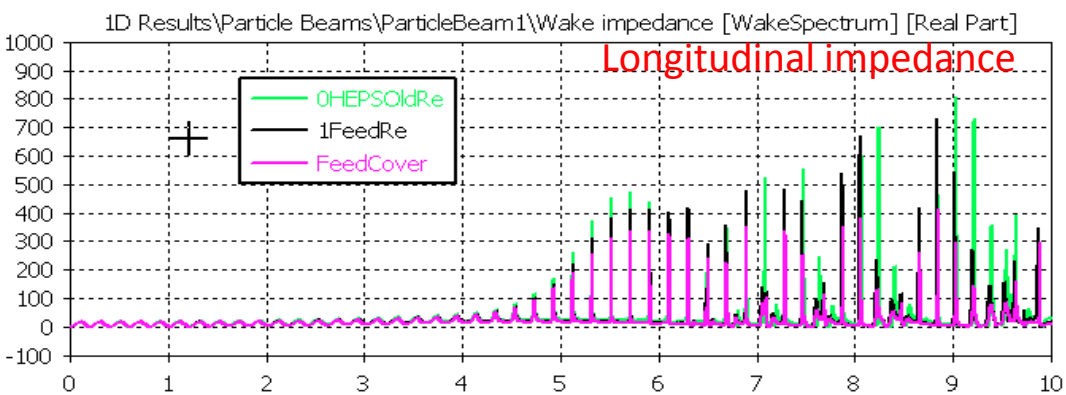




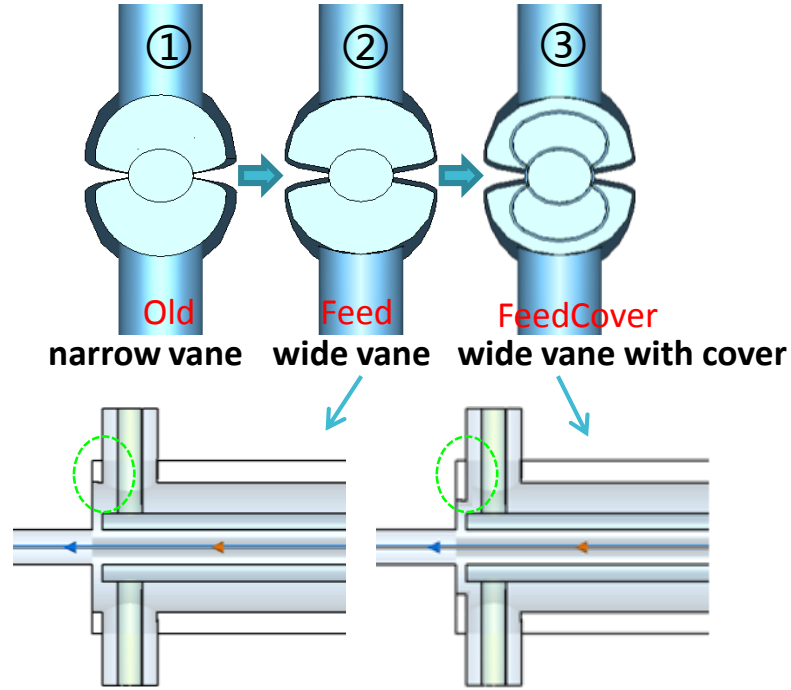
Strip-line Kicker Design Improvement 2

- Improve the taper part to further decrease beam impedance; Power loss decrease 16%.





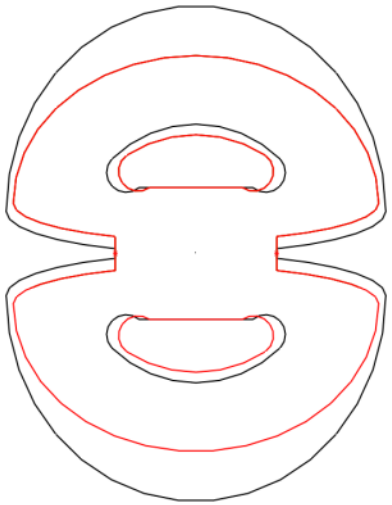
σ=3mm Gaussian beam



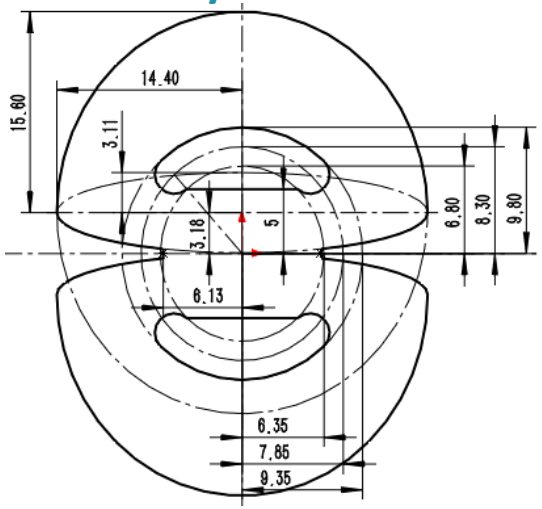
	Loss factor [V/pC]	Power loss [W] N_b=648, I_0=200mA	Power loss [W] N_b=60, I_0=200mA
①	0.855	228	2463
②	0.788	210	2270
③	0.716	191	2063

Power loss: $P=k_l I_b^2 n_b/f_{rev}$=

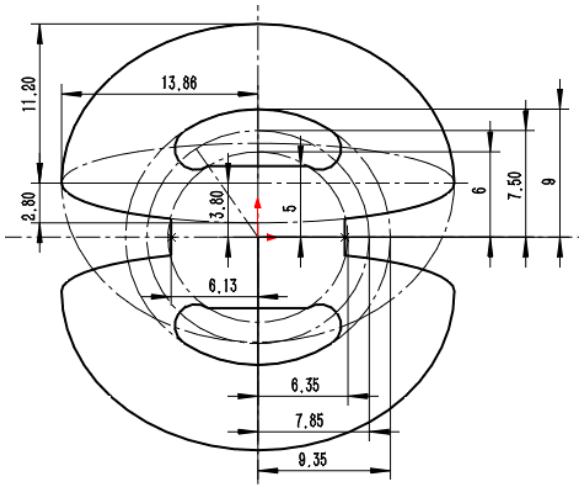
2-D Strip-line Optimization Result



Main body cross section



Transition part at the end

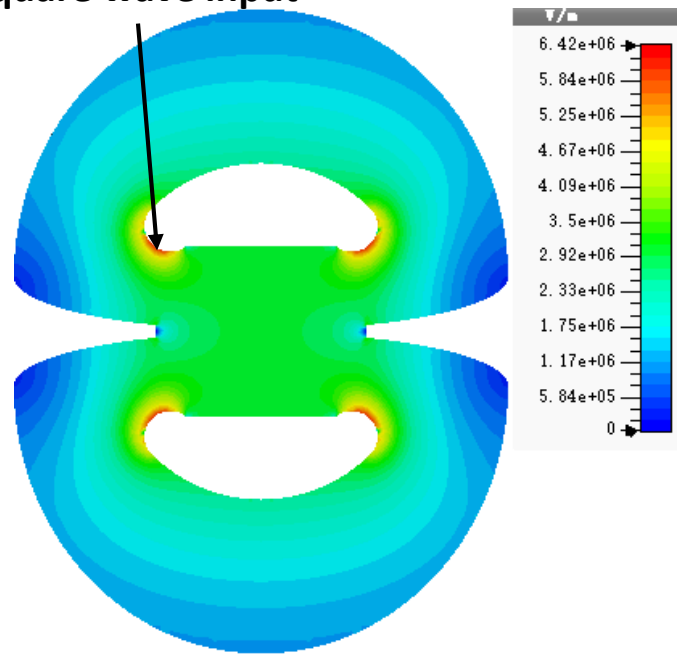


Parameters	Main body(black)	Transition part(red)
Zodd / Ω	49.81	50.00
Zeven / Ω	60.39	58.23
Emax / (MV/m)	6.42	6.63
Eave-gap / (MV/m)	2.99	3.00
ΔE/E gap / (%)	1.70	5.76
Y (±1mm) / (%)	0.20	0.63
Y (±5mm) / (%)	1.70	5.76
X (±2.3mm) / (%)	1.45	4.39

Difference-mode Electric field

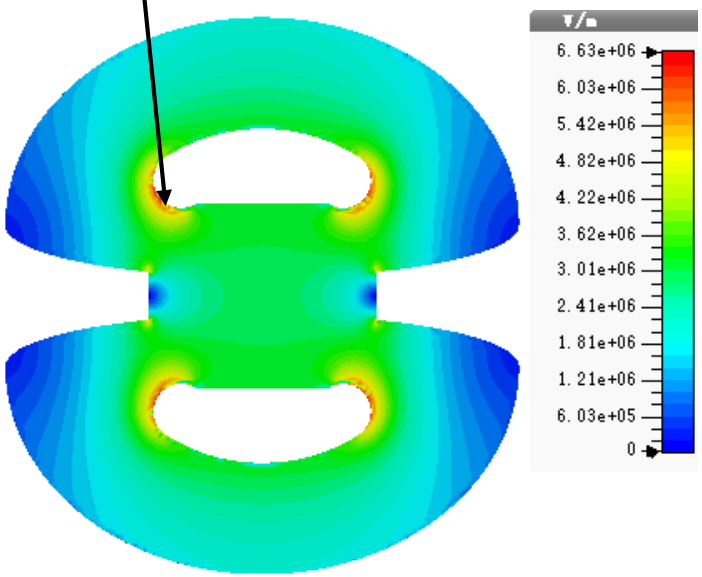
1mm slice

E = 6.42 MV/m
for ±15 kV
square wave input



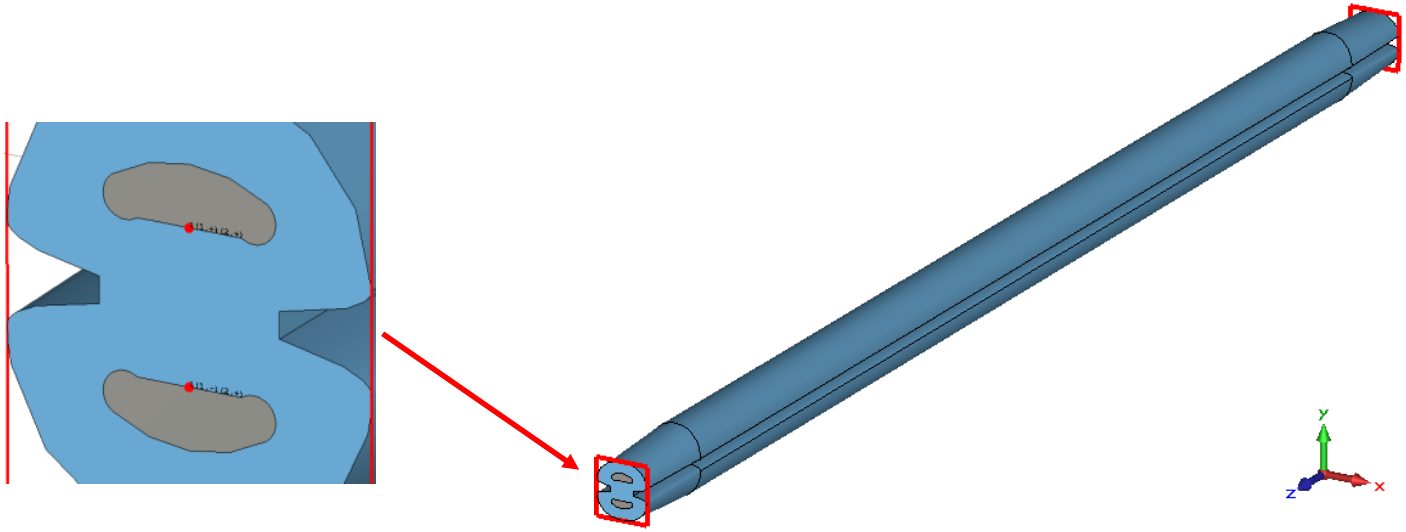
Main body

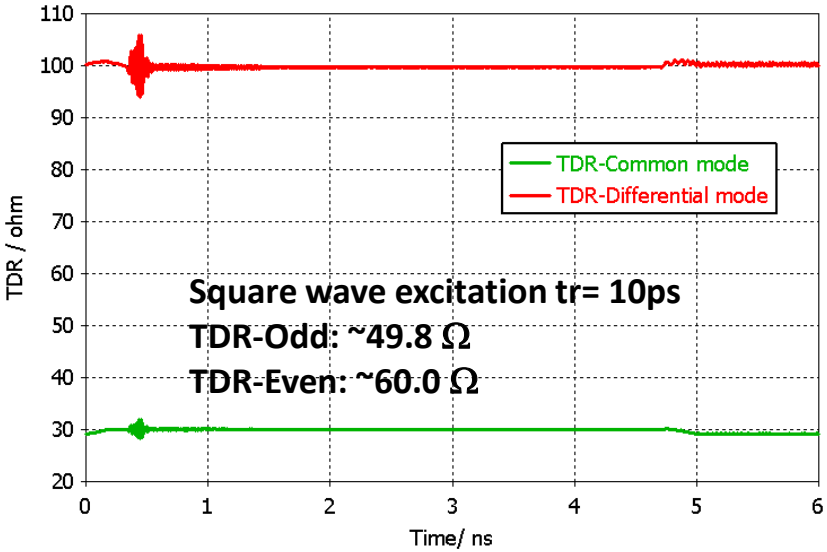
E = 6.63 MV/m
for ±15 kV
square wave input

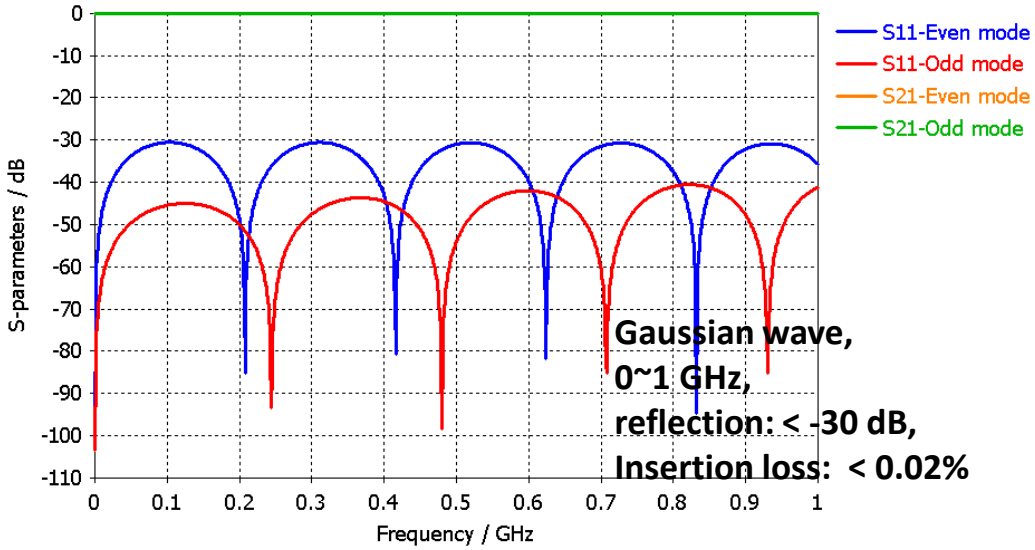


Transition part

3-D Model and RF Parameters

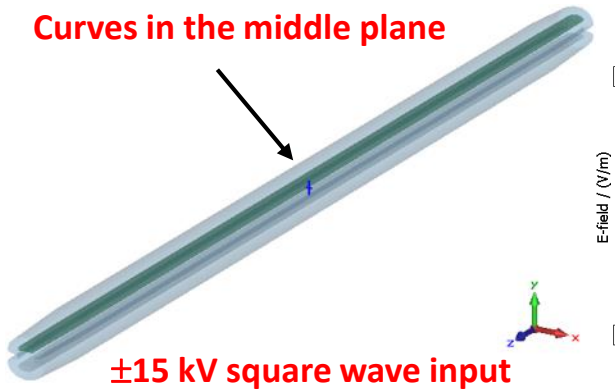


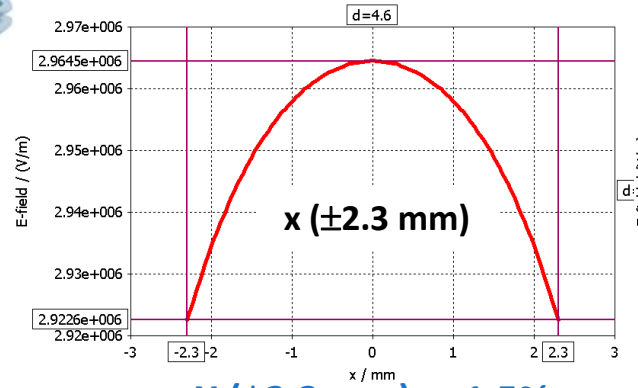




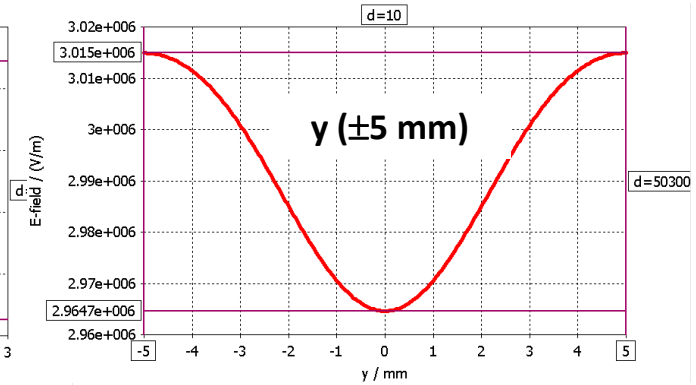
E-field uniformity

- **The field uniformity in the middle plane**



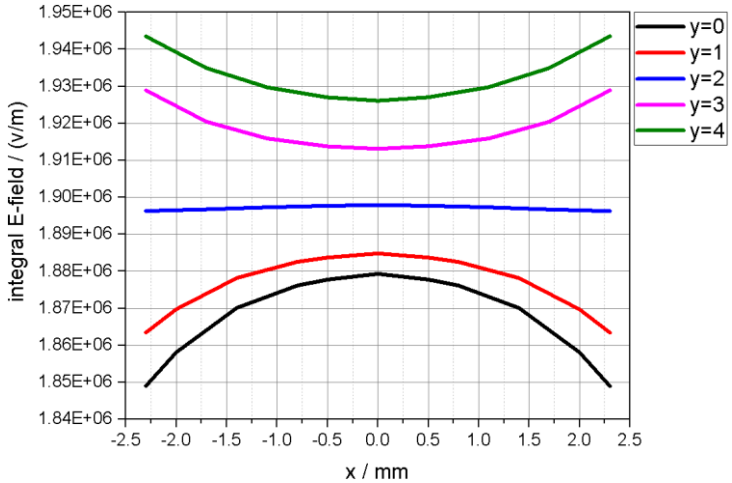


X (±2.3 mm) : <1.5%

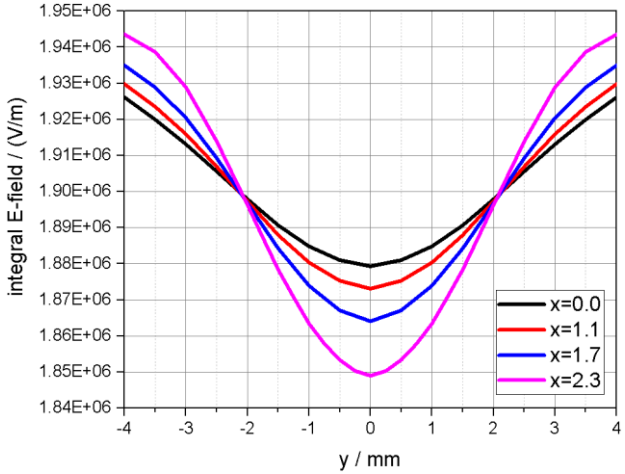


Y (±5 mm) : <1.7%

- **Integral E-field Along z**

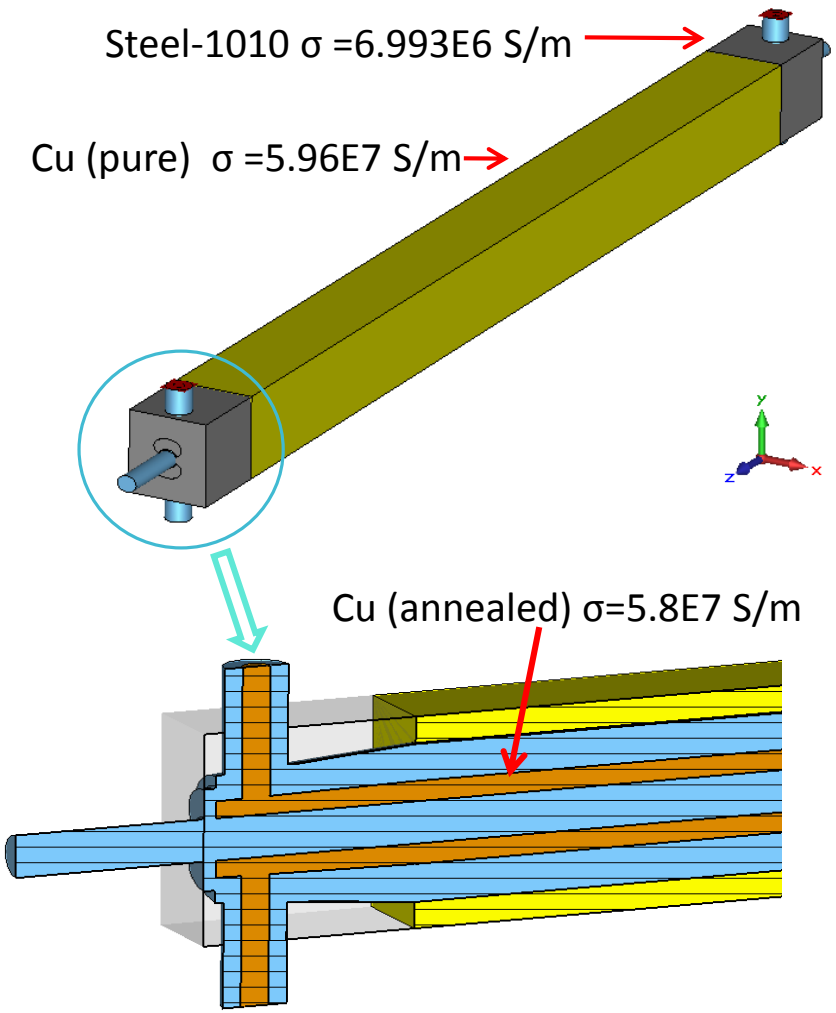


x (-2.3~2.3 mm) at y=0, 1, 2, 3, 4



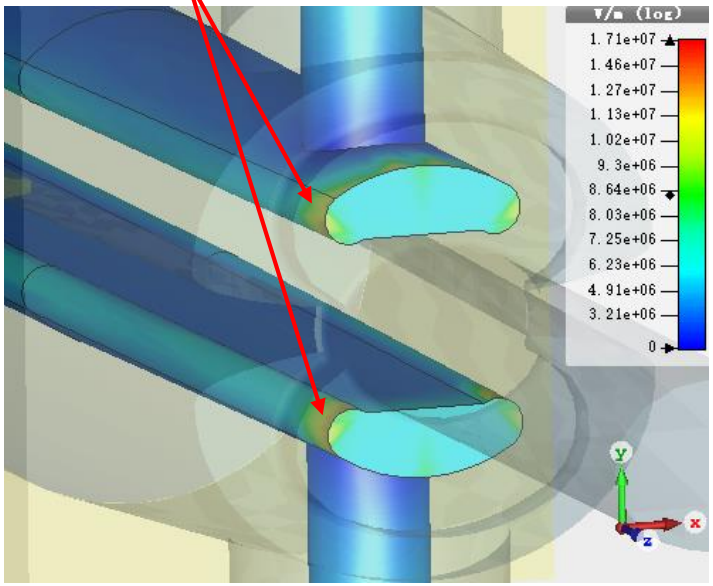
y (-4~4 mm) at x=0, 1.1, 1.7, 2.3

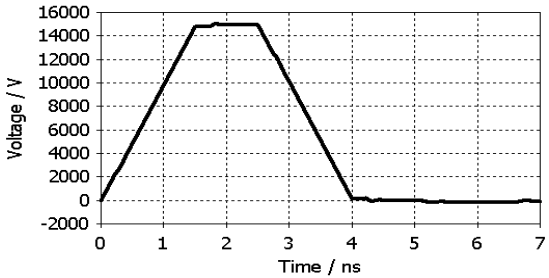
750mm Strip-line with Perfect Feedthrough Model



Coaxial Feedthrough(air line,50Ω):
Do=16 mm, Di=7 mm

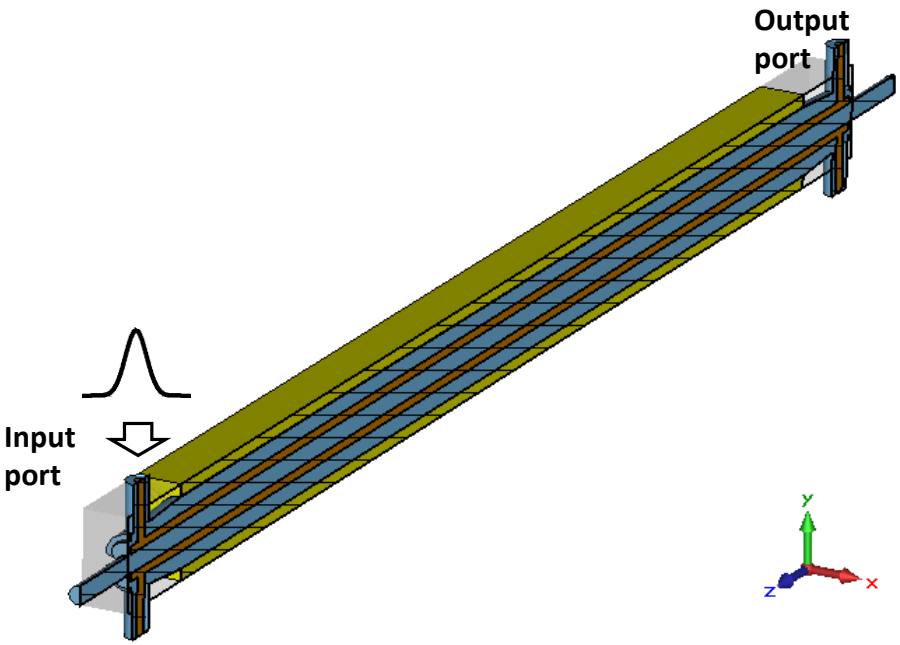
E = 17.1 MV/m for 15 kV square wave input

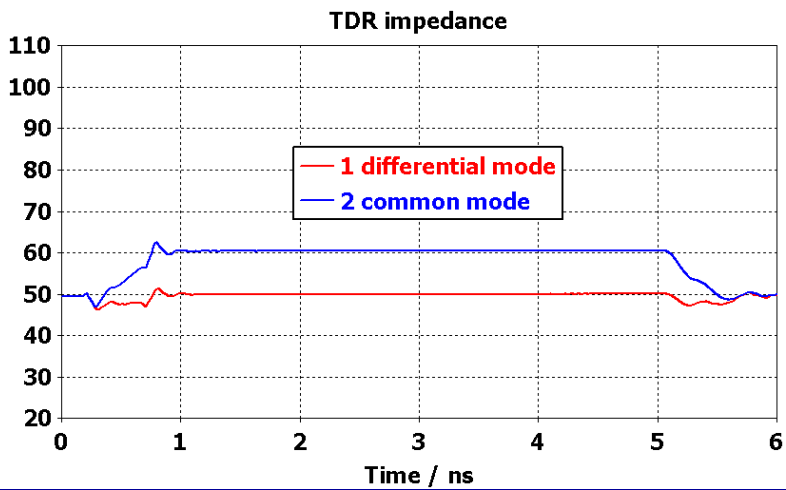


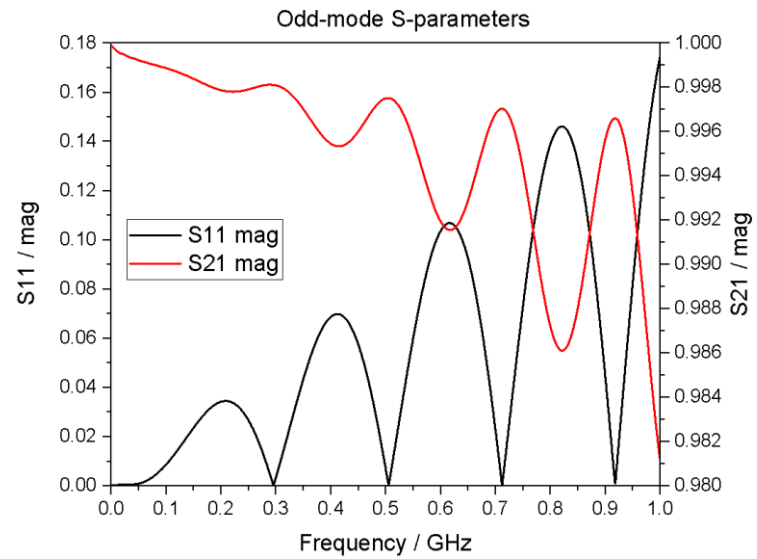


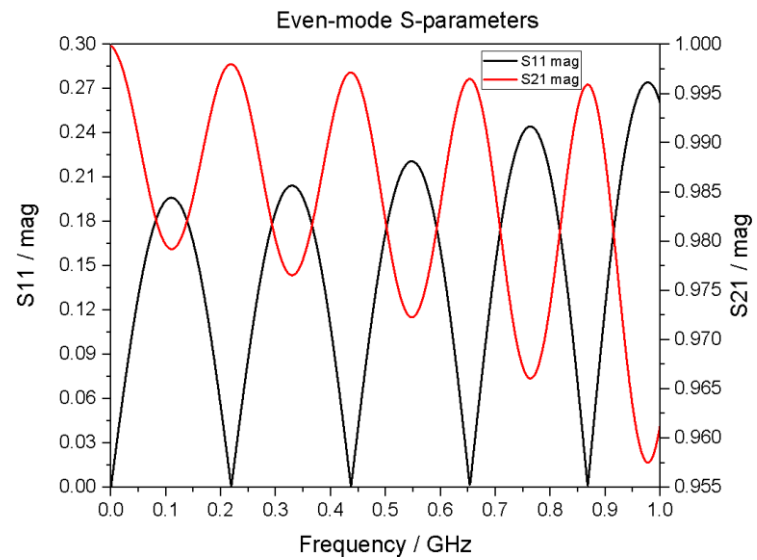
Pulse setting: $t_r+t_{top}+t_f=1.5+1+1.5=4$ns.
Voltage at t_{top} is 15 kV

RF Parameters

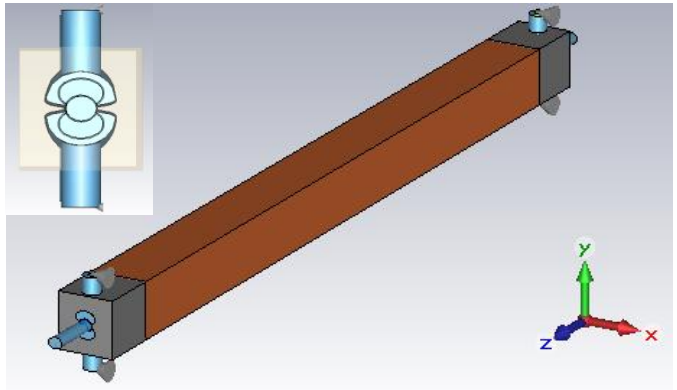








Beam Impedance and Wake



kicker model (wide vane with cover)

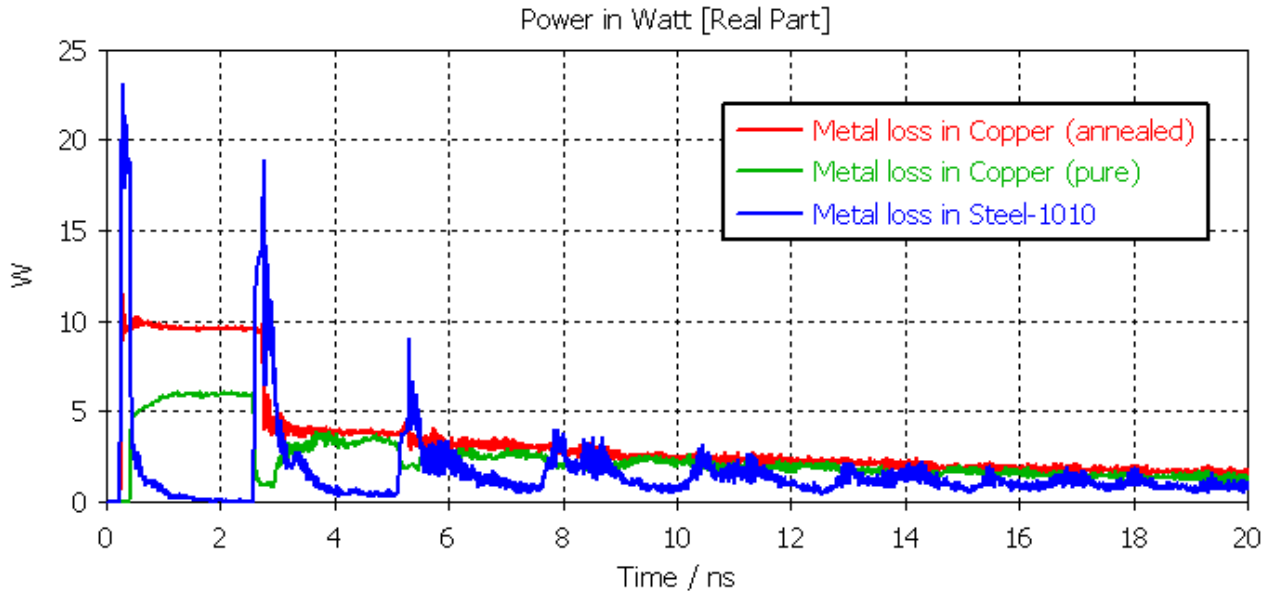
With material setting:
Blade: Cu (annealed) cond=5.8E7 [S/m]
Box_middle: Cu (pure) cond=5.96E7 [S/m]
Box_side:Steel-1010 cond=6.993E6 [S/m]

- The worst case: longitudinal injection period in high charge mode(σ_z=3mm,14.4nc)
- the power loss at each kicker is 2.1kW ;
- In longitudinal injection mode, If the injection time is 1/600 of running time , and the beam length is 3cm in normal operation, the average power loss should be decreased to 81W.

$$P_{ave} = \frac{P_{loss,1} * \Delta t_1 + P_{loss,2} * \Delta t_2}{\Delta t_1 + \Delta t_2}$$

	Loss factor [V/pC]	Power loss [W] N_b=648,I_0=200mA (1.334nc)	Power loss [W] N_b=60, I_0=200mA (14.4nc)	$\lvert Z_{\lvert\lvert}/n \rvert_{eff}$ [mΩ]	k_y [V/pC/m]
Sigz=3mm	0.716	191	2063	-0.03	313.5
Sigz=3cm	0.027	7.2	78	1.05	120.6
Sigz=3mm+3cm	-	7.5	81.3	-	-

Beam power loss dissipation

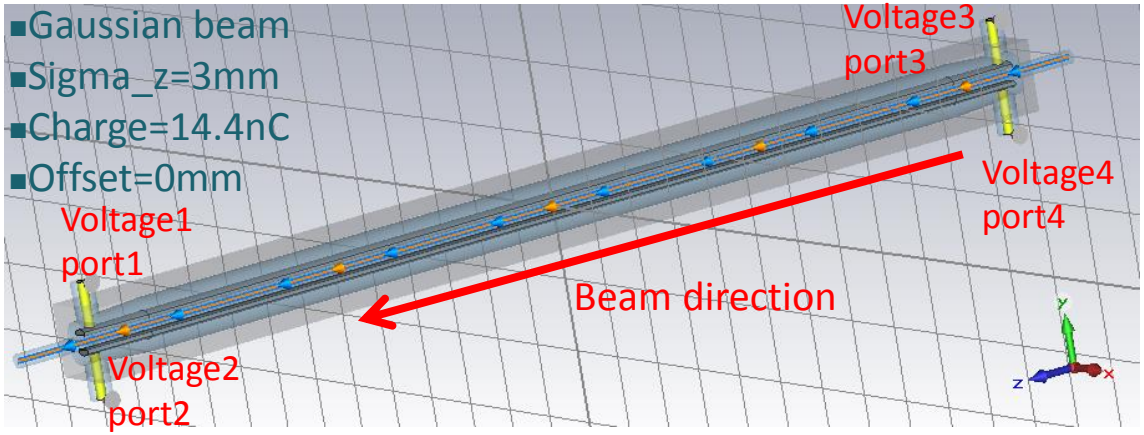


Beam parameters：
σ_z=3mm ,
n_b=648,
Charge=1.334nC
y_offset=0

Power loss [W]	2 Blades (Cu_annealed)	Box_middle (Cu_pure)	Box_sides (Steel-1010)	Port1/Port2	Port3/Port4	Sum	From loss factor
Sigz=3mm, nb=60	233.3	171.4	117.1	313.2/313.2	419.0/419.0	1986.2	2063
Sigz=3mm, nb=648	21.6	15.9	10.8	29.0/28.9	38.8/38.8	183.8	191

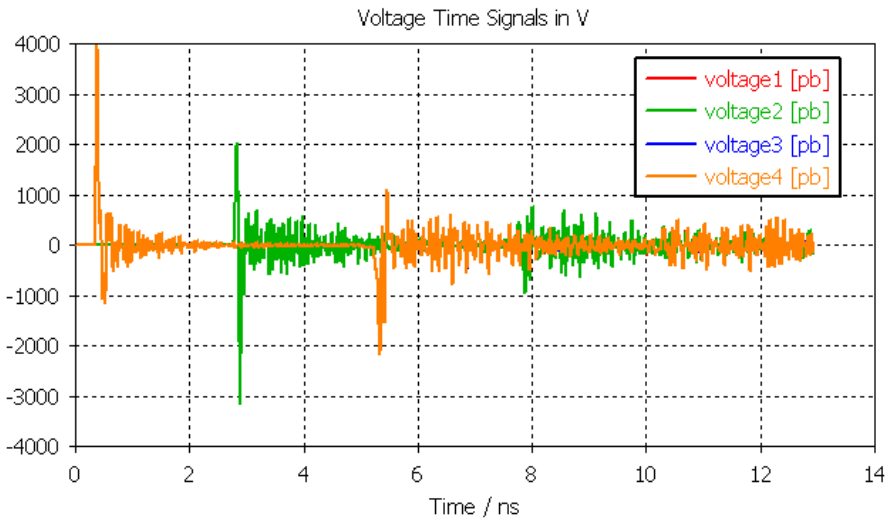
- In high charge mode, beam power loss dissipation is 233.3W at blades ，288.5W at outer body, 321.6W at upstream port and 419.3W at downstream port.
- The sum of power loss dissipation is little less than the result from loss factor, because some power flows out from beam pipes at both ends

Induced Voltage and E-field excited by Beam

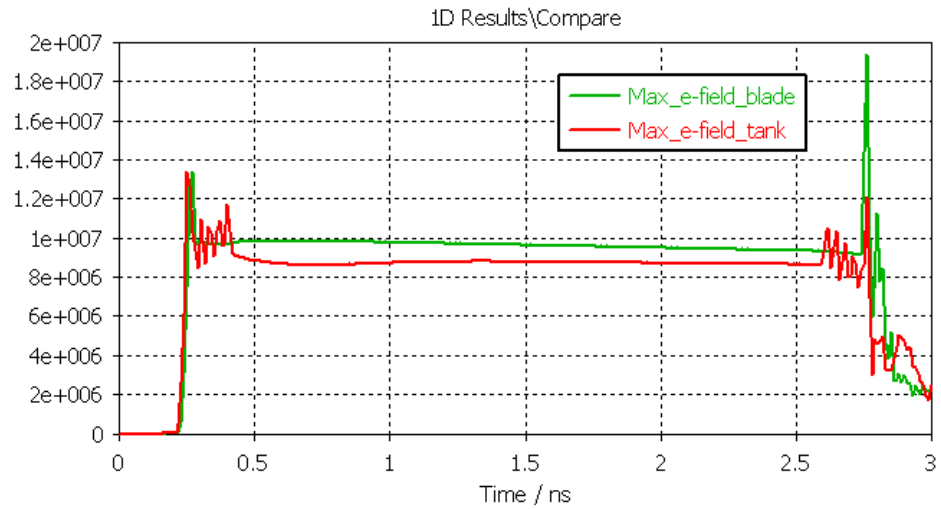


In worst case:

- Max. beam induced voltage on Feedthrough<3990 V
- Peak E field on the copper blade is 19.4 MV/m
- Peak E field on the vacuum tank is 13.4 MV/m



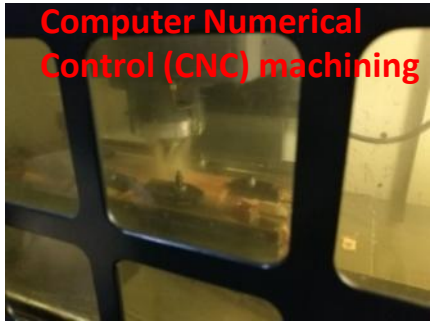
Induced Voltage on Feedthroughs



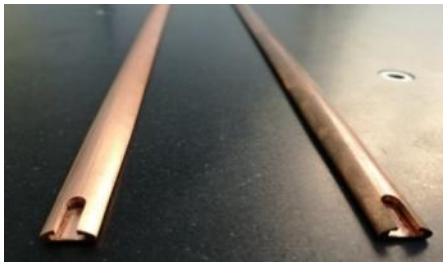
Max electric field on face

First PoP Kicker Fabrication

- PoP kicker is to prove the fabrication technique and design simulation



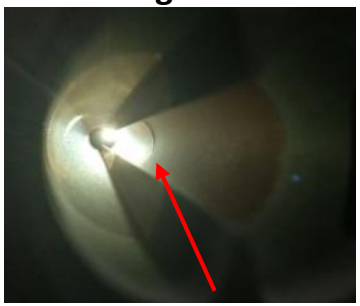
Blade machining



Out-body machining

Out-body Welding

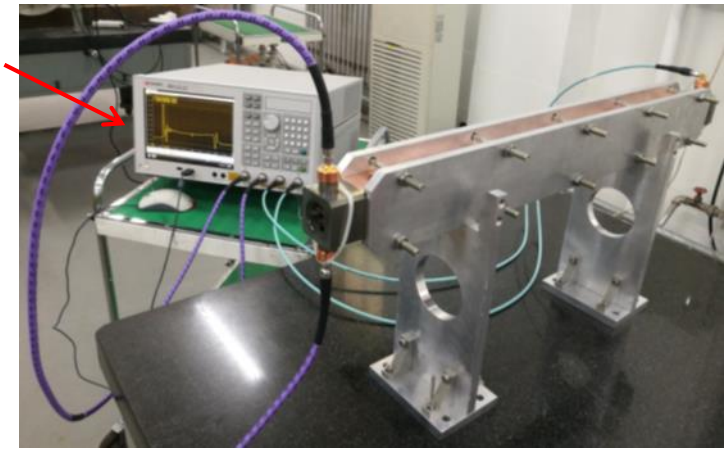
Assembled vacuum tank of kicker before brazing

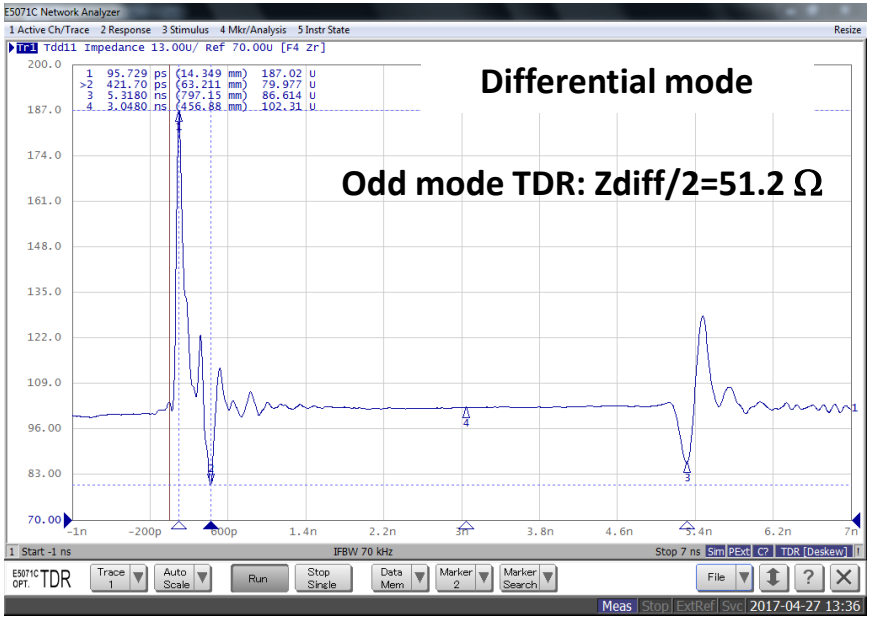


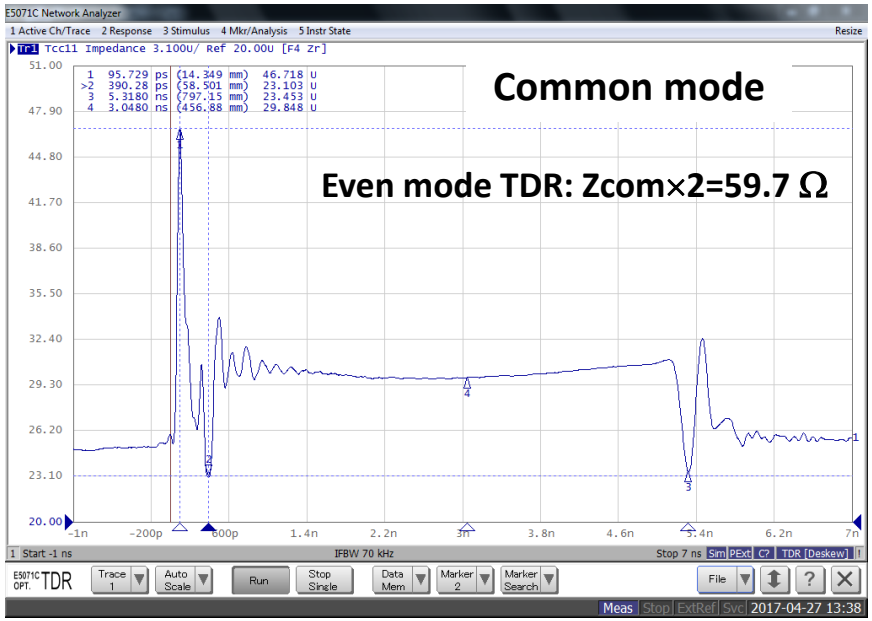
Solder wire Copper main part Steel transition part Welding Seam

PoP Kicker assembly test

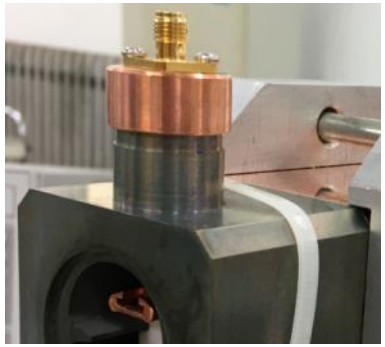
Network Analyzer:
Keysight E5071C

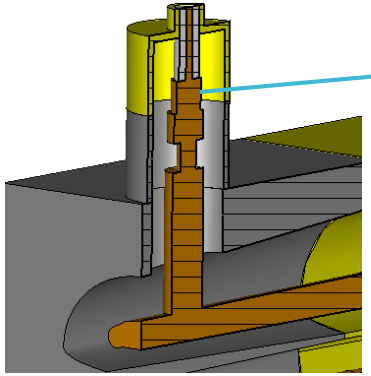




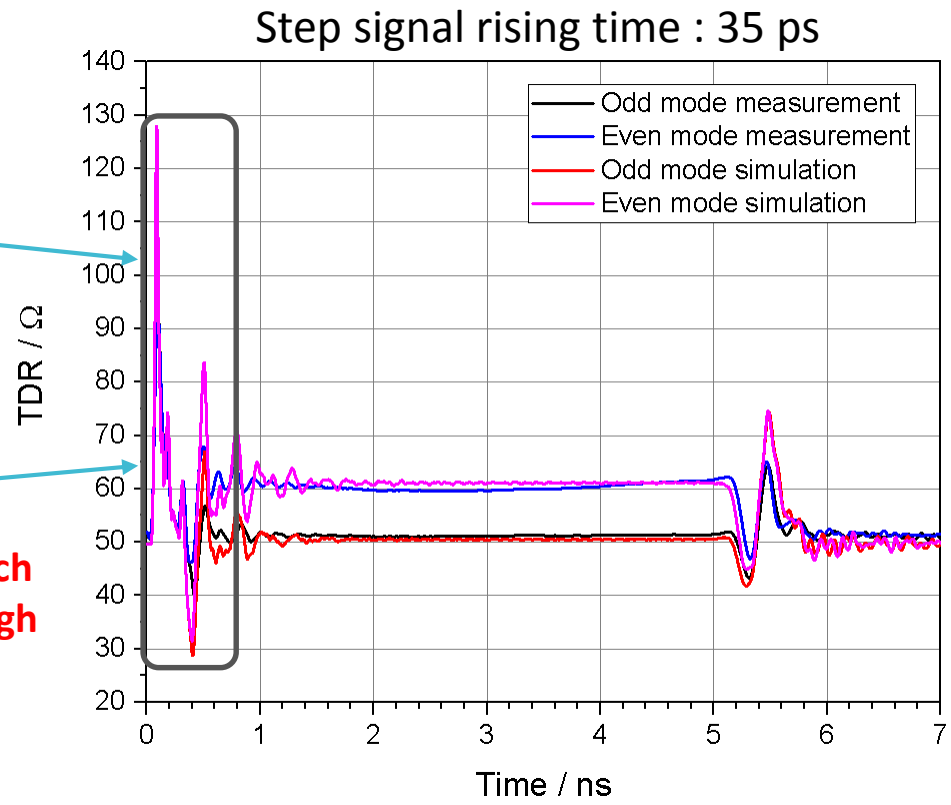


PoP Kicker TDR Test Results





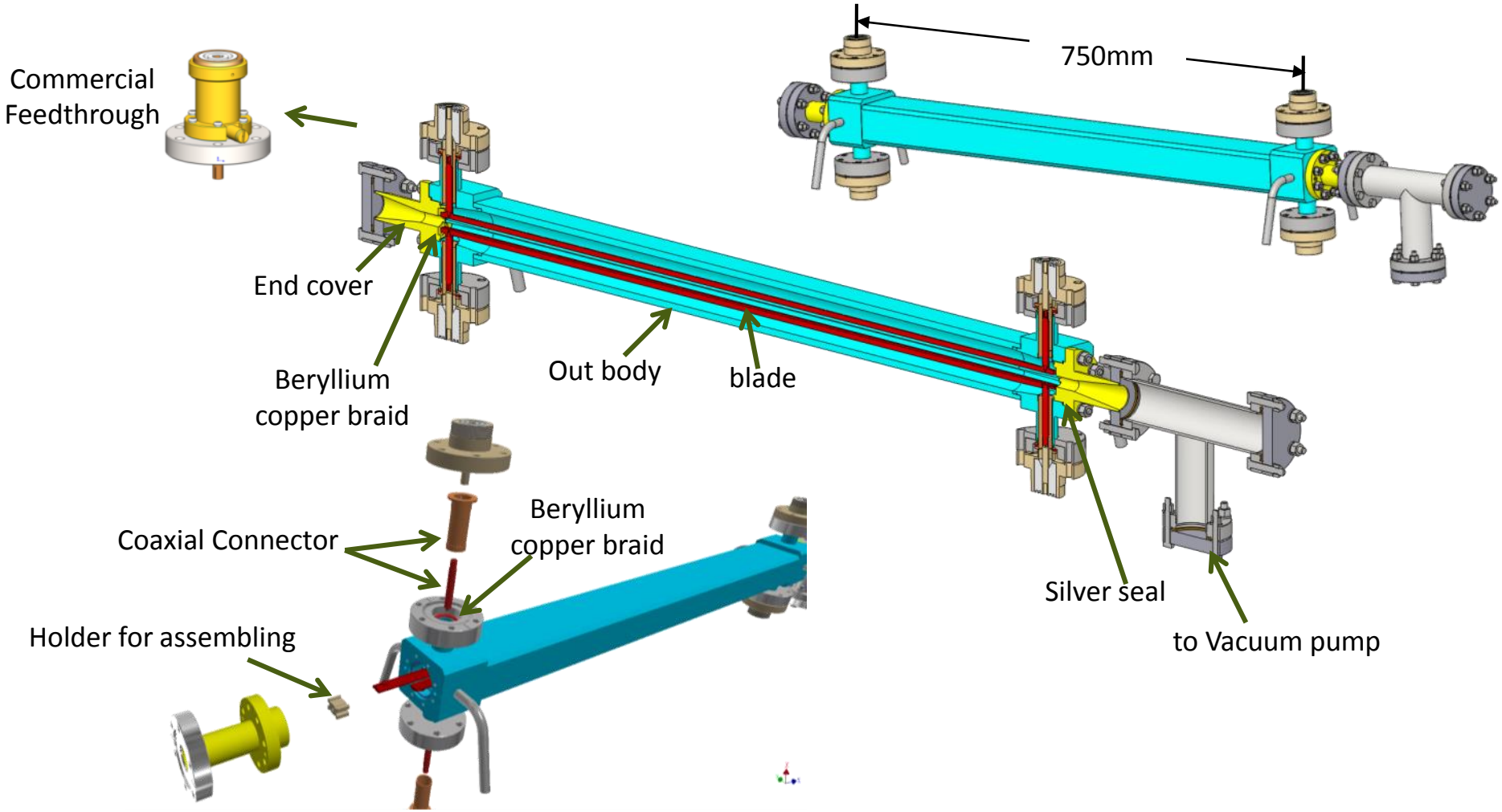
Very big mismatch in the feedthrough part.



- The measurement and simulation results agreed well

750mm-long Strip-line Kicker prototype

- Final prototype kicker design is done, and it is being fabricated in the factory

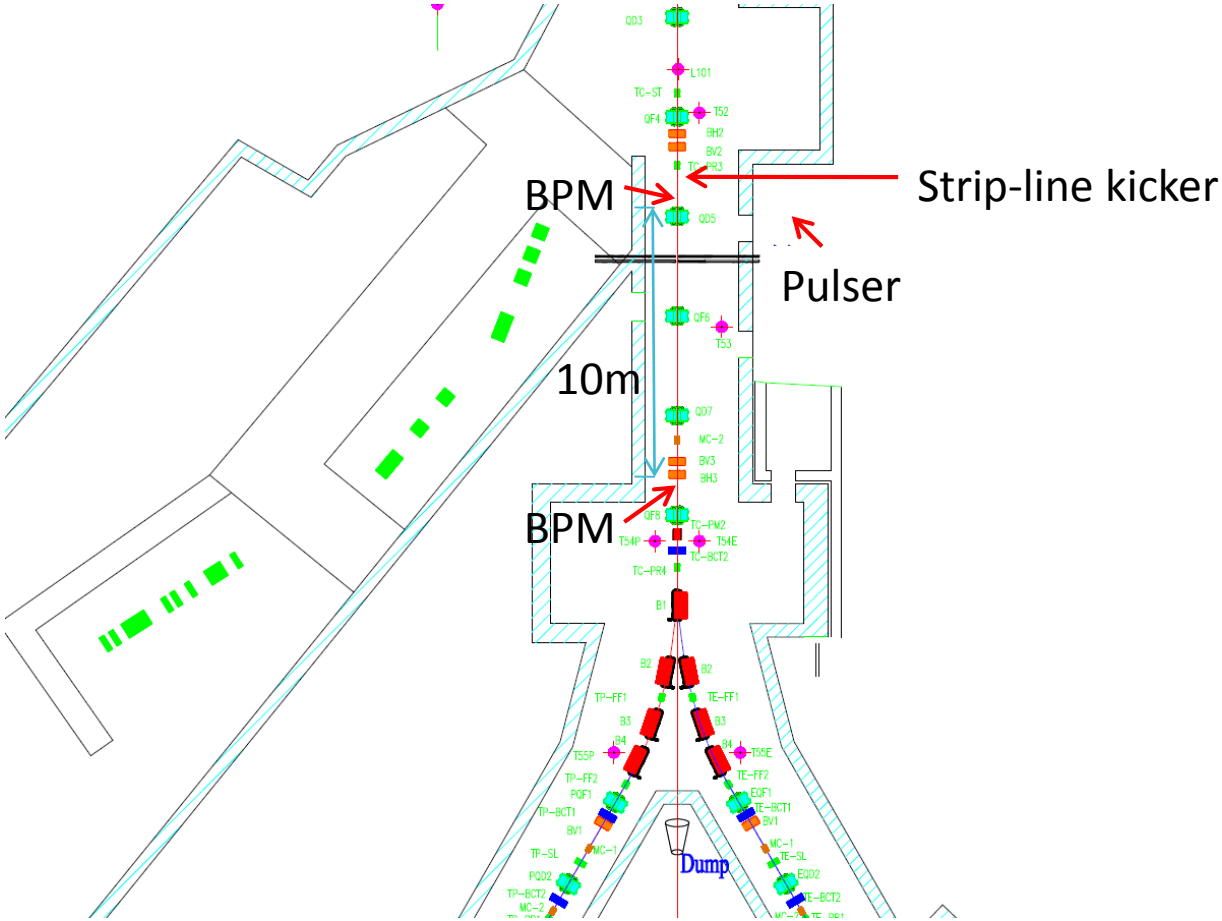


Strip-line Blades and Out body

Vacuum out water leakage issue is to be solved

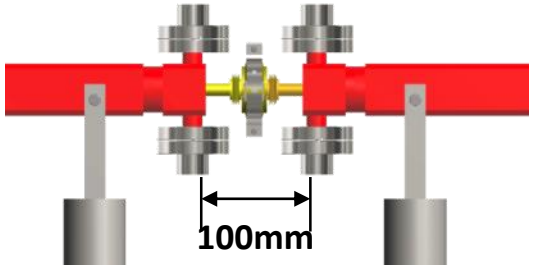
Next plans

- Cold Test after assembling next month: TDR, HV test
- Beam test at BEPCII Linac next year



300mm-long Compact Kicker Consideration

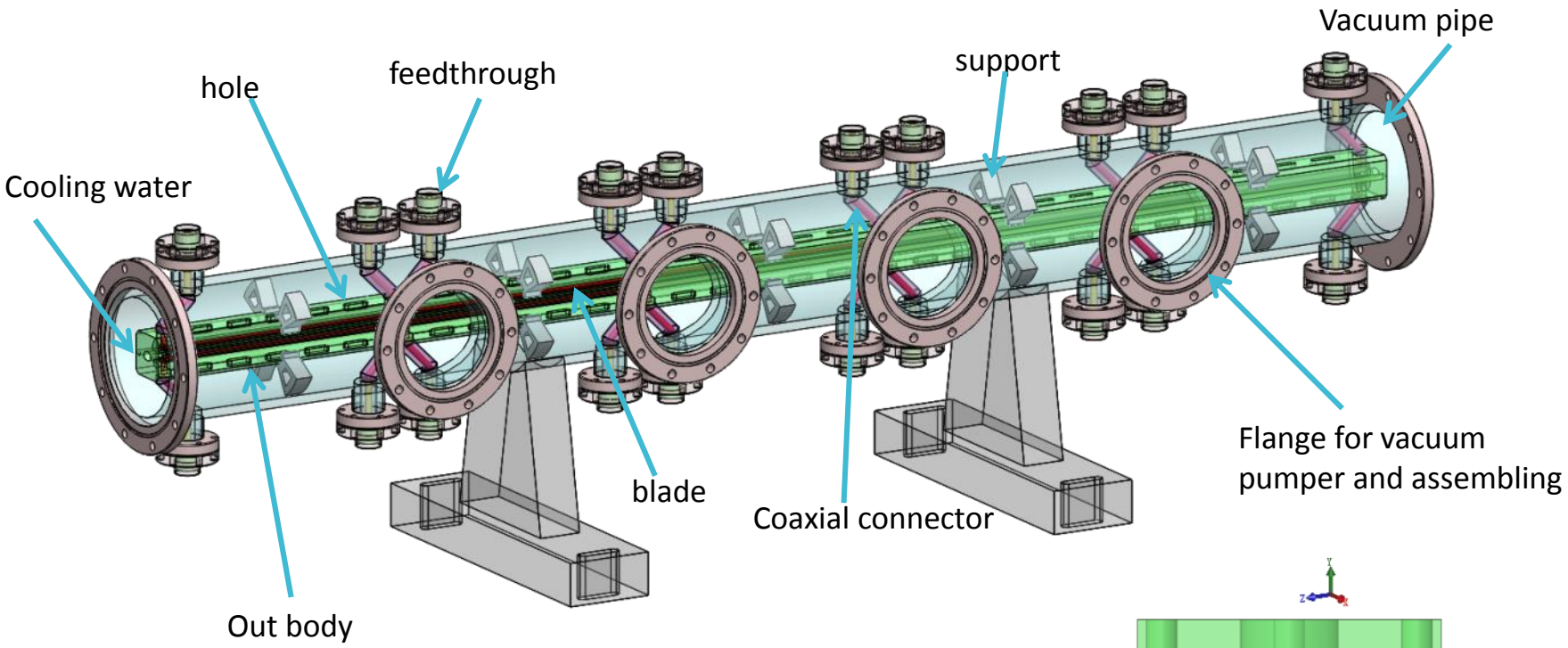
- For longitudinal injection, we need 10 sets of shorter strip-line kickers (300mm-long)
- In 750mm-long kicker design, the gap between adjacent kickers is 100mm.The same structure is not fit for 300mm-long kicker because 10 sets of shorter kickers could not install in limited space(3.3m).



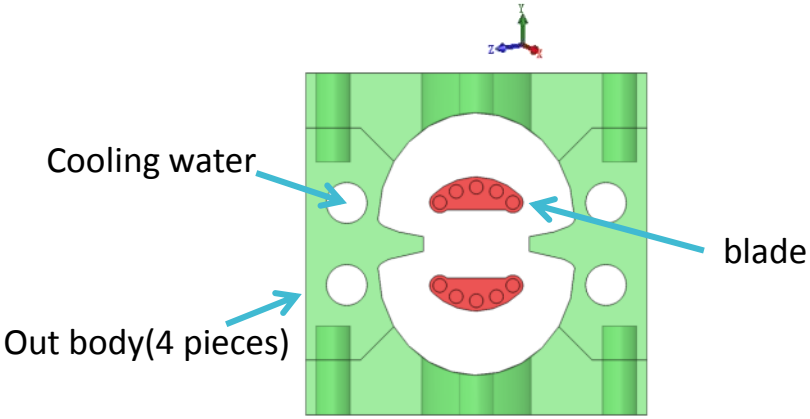
- A new compact design have been considered. The gap between adjacent kickers blade is <10mm.

5-cell module kicker Structure

- **The prototype is under design and plan to deliver to factory next month**



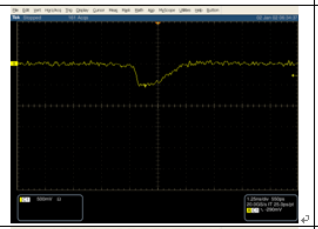
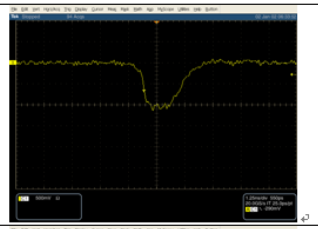
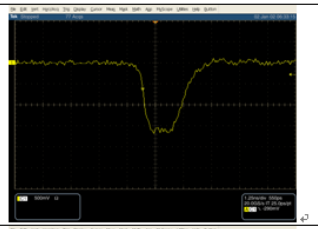
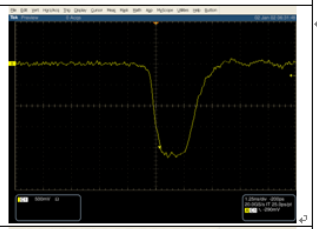
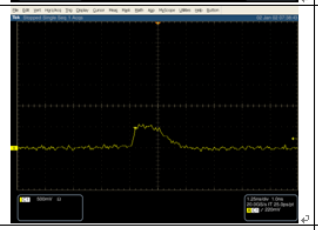
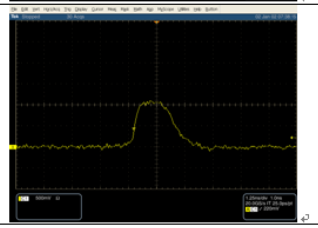
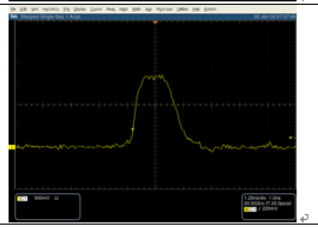
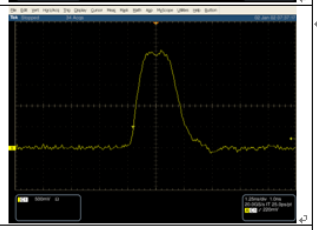
- **300mm strip-line blade without taper (cold extrusion or CNC machining)**
- **out-body Split to 4ps to machine(CNC)**
- **5 kickers in each module**



Progress of R&D on Fast Pulser

Commercial Pulser

- 4ns kicker pulser for longitudinal injection (@166+500MHz RF) is hard for us to be made at home now.
- Fortunately, the FID commercial pulser can meet our requirements.

		5 kV	10 kV	15 kV	20 kV
Negative Channel					
Positive Channel					
Rise time 10-90%	Negative channel	600 ps	600 ps	600 ps	750 ps
Rise time 5-95%	Negative channel	600 ps	1 ns	1 ns	1 ns
Flat top at 90%	Negative channel	1 ns	1 ns	1 ns	1 ns
Pulse width at 5%	Negative channel	2,5 ns	3 ns	3 ns	3,5 ns

HEPS-TF Pulser R&D

- On the other hand, HEPS-TF's task is to R&D an 8ns pulser for swap-out injection (baseline)

Parameters	Unit	Value
Quantity of Channel	-	2
Max Output Voltage	kV	±15
Max Output Current	A	300
Resistor Load	Ω	50
Pulse Rise Time（10%-90%）	ns	2
Pulse Fall Time（90%-10%）	ns	2
Pulse Flat-top Width（90%）	ns	4
Pulse Flat-top Variation	-	≤1%
Pulse Flat-top Reproducibility	-	≤1%
Pulse Tail Amplitude	-	≤3%
Pulse Rep Rate(CW)	Hz	50
Pulse Burst Rate(100ms once in every 500ms)	Hz	300
Jitter Trigger to Output（rms）	ns	0.1
Jitter Channel to Channel (rms）	ns	0.1
Skew Between Channels	ns	0.1

Fast Pulser Design Consideration

The potential technologies for HV ns-fast pulser:

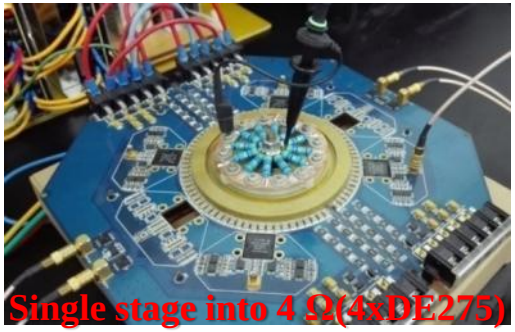
- RF-MOSFET based adder
  - Inductive adder
  - Transmission line adder
  - Marx generator
  - Series stacking
  - Hybrid Adder
- Co-axial magnetic switch compressor (shock wave transmission line)
- DSRD based PFL(Pulse Form Line) modulator
- Other switch: FID , SOS, SAS

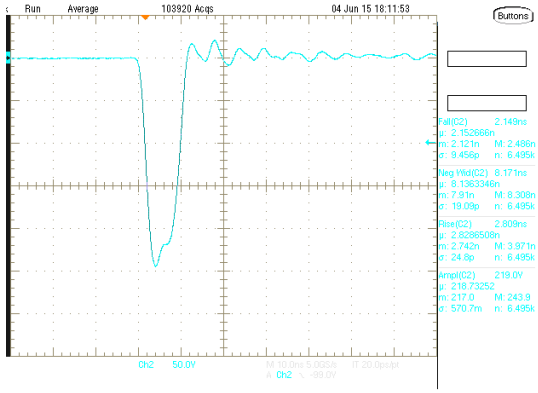
Two solutions was considered for HEPS-TF:

- Hybrid adder (inductive adder+transmission line adder) based on RF-MOSFET
- PFL(Pulse Form Line) modulator based on DSRD

1. RF-MOSFET Pulser

- It is hard to produce a short pulse(<4ns) only by commercial RF-MOSFETs and driver (IXYS DE-series MOSFET: DE275-102N06A,Tr=2ns, Min.PW=8ns; Behlke MOSFET Module: HTS-50-08-UF, Tr=1.2ns, Min.PW=5ns)





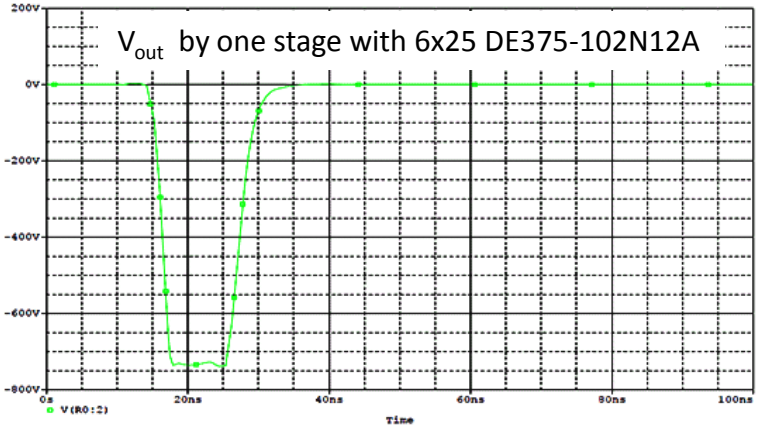
U=220V，PRF=1kHz，RL=4Ω，10X attenuation
Front edge (10%-90%）=2.15ns
Rear edge(10%-90%)=2.8ns
Width of pulse(FWHM) ≈8.2ns

- Pulsed power stacking is necessary for pulse of 15kV into 50Ω

(IXYS DE-series MOSFET: Voltage rate=1kV;

HTS-50-08-UF: Voltage rate=5kV)

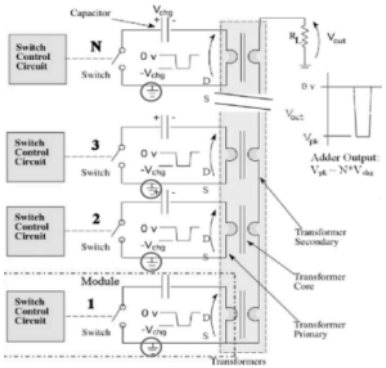
IXZ631DF12N100 X 150 (6pcX25stage)= 15kV into 50Ω

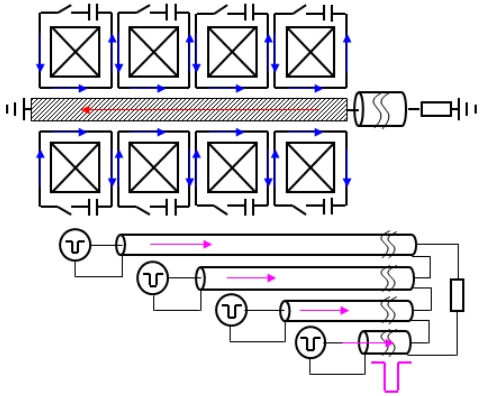


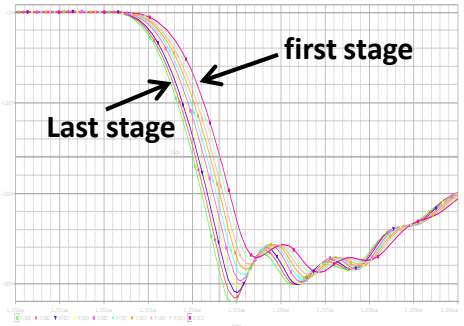
25-stage adder (inductive or TLT) simulation

Hybrid Adder Based on MOSFET

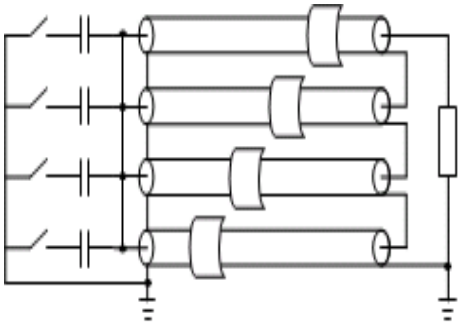
- Inductive adder with many stages would lead to slow down front edge of output pulse due to transmission line effect(TLE)





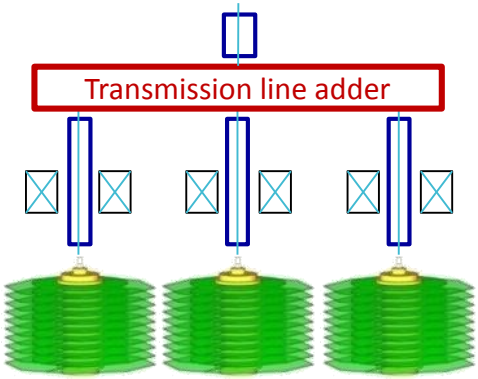


every stage pulse transmit to load end



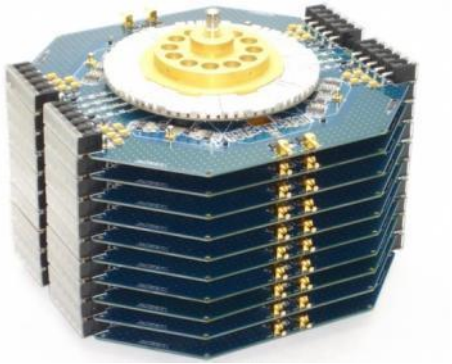
Transmission line adder

- Transmission line adder can eliminate the TLE, but it is not easy to get commercial low-impedance transmission line ;So, a hybrid adder was proposed.



3×10stage inductive adder

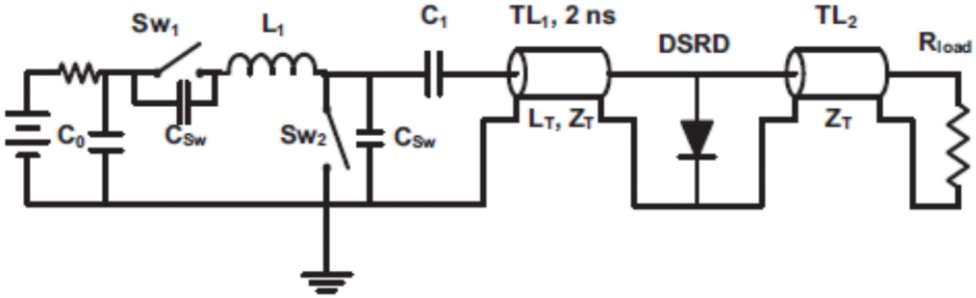
+ 3×

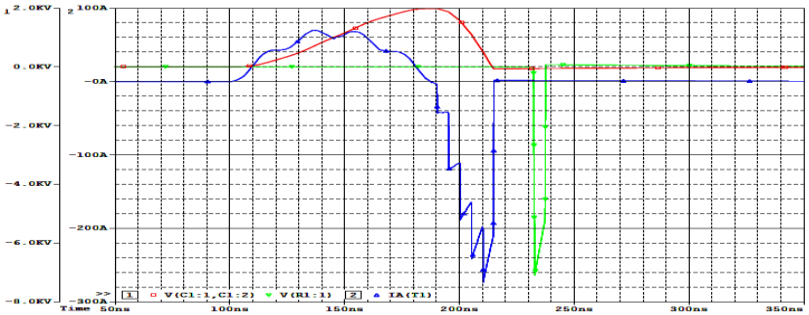


5kV inductive adder prototype built in 2011

2. DSRD Based PFL Modulator R&D

- Drift Step Recovery Diode(DSRD): Special semiconductor diode [4]
- Opening in sub-ns
- Got samples: K005 from the vender in china ($i_p \geqslant 300A$/ V_p=10kV)





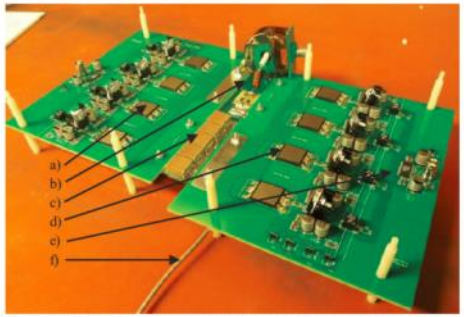
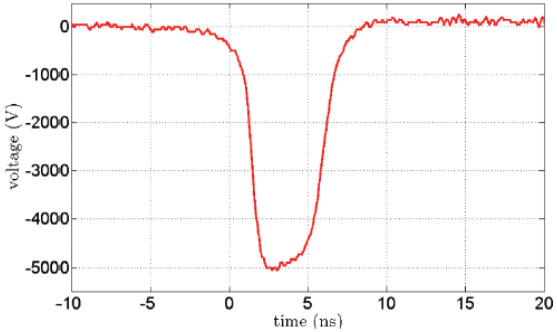


Figure 1. The 5kV pumping circuit. Shown are a)Sw_1array, b)L_1, c)energy storage capacitors, d)Sw_2 array, e)transformer isolated trigger circuit, f)TL_1 The DSRD is connected to the end of transmission line TL_1 outside of the picture range.

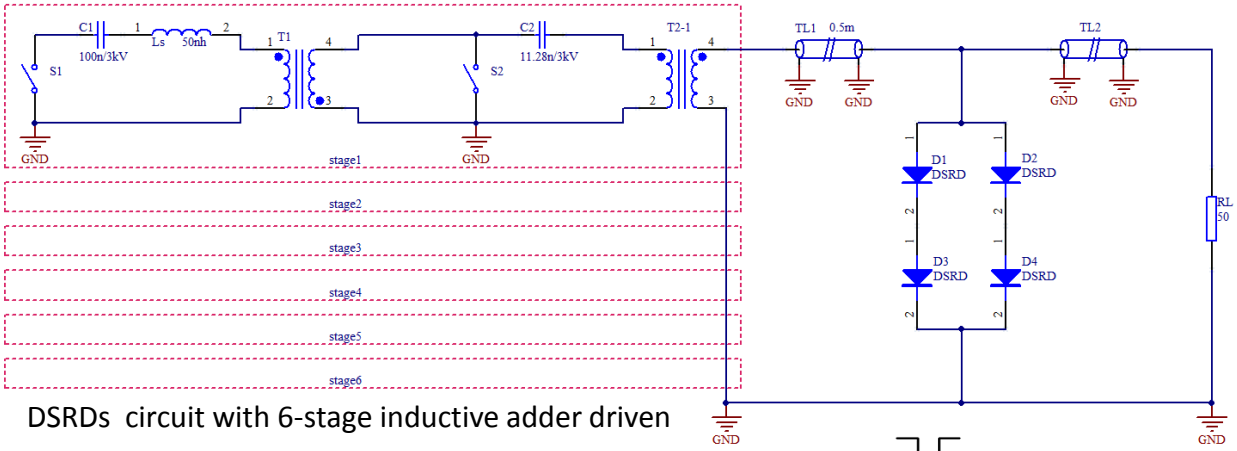
Output voltage	5 kV
Burst repetition rate	3 MHz
Pulses per burst	30
Macro repetition rate	5 Hz
Flattop pulse length	4 ns
Risetime	1 ns
Falltime	~ 1 ns
Load impedance	50 Ω



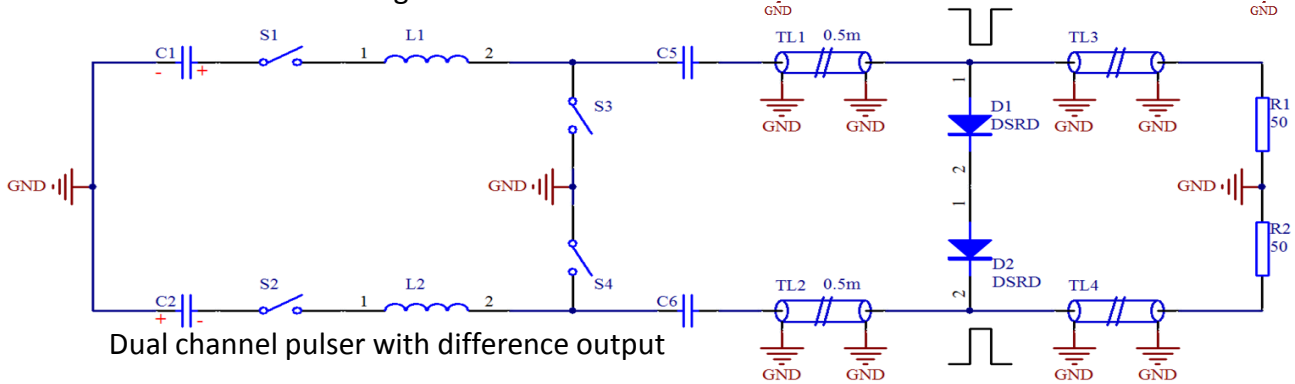
(A. Benwell1 , SLAC, A 5KV, 3MHz Solid-state Modulator Based on theDSRD Switch for an Ultra-fast Beam Kicker)

±15kV DSRD Pulser Circuit Design

- A 6-stage inductive adder for DSRD pumper circuit; Its advantages are free HV components and isolated driver (<1kV); need much fewer components
- 4 DSRDs(2 parallel, 2 series) switching 600A into 50 Ω;It is independent to the pumper
- 0.5m long PFL(TL1) for p_w=5ns



DSRDs circuit with 6-stage inductive adder driven

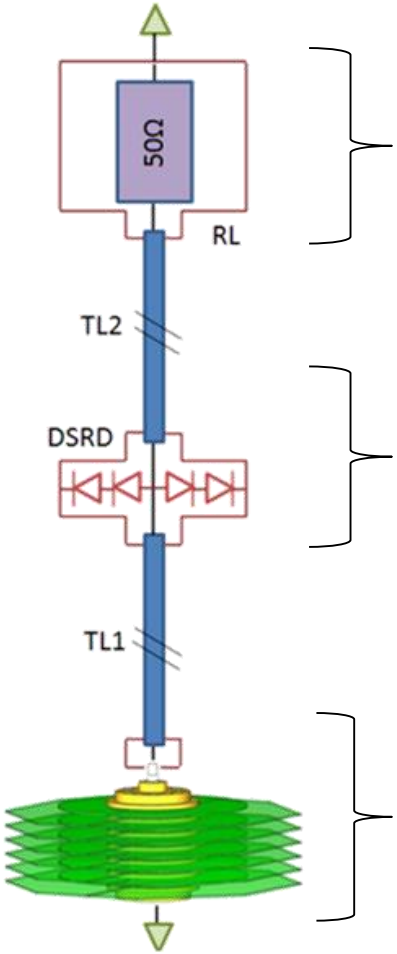


Dual channel pulser with difference output

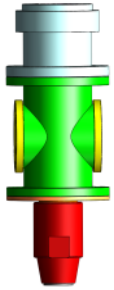
DSRD Pulser Structure Design

The whole pulser is design as 50Ω coaxial structure, including:

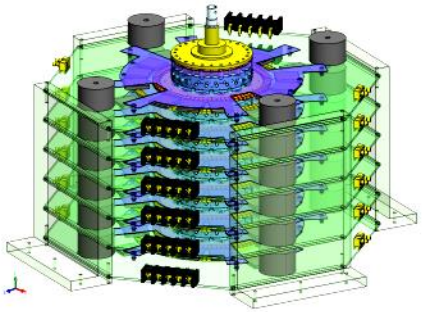
- ◆Pumper circuit (6-stage inductive adder based MOSFET)
- ◆PFL and Transmission line
- ◆DSRD assembly
- ◆Terminal attenuation



HV RF Attenuation

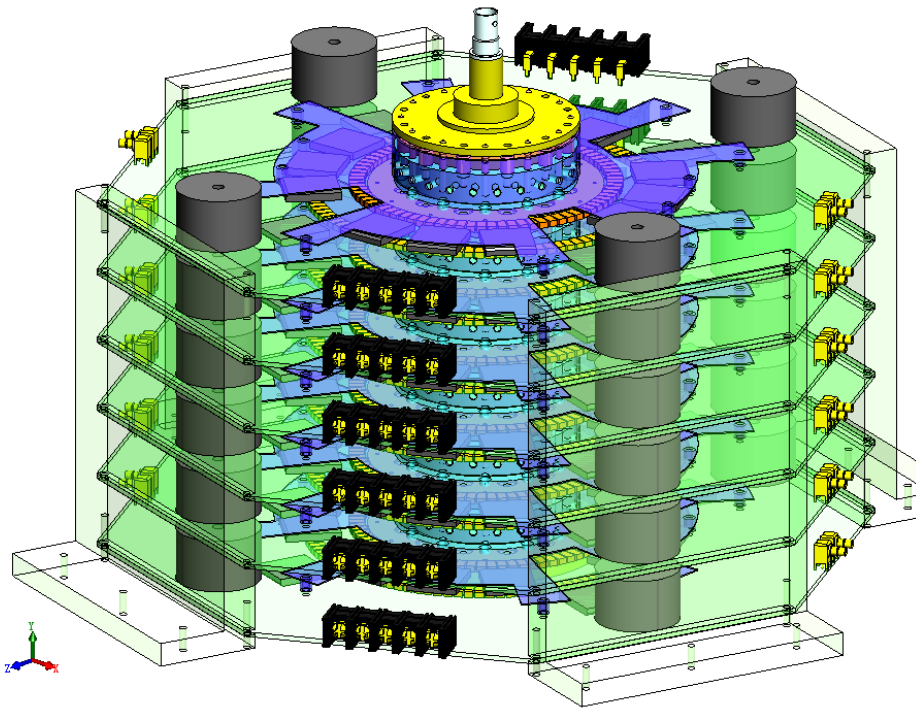


DSRDs

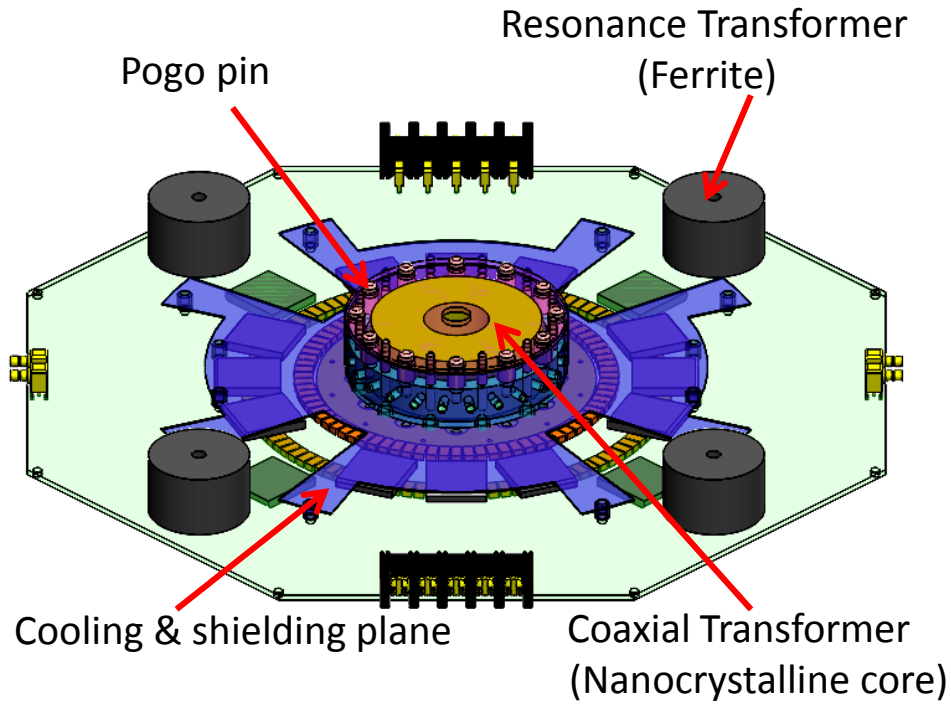


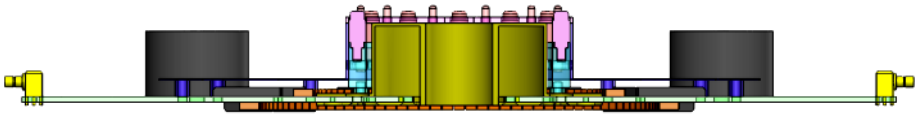
DSRD pumping power supply (inductive adder)

6-stage Pumper DSRD Pulser

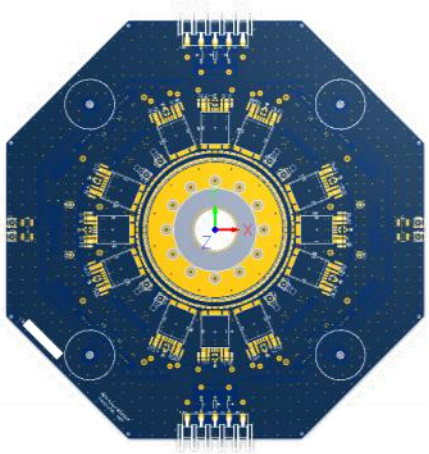


6-stage Inductive adder



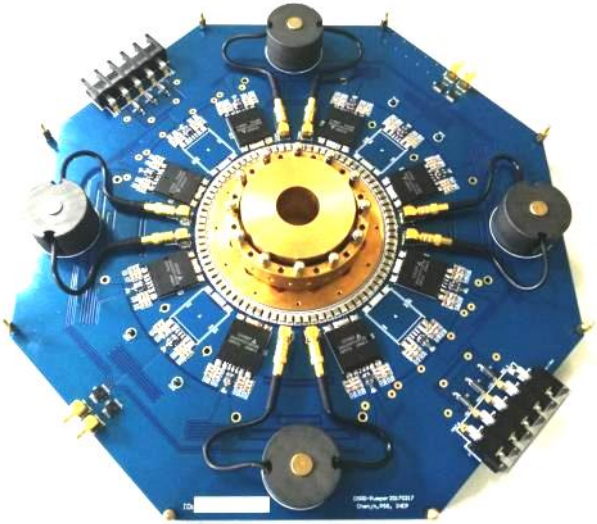


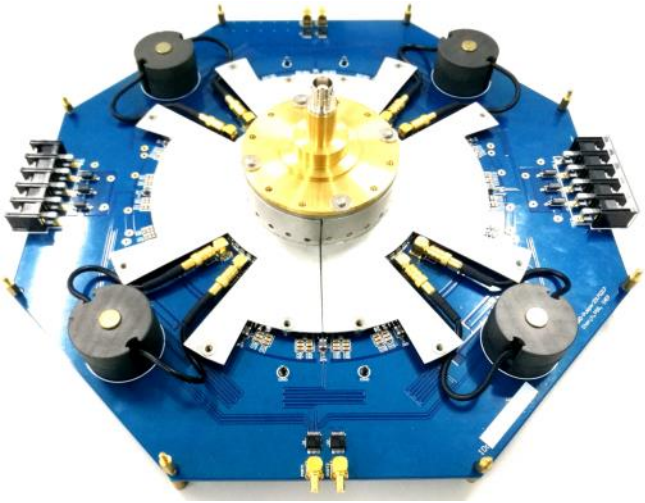
Pumper P.S. PCB Design and Assembling



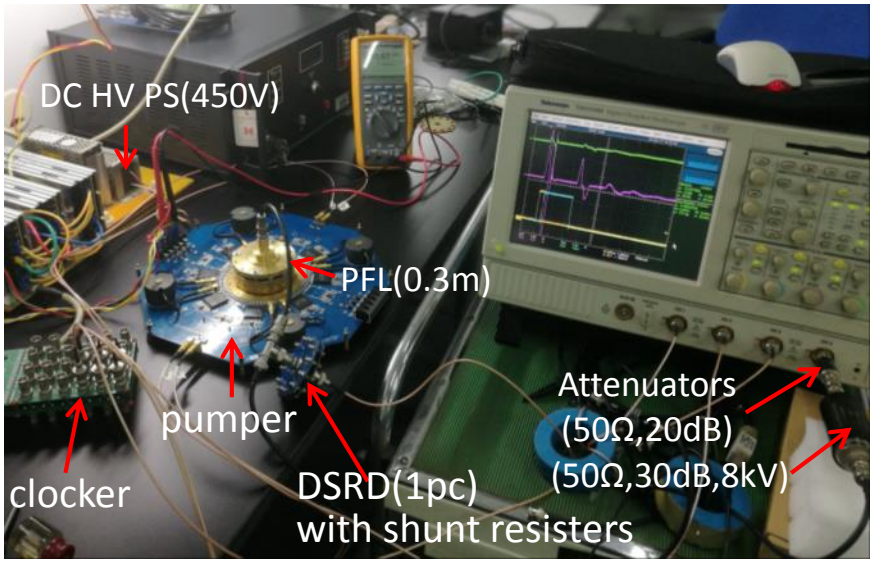
Top layer

Bottom layer

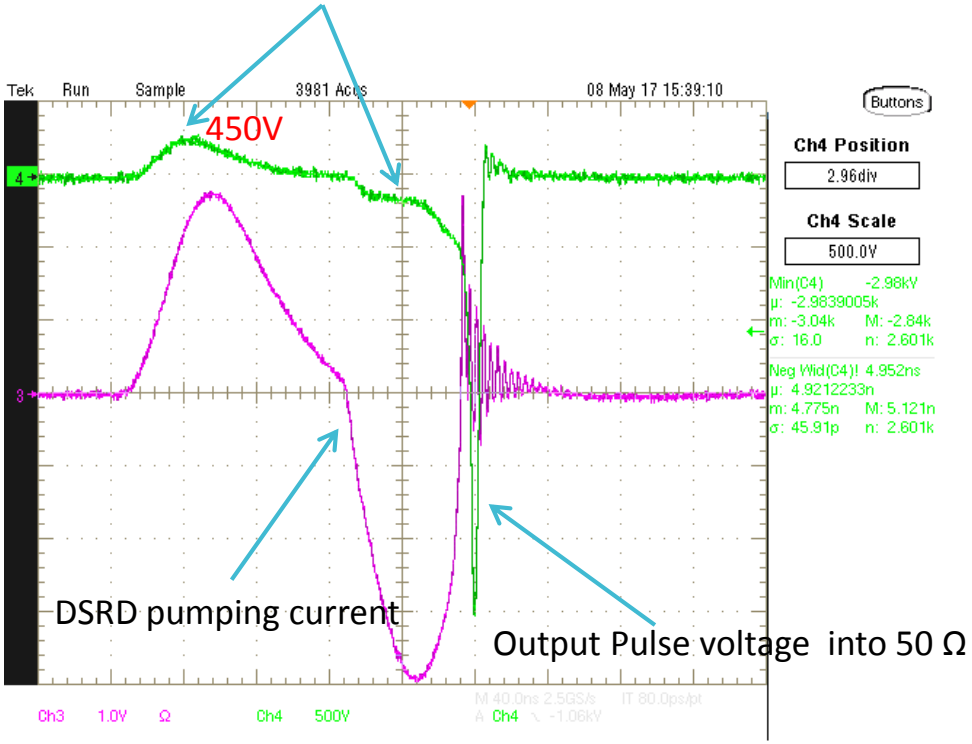




First PCB Assembling and Test

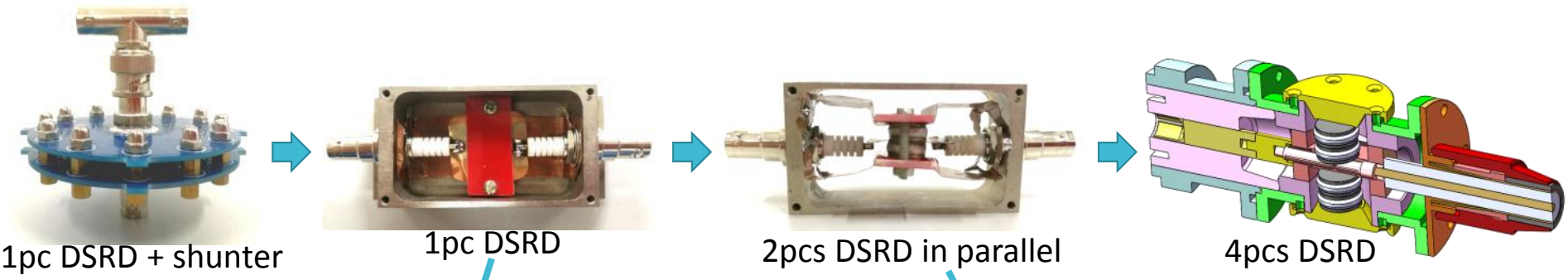


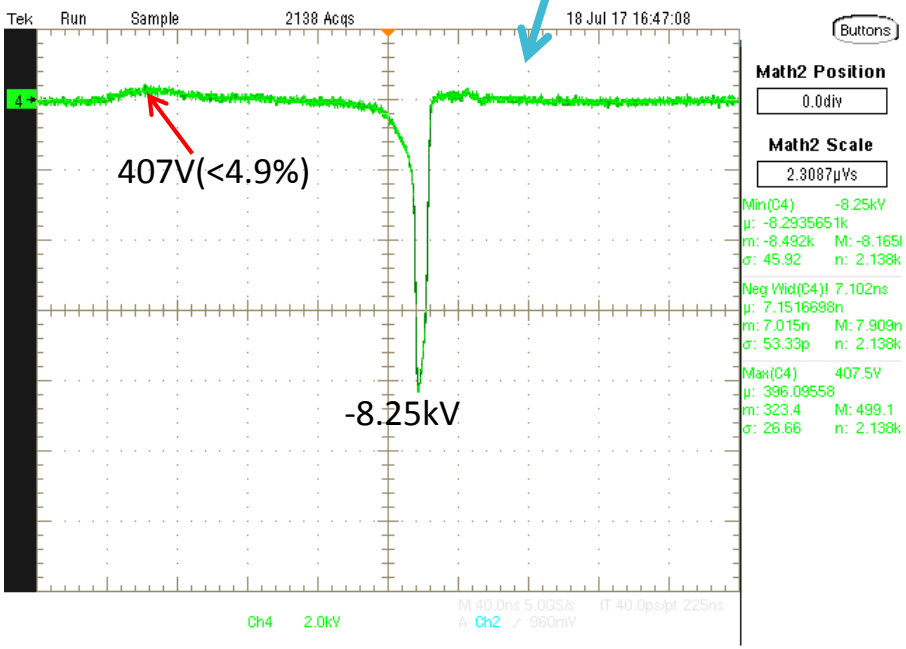
Voltage step during pumping caused by DSRD loop stray inductance ,shunt resistance, T-BNC-connector

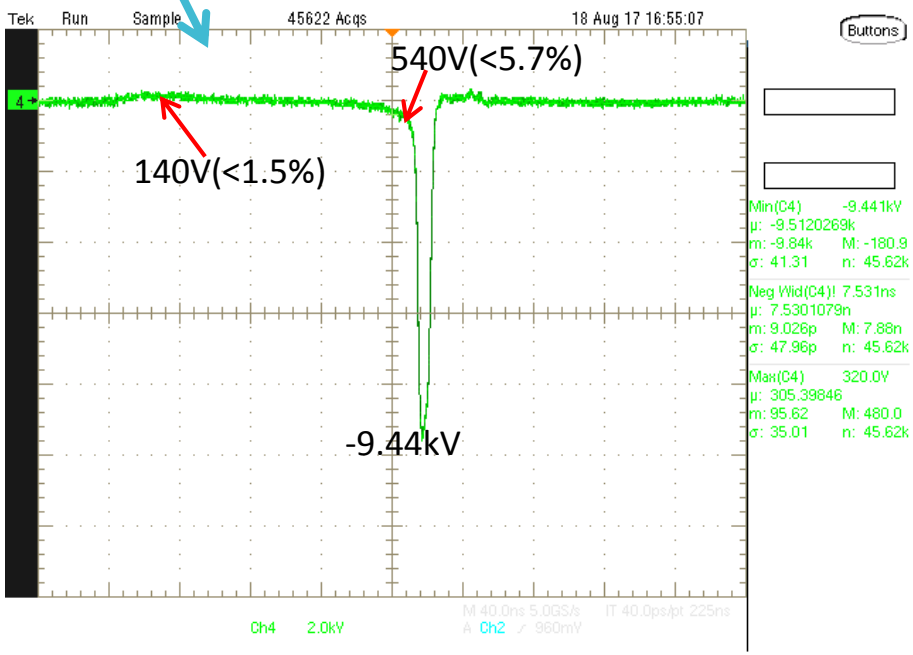


- Single stage pumper, PFL=0.3m
- Input DC HV=450V
- Attenuator:30dB+20dB, 50Ω
- Output pulse:
  - Pulse Amplitude=3.1kV
  - Pulse Width(FWHM)=4.9ns

DSRD housing improvement

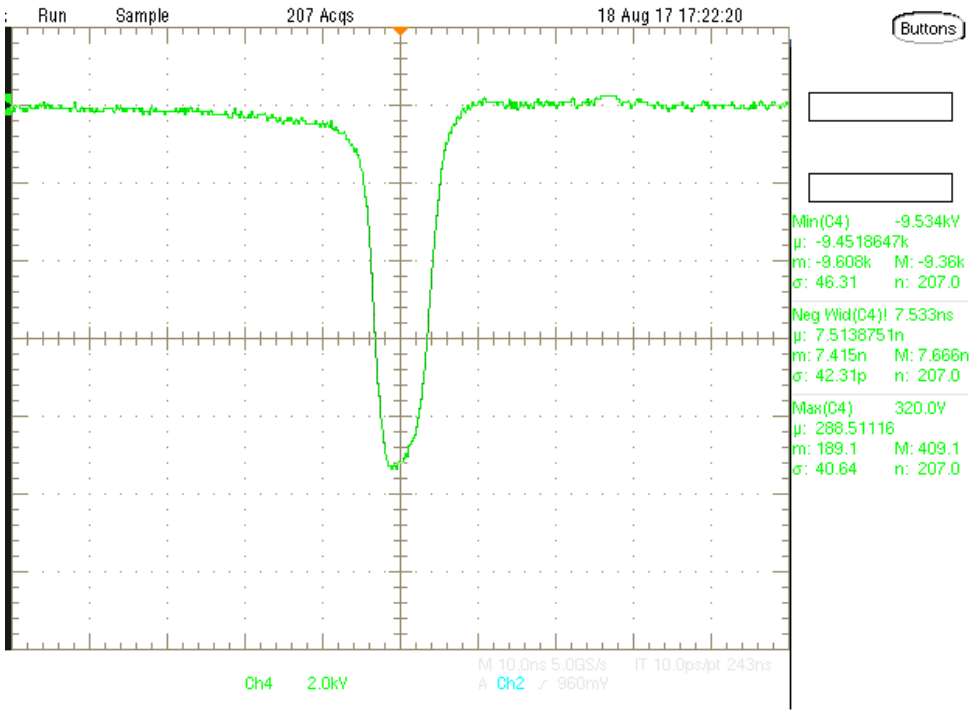






test at 3 stages, Input DC HV=450V

Latest 3-stage Circuit Testing



- 3 stage pumper
- 2Pcs DSRD in parallel,0.5m PFL
- Input DC HV=450V
- Attenuator:30dB+20dB, 50Ω
- Output pulse:
  - Pulse Amplitude=9.5kV
  - Pulse Width(FWHM)=7.5ns

3-stage testing is so far so good, and 6-stage full-power prototype is going to be tested after new DSRD housing , HV cable, connector, and attenuator is available next month.

Summary

- Due to small DA, only On-axial swap-out injection and longitudinal injection based on ultra-fast kicker system are possible for HEPS. So, the task of HEPS-TF is to R&D a set of strip-line kicker system.
- A 750mm-long strip-line kicker is being fabricated. A 300mm-long compact strip-line kicker design is ongoing.
- For kicker pulser, MOSFET-based hybrid adder and DSRD-based PFL modulator are both potential approach for 8ns pulser .
- Limited by switch speed, MOSFET-based adder is difficult to get a shorter pulse (PW<5~8ns).
- A DSRD PFL modulator with a special 6-stage inductive adder pumper was designed. A half prototype was tested successfully and R&D is ongoing.

Reference

[1] C. Yao,…Development of Fast Kickers For The APS MBA Upgrade, Proceedings of IPAC2015

[2] X. Sun,…Simulation Studies Of A Prototype Stripline Kicker for the APS-MBA Upgrade

[3] C. Yao,… Preliminary Test Results of a Prototype Fast Kicker for APS MBA Upgrade

[4] A. Benwell1 , SLAC, A 5KV, 3MHz Solid-state Modulator Based on theDSRD Switch for an Ultra-fast Beam Kicker

Thanks for your attentions !