Inductive Adders for the CLIC Damping Ring Kickers

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Outline

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  - Specifications for CLIC DR Extraction Kicker Modulator
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  - Methods to Improve the Pulse Flat-top Stability
- Prototyping and Measurements
  - Prototypes 1-4
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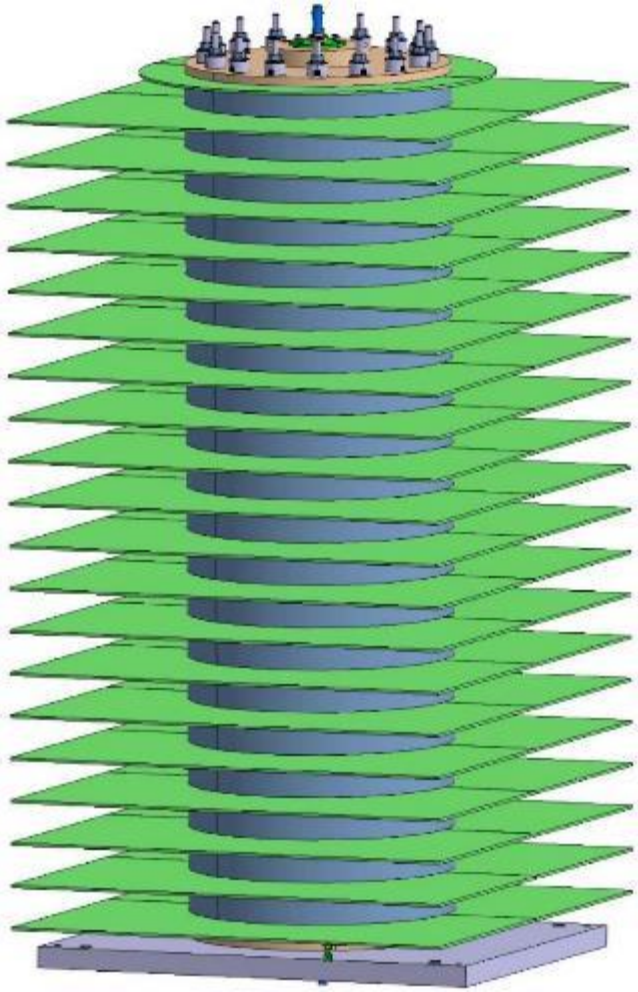
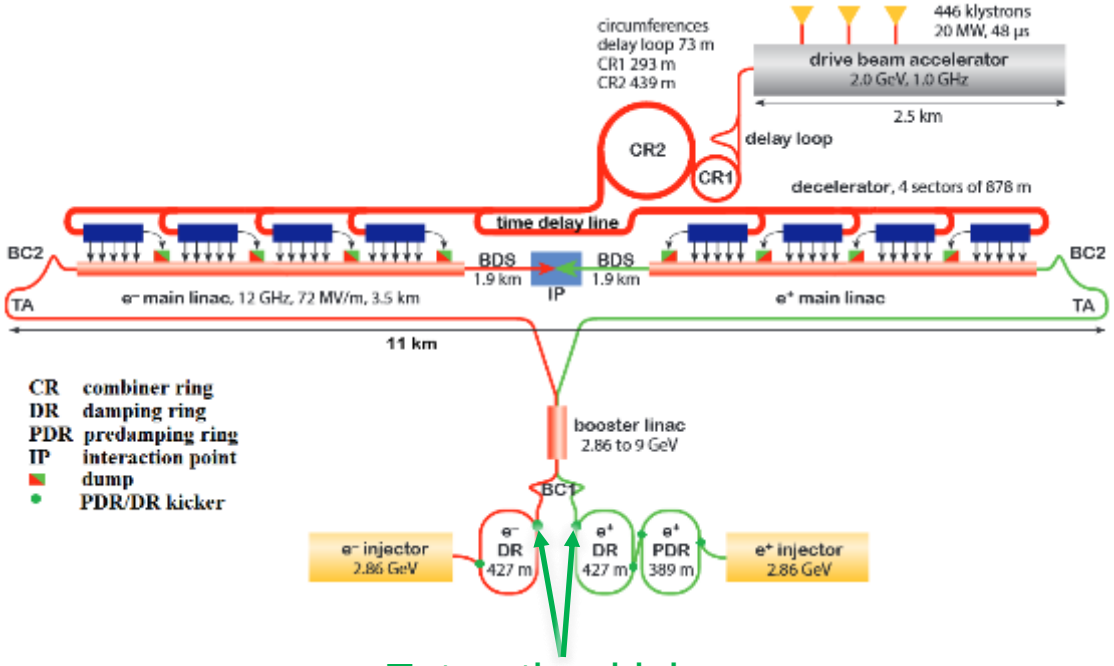
  - Measurements on a Controlled Decay Waveform
  - Measurement Techniques
- Summary and Future Work



Compact Linear Collider (CLIC)

- Electron-positron collider, up to 48 km (3 TeV) long linear accelerator.
- Several stages: Injectors, Pre-Damping (**PDR**) and Damping Rings (**DR**) and main linear accelerators.
- A crucial parameter to be minimized is the beam emittance (“cross-sectional area of the beam”).
- The emittance of the beam is reduced by PDRs and DRs. The energy of the particle beam is preserved, but the emittance of the beam is decreased.
- Each bunch passes through the linear accelerator only once: any variation of the electric and/or magnetic field of the **DR extraction kicker** would cause the emittance to increase.

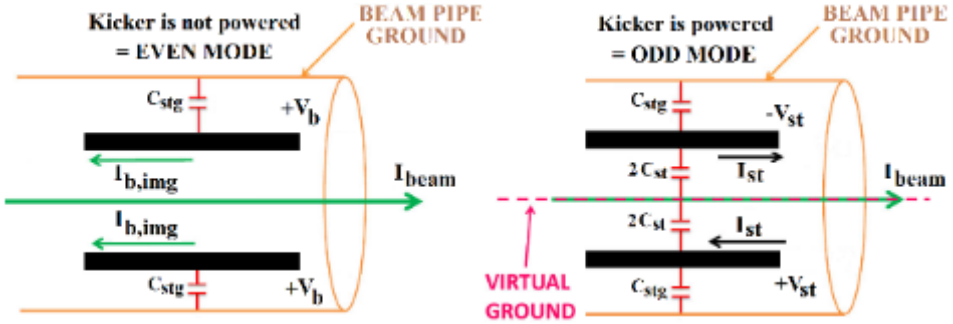


CLIC layout for 380 GeV baseline

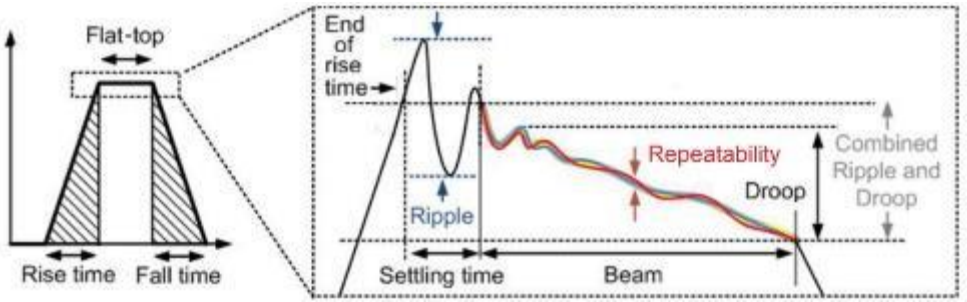
Specifications for CLIC DR Extraction Kicker Systems

	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (per electrode)	±12.5 kV
Electrode pulse current [40.5 Ω load]	±309 A
Repetition rate	50 Hz
Pulse flat-top duration *900 ns = 160 ns + 580 ns gap + 160 ns	~160 ns | ~900* ns
Flat-top repeatability	$\pm 1 \times 10^{-4}$ (±0.01 %)
Flat-top stability [droop+ripple]	$\pm 2 \times 10^{-4}$ (±0.02 %)
Field rise time	1000 ns (max.)
Field fall time	1000 ns (max.)
Beam energy	2.86 GeV
Total kick deflection angle	1.5 mrad (0.09 deg)
Aperture	20 mm
Effective length	1.7 m
Field inhomogeneity [1 mm radius]	±0.01 %

- **Extremely tight requirements for flat-top stability and repeatability!**
- **For rise/fall times, ≤ 100 ns desired.**

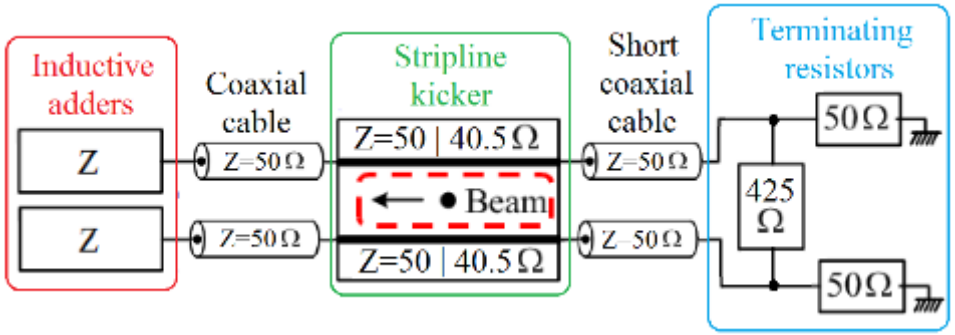


- **Stripline kicker: two electrodes, powered with opposite polarities**
- **Both electric and magnetic fields deflect the beam.**
- **Impedances of the striplines are 50 Ω when "off" and 40.5 Ω when "on":**

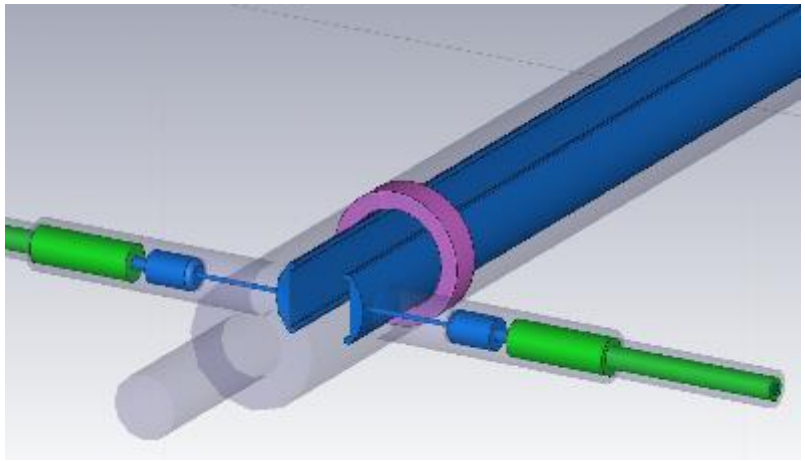


CLIC DR kicker pulse definition

Specifications for the CLIC DR Extraction Kicker Modulators: *Waveform* stability & repeatability



Simplified schematic of a CLIC DR stripline kicker system

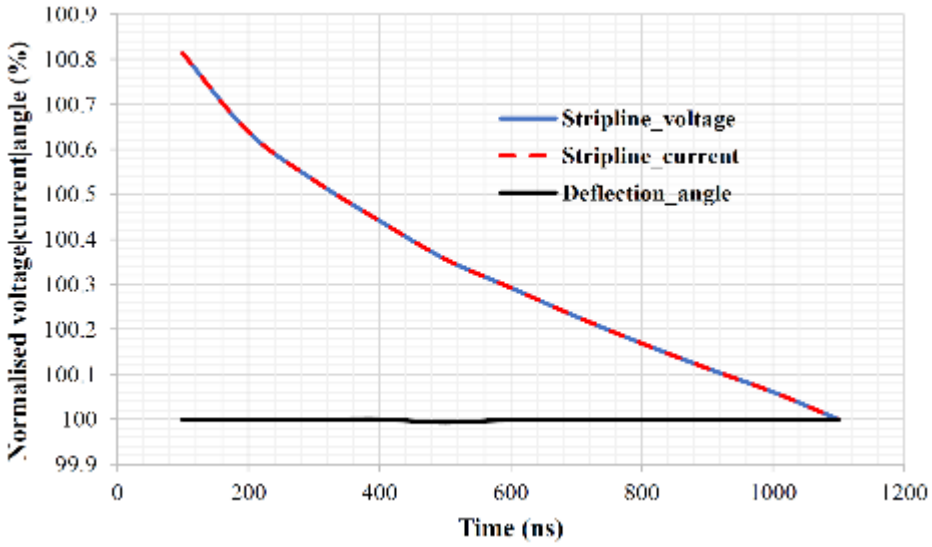


3D model of the CLIC DR stripline electrodes

- **Stripline kicker: both electric and magnetic fields deflect the beam.**
- **Impedances of the striplines are 50 Ω when "off" and 40.5 Ω when "on": both modes are matched with a terminating resistor network.**
- **The total deflecting angle for particles in each bunch during a single kick should be the same.**
- **According to optimization studies of the CLIC DR prototype stripline kicker (by C. Belver-Aguilar), the impedance of the kicker changes during the pulse: in order to generate the same deflection for each bunch, the voltage and current need to be modulated.**
- **The optimum waveforms for both stripline electrodes are identical "controlled decays": these generate a constant "flat-top" for total deflecting field.**

Specifications for the CLIC DR Extraction Kicker Modulators: *Waveform* stability & repeatability

	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (per electrode)	±12.5 kV
Stripline pulse current [40.5 Ω load]	±309 A
Repetition rate	50 Hz
Pulse waveform duration *900 ns = 160 ns + 580 ns gap + 160 ns	~160 ns | ~900* ns
Waveform repeatability	$\pm 1 \times 10^{-4}$ (±0.01 %)
Waveform stability	$\pm 2 \times 10^{-4}$ (±0.02 %)
Voltage rise/fall time	< 1000 ns



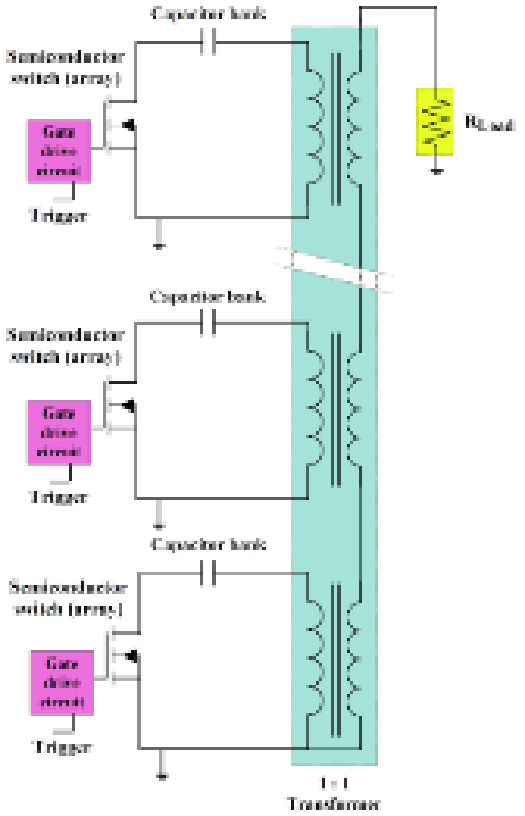
- The required waveforms (for each electrode) are controlled decays.
- Definitions for waveform parameters
  - Repeatability: difference of amplitudes of any two waveforms during the ”flat-top” of the pulse (160 | 900 ns)
  - Stability: difference between the optimum waveform and a generated waveform at any time point during the ”flat-top” of the pulse.
- Extremely tight requirements for waveform stability and repeatability!
- For rise/fall times, ≤ 100 ns desired

Goals and Challenges

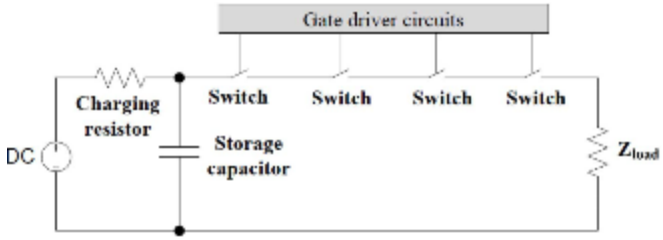
- As part of feasibility study of CLIC, the following goals have been set:
  1. Identifying the most suitable topology for the CLIC DR kicker modulator.
  2. Proposal for possible means for achieving the required performance regarding flat-top stability and repeatability.
  3. Design, manufacturing and testing of the prototype pulse modulator.
  4. Design and manufacturing of two full-scale modulators and, finally, testing of them in a beamline with the prototype stripline kicker.
- Challenges
  - ±0.02 % (± 2.5 V) requirement for the flat-top/waveform stability at ±12.5 kV for 160-900 ns is an extremely demanding specification: an order of magnitude better than in any existing kicker systems! E.g. for the LHC injection kickers, stability requirement is ±0.5 %.
  - Impedance mismatch: even-mode impedance 50 Ω, odd-mode impedance ~40.5 Ω!
  - How to generate the required waveform?
  - How to measure it?
- Evolution of parameters
  - Prototypes 1&2 (2012-): 160 ns flat-top, 50 Ω load
  - Prototype 3 (2015-): ~900 ns flat-top, 40.9 Ω load
  - Prototypes 4&5 (full-scale) (2017-): 900 ns ”controlled decay waveform”, ±12.5 kV, 40.5 Ω load (309 A) + option for ±17.5 kV, 400 A (dump kicker).

Topology: Inductive Adder

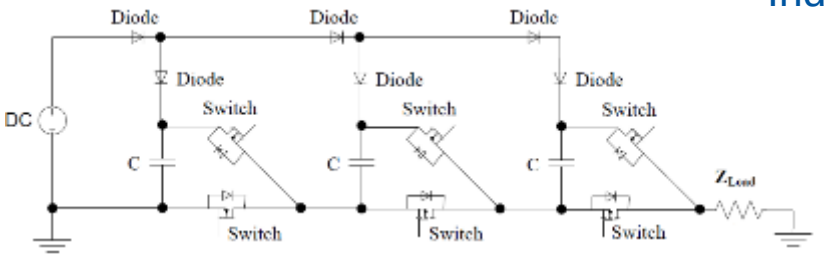
- According to an extensive literature survey, the most suitable topologies for the CLIC DR kicker systems were the following:
  - Series switch topology
  - (Solid-state) Marx modulator
  - Inductive adder
- The **inductive adder** was selected as the most promising candidate.
  - Many primary “layers”, each with solid-state switches
  - The output voltage is approximately the sum of the voltages of the primary constant voltage layers



Inductive adder



Series switch topology



Solid-state Marx modulator

Topology: Inductive Adder

- Its advantages, in comparison with the two other topologies, are the following:

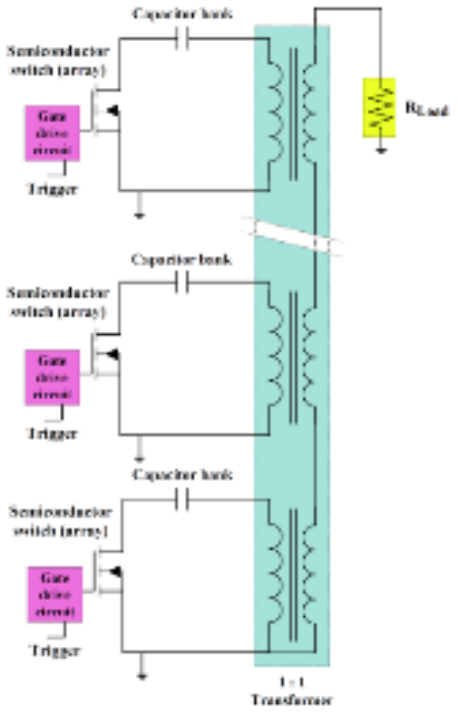
  + The output voltage can be modulated during the pulse by passive/active analogue modulation.

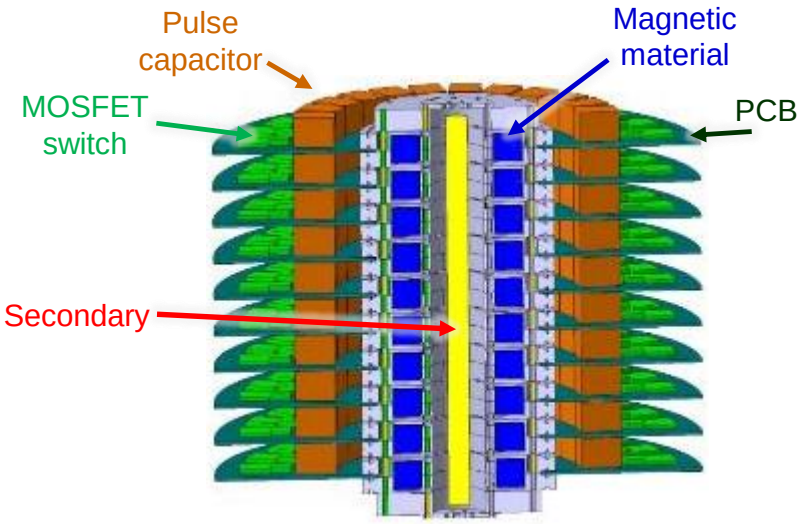
  + Possibility to generate positive or negative output pulses with the same adder: the polarity of the ouput pulses can be easily changed by grounding the other end of the output of the adder

  + All control electronics referenced to ground potential.

  + Built-in fault tolerancy and redundancy: if one switch or layer fails, the adder still gives full voltage or a significant portion of the required output pulse (good for the machine safety).

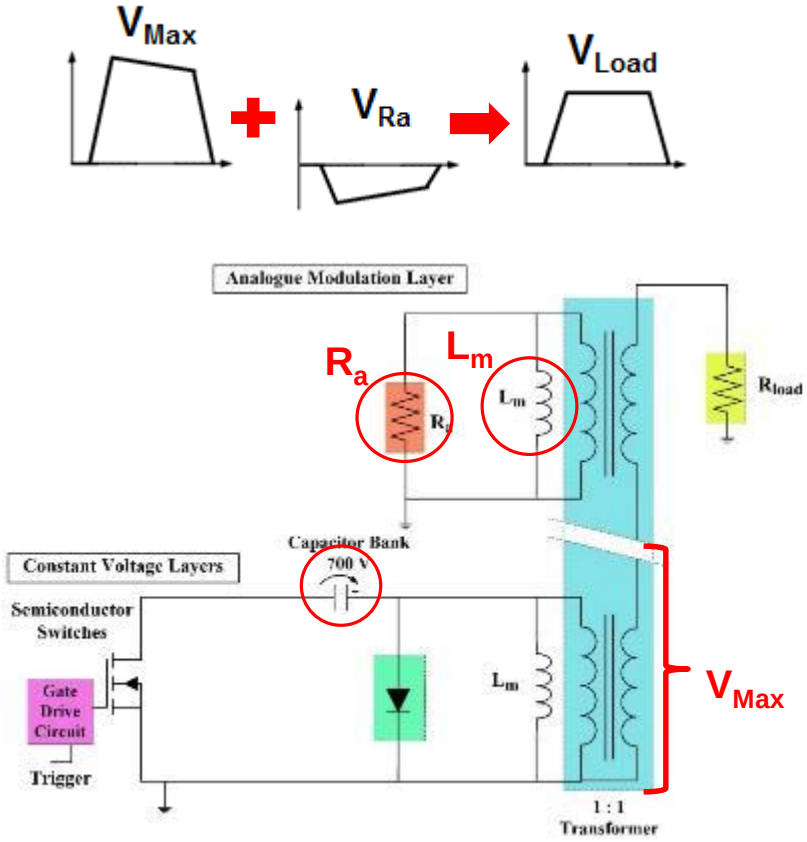
  + Modularity: the same design can potentially be used for kickers with different specifications (CLIC PDR & DR kicker modulators, extraction + dump kicker)





Improving the Pulse Flat-top Stability: **Passive** and Active Modulation

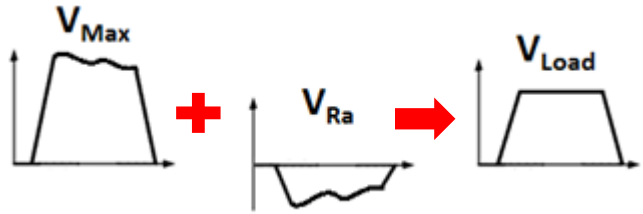
- Droop and ripple of the output pulse can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the sum of the voltages across all of the layers.
- Two modes:
  - **Passive mode:** During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction in the primary voltage (i.e. droop) of the other layers.

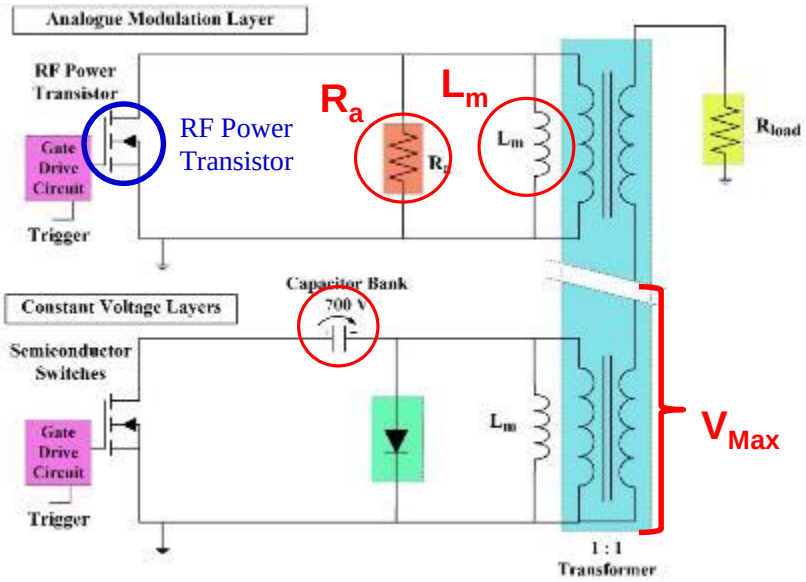


Passive analogue modulation

Improving the Pulse Flat-top Stability: Passive and **Active** Modulation

- Droop and ripple of the output pulse can be compensated with an analogue modulation layer
- In the analogue modulation layer, resistor R_a is effectively in series with the load
- The load voltage is the sum of the voltages across all of the layers.
- Two modes:
  - **Passive mode:** During the pulse, current through L_m increases, which causes current through R_a to decrease. Therefore, voltage over R_a decreases, which can compensate for a reduction in the primary voltage (i.e. droop) of the other layers.
  - **Active mode:** A linear RF power transistor in parallel with resistor R_a. The voltage across R_a can be controlled by modulating the current through the RF power transistor.



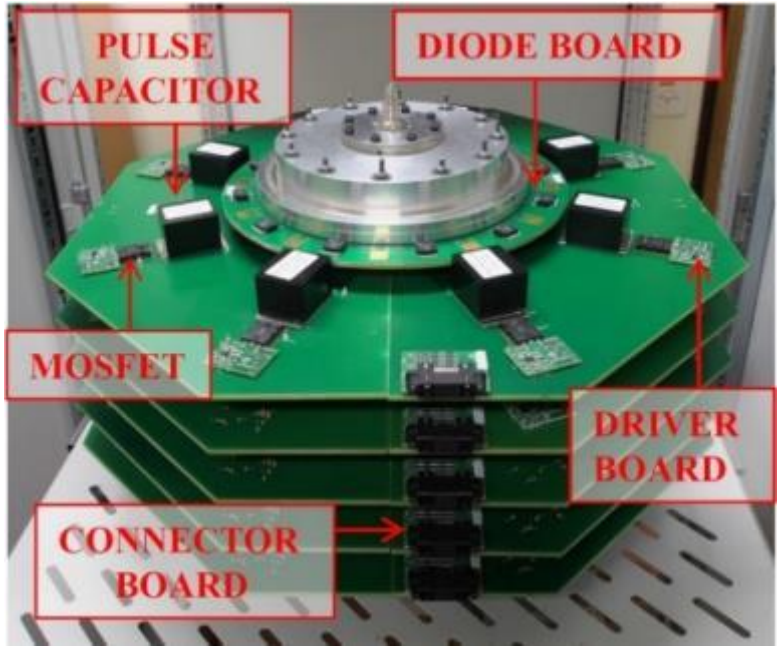


Active analogue modulation

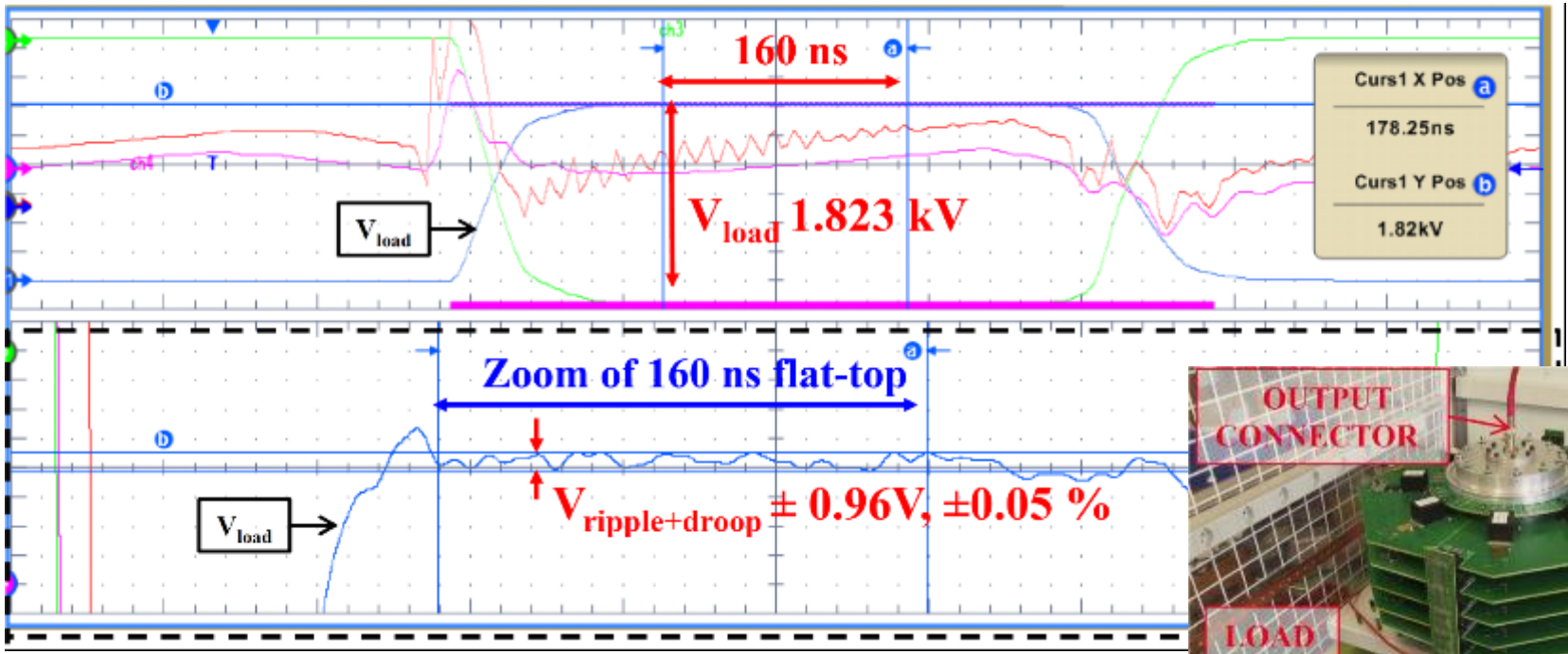
The First Two 5-Layer Prototype Inductive Adders

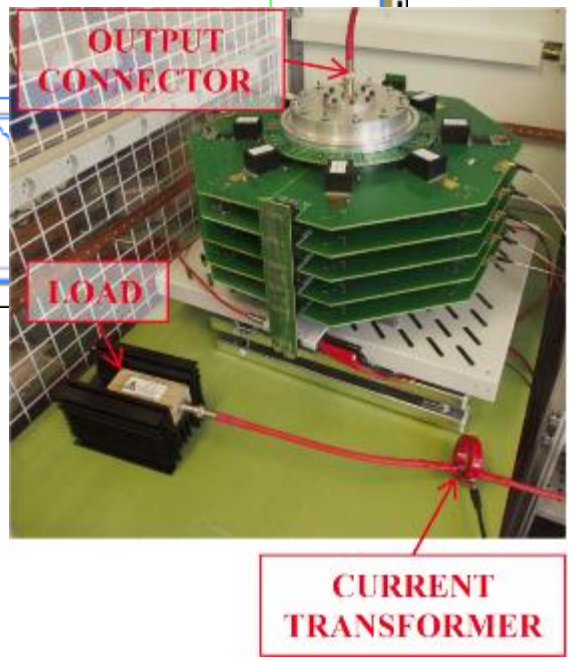
- The purposes of the prototype inductive adders have been:
  - To verify experimentally theoretical models and design steps for an inductive adder with extremely high flat-top stability.
  - To test and evaluate main components (MOSFETs, pulse capacitors, magnetic cores)
  - To test both passive and active analogue modulation
  - To approach the required ±0.02 % flat-top stability for the output pulse, as specified for the CLIC DR extraction kicker system
  - To evaluate magnetic core material for the 12.5 kV prototype inductive adder
  - Status: available as a test bench: 3.5 kV, 70-250 A, 250-900 ns, up to 50 Hz.

Design Parameter	Prototype Inductive Adder	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**3.5**	12.5
Output Current [50 Ω load] (A)	**70 (250)**	250
Voltage per layer	**700**	700
Number of layers	**5**	20
Pulse flat-top duration (ns)	**Up to 900**	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**≤ 100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**≤ 100**	< 1000
Targe flat-top stability (for 160 ns)	**≤ ±0.02 %**	±0.02 %
Repetition rate (Hz)	**Up to 50**	50



Measurements on Prototypes 1&2 (2014)





- **Setup for the measurement:**
  - Vacuumschmelze W567 cores
  - 4 constant voltage layers
  - 1 active analogue modulation layer
  - 1 branch powered per half-layer PCB, 2 branches per layer
  - Capacitors (24 µF/layer) initially charged to 551 V
  - **Active compensation of droop and ripple**
  - **Measurements with a 8-bit oscilloscope (average of 1000 pulses)**

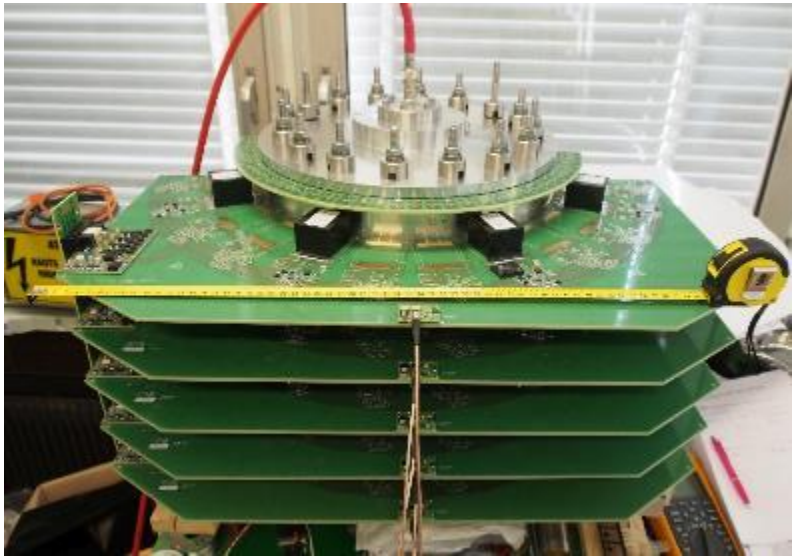
⇨ ±0.05 % (±1 V) flat-top stability over 160 ns at 1.8 kV

Prototype 3: the First 5 ”Full-scale” Layers of the 12.5 kV, 20-layer, Inductive Adder

- 5-layers, otherwise identical design with 20-layer, 12.5 kV CLIC DR extraction kicker inductive adder.
- Specifications according to requirements for CLIC DR extraction kicker.
- Target flat-top stability ±0.02 % for 900 ns, target flat-top repeatability ±0.01 % for 900 ns.
- Status: in operation, used as a test bench for printed circuit boards (PCBs) and magnetic cores.

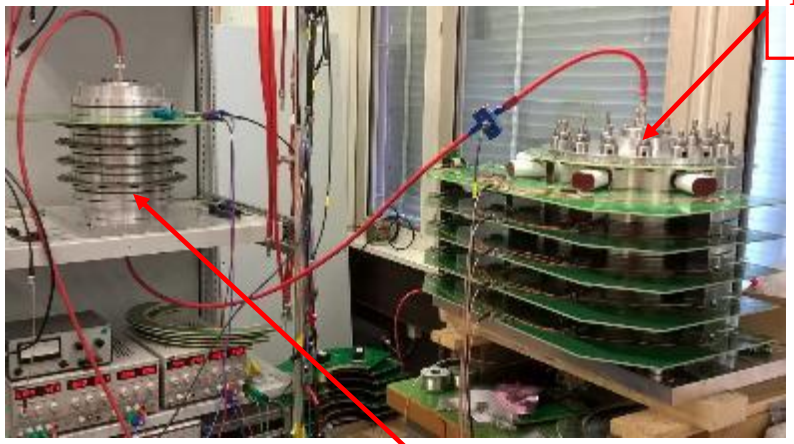
Design Parameter	5-Layer Full-Scale Prototype	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**3.5**	12.5
Output Current	**308***	250
Voltage per layer	**700**	700
Number of layers	**5**	20
Pulse flat-top duration (ns)	**1100**	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**100**	< 1000
Flat-top stability (for 900* ns)	**≤ ±0.02 %**	±0.02 %
Flat-top repeatability (for 900* ns)	**≤ ±0.01 %**	±0.01 %

*Stripline odd-mode impedance 40.5 Ω



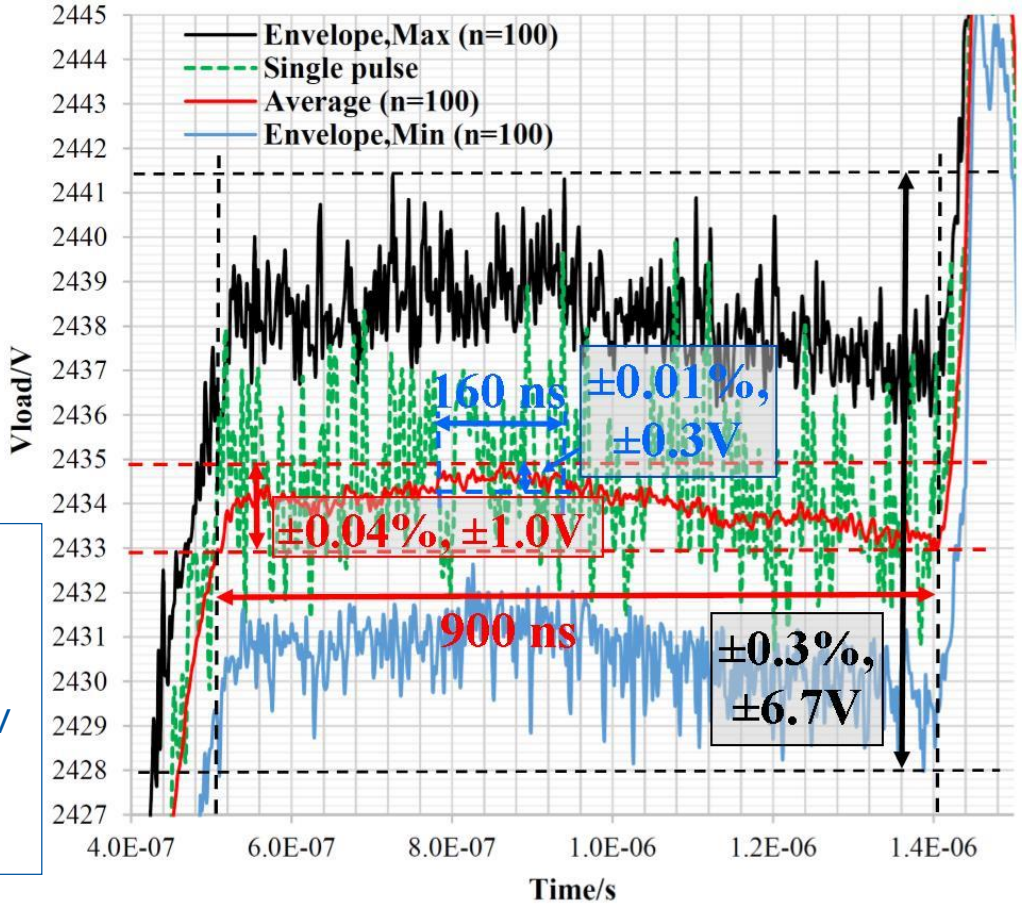
First 5 layers of the 12.5 kV inductive adder assembled at CERN

Measurements on Prototype 3 (2016)



New 3.5 kV, 5-layer, full-scale inductive adder prototype

2nd inductive adder with an analogue modulation layer only (in series with the 3.5 kV inductive adder)



- **Setup for the measurement:**
  - 5 constant voltage layers, Finemet FT-3L cores
  - 1 active analogue modulation layer
  - 1 branch powered per half-layer PCB
  - Capacitors (24 µF/layer) initially charged to 555 V
  - **Active compensation of droop (not ripple)**
  - **Measurements with a 16-bit (effective) oscilloscope!**

⇨ **Flat-top stability ±0.01% (±0.3 V) over 160 ns, ±0.04% (±0.3 V) over 900 ns.**

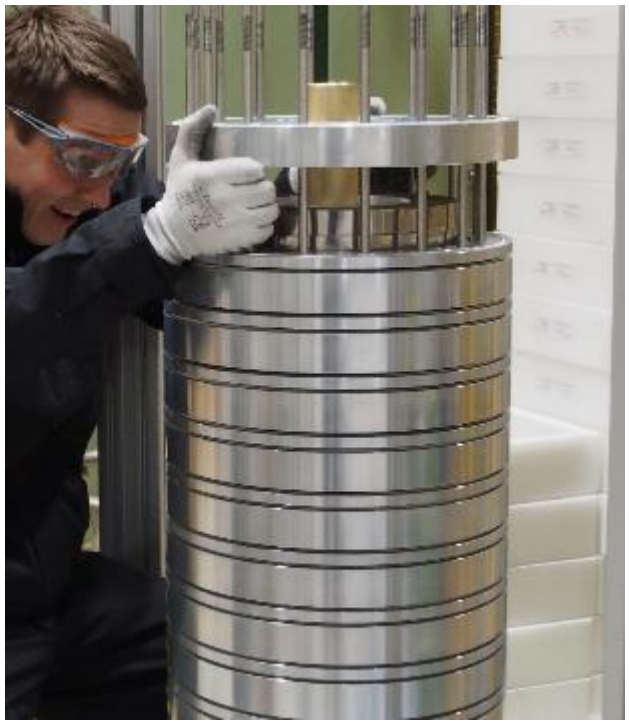
⇨ **CLIC DR specifications: ±0.02% (±2.5 V) for 160|900 ns (1 GHz|2 GHz)**

Prototype 4: Full-Scale,12.5 kV, 20-layer, Inductive Adder for CLIC DR Extraction Kicker System

- Specifications according to requirements for CLIC DR extraction kicker:
  - Target waveform stability ±0.02 % for 900 ns at 12.5 kV
  - Target waveform repeatability ±0.01 % for 900 ns at 12.5 kV
- Status: assembled, measurements carried out with up to 17 constant voltage layers + 1 analogue modulation layer until now.

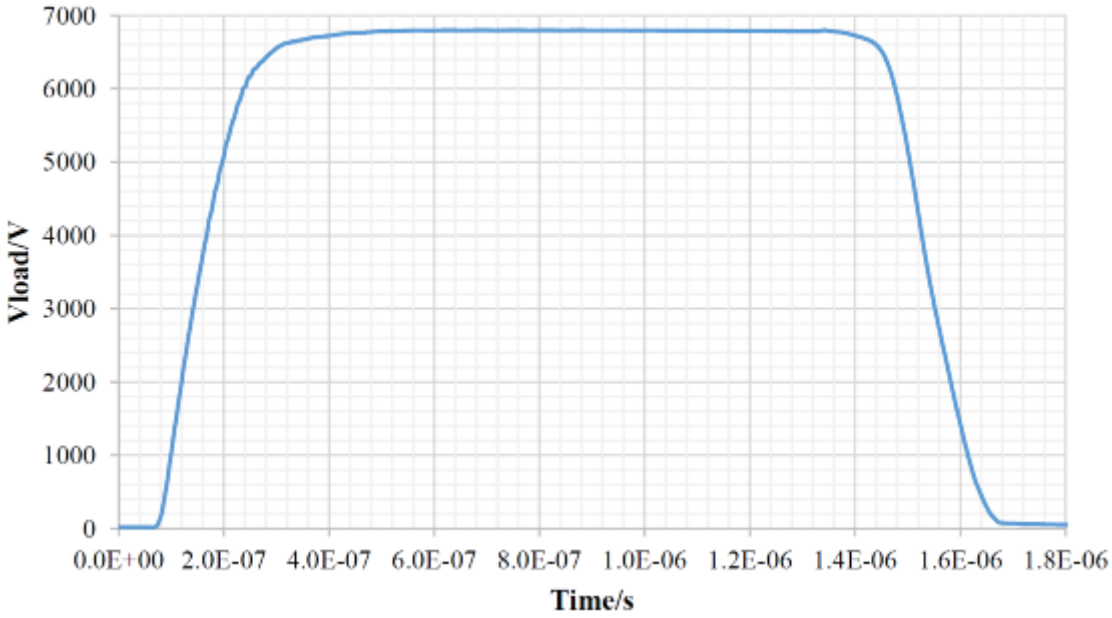
Design Parameter	20-Layer Full-Scale Prototype	CLIC DR Extraction Kicker Modulator
Output Voltage (kV)	**12.5**	12.5
Output Current	**308***	250
Voltage per layer	**700**	700
Number of layers	**20**	20
Pulse flat-top duration (ns)	**1100**	160 – 900
Pulse rise time [0.1-99.9 %] (ns)	**100**	< 1000
Pulse fall time [0.1-99.9 %] (ns)	**100**	< 1000
Flat-top stability (for 900* ns)	**≤ ±0.02 %**	±0.02 %
Flat-top repeatability (for 900* ns)	**≤ ±0.01 %**	±0.01 %

*Stripline odd-mode impedance 40.5 Ω



Prototype 4: Pulse without Modulation

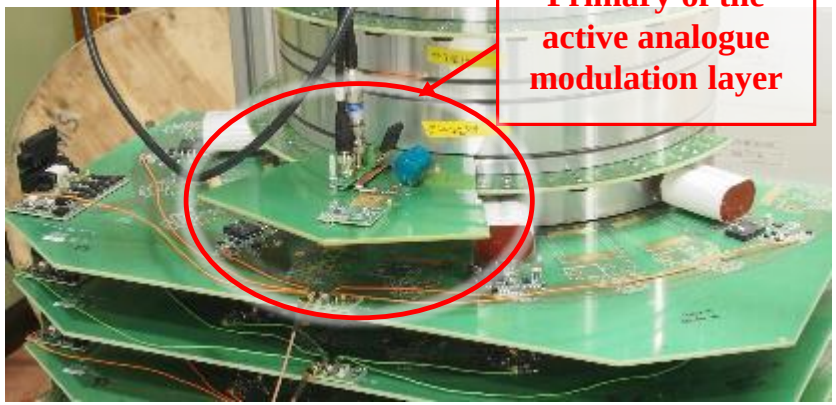
Height
120 cm

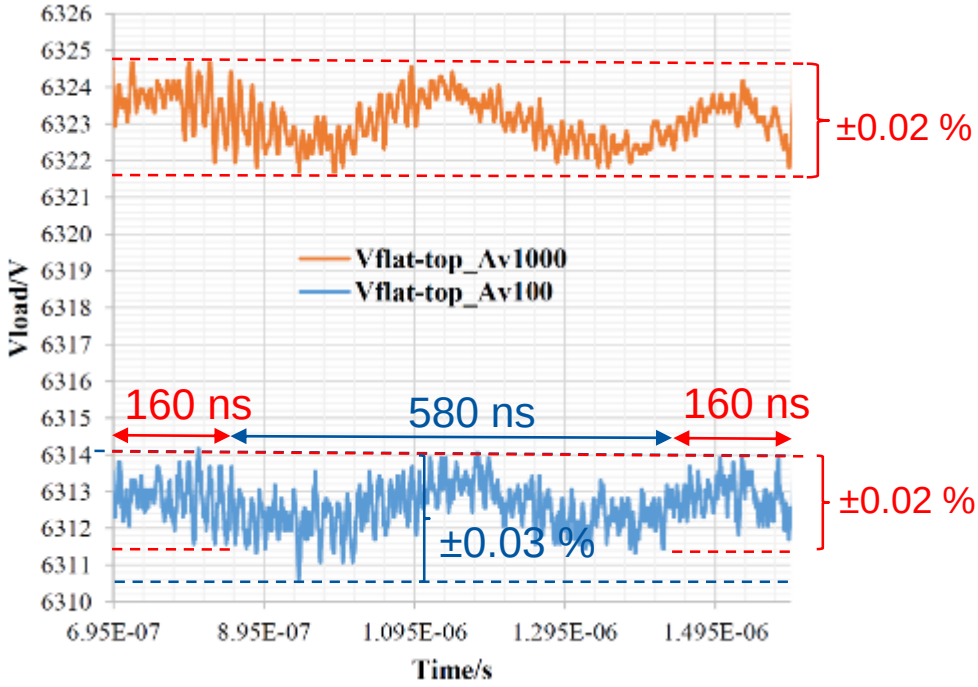


- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 10 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 µF/layer) initially charged to 700 V.
  - **No modulation applied**
  - **Output voltage 6.8 kV, droop ~15 V for 600 ns.**

⇨ Flat-top stability w/o compensation: ±0.1 % (±8.0 V) over 800 ns, at 6.8 kV

Prototype 4: Flat-top Pulse, with Modulation





- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 17 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 µF/layer) initially charged to 400 V.
  - **1 active analogue modulation layer**
  - **Active compensation of droop and ripple**
  - **Output voltage 6.3 kV**

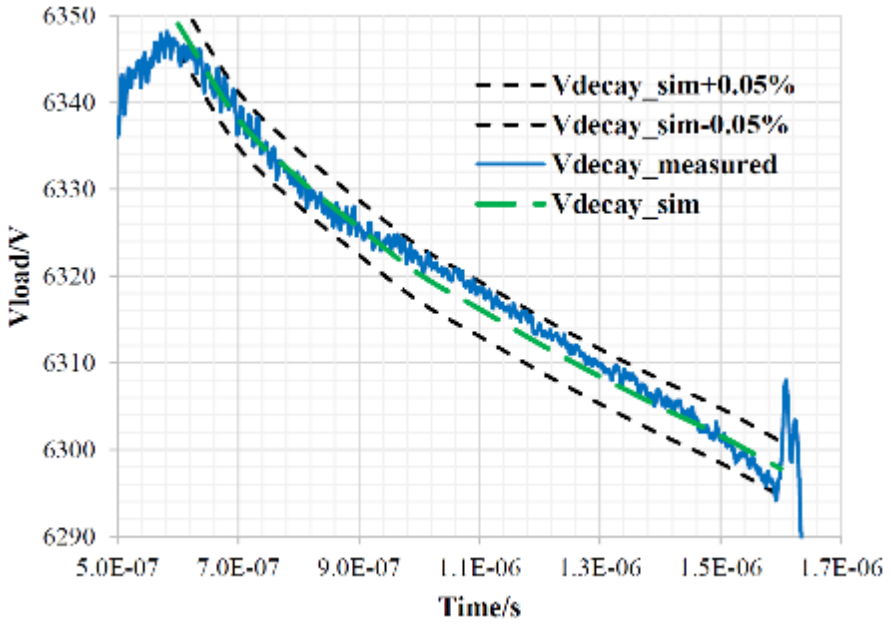
⇨ **Until recently, the specifications called for a ”flat-top” pulse.**

⇨ **Manually tuned compensation, not yet fully optimised: could possibly be improved e.g. by applying frequency domain compensation, with Fast Fourier Transform analysis.**

⇨ **Flat-top stability: ±0.02 % (±1.6 V) over 900 ns at 6.3 kV: CLIC DR 1 and 2 GHZ specifications at a half of the nominal voltage.**

Prototype 4: Attempt at Optimum Controlled Decay Waveform

- **Setup for the measurement:**
  - 20-layer prototype inductive adder
  - 17 constant voltage layers, with half-layer PCBs
  - 4 branches powered per layer, capacitors (48 µF/layer) initially charged to 700 V.
  - **1 active analogue modulation layer**
  - **Active modulation applied to adjust the flat-top to a controlled decay**
  - **Output voltage 6.3 kV**



- **Maximum difference between the simulated, optimum waveform and measured waveform: ±0.1 % (±6.3 V) at 6.3 kV (a half of the nominal voltage).**
- **Manually tuned compensation, not optimised: can be improved e.g. applying frequency domain compensation, with Fast Fourier Transform analysis.**
- **Target for next measurements: maximum difference within ±0.02 % of the optimum decay waveform, according to CLIC DR kicker stability specifications.**

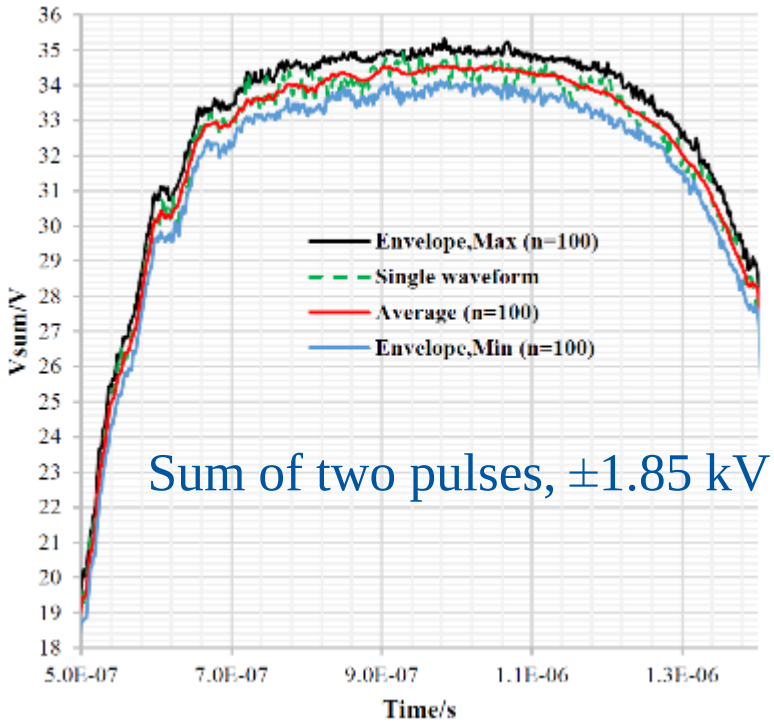
Measurement Techniques Applied for Testing CLIC DR Inductive Adders

- **Measurements shown in previous slides were carried out with a current tranformer and 16-bit (effective) high-end oscilloscope, i.e. with *direct electrical measurement*.**
- **Limits: channel noise of Rohde&Schwarz 16-bit (effective) oscilloscope RTO1004 is approximately ±0.2 % of the range (min/max envelopes for e.g. 100 pulses).**
- **Averaging (e.g. 100 or 1000 pulses) applied to filter out asynchronous, arbitrary, noise. However, it is impossible to define 1) stability of a single waveform, and 2) repeatability (min/max envelopes) if smaller than ±0.2 % of the channel range.**
- **Other techniques applied:**
  - **Pulse cancelling method**
  - **Balanced measurement setup (borrowed from PSI, Switzerland)**
- **Final measurements will be carried out with two full-scale prototype inductive adders powering a prototype stripline kicker installed in the beam line.**

Measurement Techniques: Pulse Cancelling

Setup for the measurement:

- 2 prototype inductive adders: one of the first 5-layer, 3.5 kV, prototypes and the new, full-scale, 5-layer, 3.5 kV prototype.
- 4 or 8 branches powered per layer, capacitors (24 µF pr 48 µF/layer) initially charged to 400 V
- **Output voltage of inductive adders: ±1.85 kV**
- **Sum voltage ~35 V.**
- **No Modulation**
- **16-bit (effective) oscilloscope**



Sum of two pulses, ±1.85 kV

- ⇨ Dynamic range of the waveform: ~350 V (during rise/fall times)
- ⇨ Min/max envelopes ±0.2 % (±0.9 V) over 900 ns: this is ±0.2 % x range, 400 V, of the channel!
- ⇨ **The min/max envelopes were dominated by oscilloscope noise.**

Measurement Techniques: Balanced Measurement Setup for measuring pulse-to-pulse repeatability

Balanced measurement setup: differential amplifier with a stable DC current source for a reference and fast clamping circuit to filter input signal when it is out of dynamic range.

Setup for the measurement:

- 5 constant voltage layers
- 1 Passive analogue modulation layer
- 4 branch powered per layer, capacitors (24 µF/layer) initially charged to 125 V
- **Passive compensation of droop**
- **Output voltage ~475 V (negative)**
- **Output voltage measured with a differentital amplifier, developed at PSI (M. Paraliev)**

- ⇨ Pulse-to-pulse stability (flat-top repeatability) measured by recording a mean and standard deviation of the mean for 105 pulses, for 900 ns pulse flat-top duration.
- ⇨ **Measured standard deviation σ = 0.49 mV, ±3.5 σ = ±1.7 mV at 475 V (±0.0004 %)**
- ⇨ **Flat-top repeatability ±0.0004 %= ±4 ppm, << ±0.01 % (CLIC DR ext. kicker requirement)**

- ⇨ Promising results for repeatability measurement, however relatively low voltage (~475 V).
- ⇨ The measurement setup was opitimised for sinusoidal waveform with a fixed frequency, therefore it is not clear how accurate it is for measurements on ”rectangular” pulses with fast rise times and wide bandwidth.
- ⇨ Another setup, with more optimised design for fast rectangular pulses, lent to CERN by PSI. To be tested shortly.

Summary

- **The specifications for the pulse power modulators for the CLIC DR kicker systems are very probably feasible with inductive adder technology.**
- Three 5-layer, 3.5 kV prototype inductive have been built and tested at CERN.
- First full-scale, 20-layer, 12.5 kV CLIC DR extraction kicker inductive adder has been built, and testing is on-going (tested up to 6.8 kV).
- Both passive and active analogue modulation methods tested to a) improve the flat-top stability of the waveforms and b) to adjust the output waveform for a controlled decay waveform.
- Generation of a controlled decay waveform is feasible without a design change (originally optimised for a flat-top)
- The best measured stabilities, with active droop and ripple compensation (not fully optimised):
  - ±0.02 % over 900 ns for a flat-top pulse at 6.3 kV (CLIC DR 1&2 GHz specifications at a half of the nominal voltage)
  - ±0.1 % over 900 ns for a “controlled decay waveform” at 6.3 kV.

Future Work

- Testing of the 1st full-scale protype wtih ~20 layers up to 12.5 kV.
- Improvement of waveform stability to ±0.02 % and repeatability to ±0.01 % for 900 ns.
- Assembly of the 2nd full-scale, 20/28-layer, prototype: combined 12.5 kV/17.5 kV extraction kicker + dump kicker modulator.
- Revision of half-layer PCBs (Mainboards)
  - Cross-talk problems between HV and trigger lines (false post-pulse triggering)
  - Upgrades for short-circuit & over-current protection circuits.
- Design of LabVIEW-based automated waveform correction control system for inductive adders: first hardware setup available for programming and testing.
- Measurements with balanced measurement setup (from PSI, Switzerland) for evaluating repeatability (and possibly stability) with improved resolution in comparison with direct CT measurements.
- Testing of 50 Ω & 425 Ω HV terminating loads, designed at CERN.
- Future measurements of two 12.5 kV inductive adders with a stripline kicker installed in a beamline in an accelerator test facility (at ALBA Cells in Spain, in 2018).
- Much interest for inductive adder technology at CERN, regarding e.g. FCC and PS KFA kicker systems.

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12. Holma J., Barnes M.J.: “Evaluation of Components for the High Precision Inductive Adder for the CLIC Damping Rings”, Proc. of IPAC 2012, New Orleans, USA, May 20-26, 2012.
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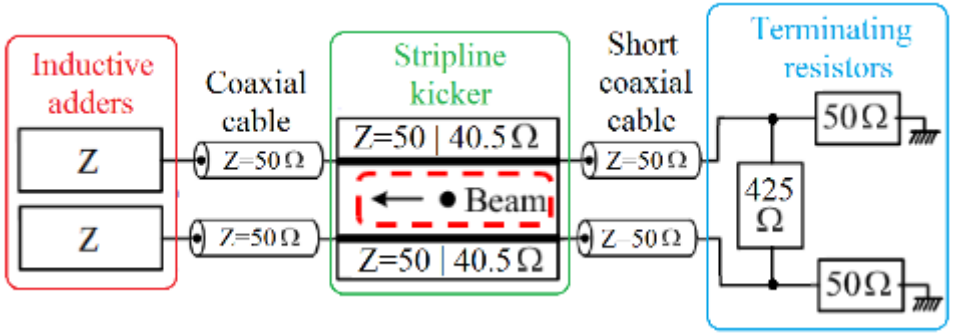
CERN

Spares and extras

Specifications for CLIC DR Extraction Kicker Systems

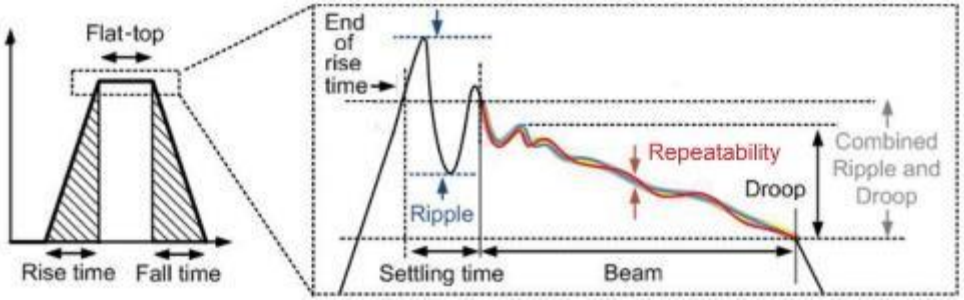
	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (per Stripline)	±12.5 kV
Stripline pulse current [40.5 Ω load]	±309 A
Repetition rate	50 Hz
Pulse flat-top duration *900 ns = 160 ns + 580 ns gap + 160 ns	~160 ns | ~900* ns
Flat-top repeatability	$\pm 1 \times 10^{-4}$ (±0.01 %)
Flat-top stability [droop+ripple]	$\pm 2 \times 10^{-4}$ (±0.02 %)
Field rise time	1000 ns (max.)
Field fall time	1000 ns (max.)
Beam energy	2.86 GeV
Total kick deflection angle	1.5 mrad (0.09 deg)
Aperture	20 mm
Effective length	1.7 m
Field inhomogeneity [1 mm radius]	±0.01 %

- **Extremely tight requirements for flat-top stability and repeatability!**
- **For rise/fall times, ≤ 100 ns desired.**



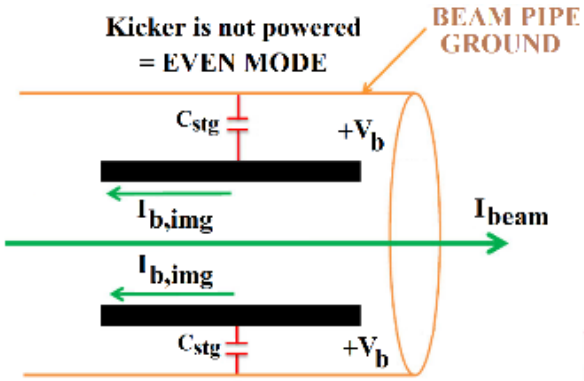
Simplified schematic of a CLIC DR stripline kicker system

- **Stripline kicker: two electrodes, powered with opposite polarities**
- **Both electric and magnetic fields deflect the beam.**

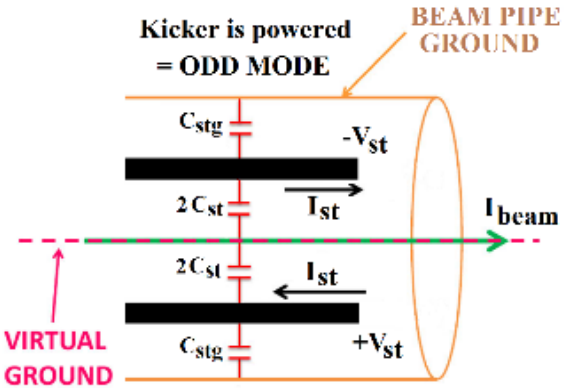


CLIC DR kicker pulse definition

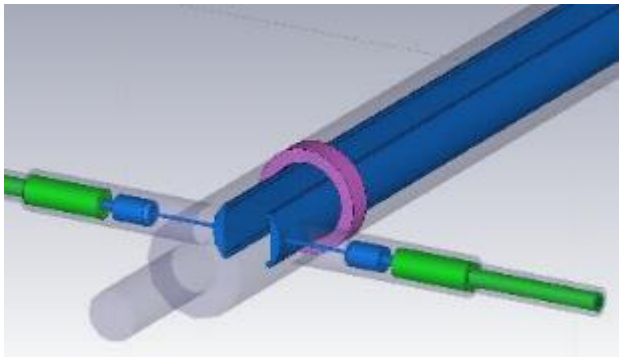
Specifications for the CLIC DR Extraction Kicker Modulators: *Waveform* stability & repeatability



"Kicker off": Z = 50 Ω



"Kicker on", Z = ~40.5 Ω



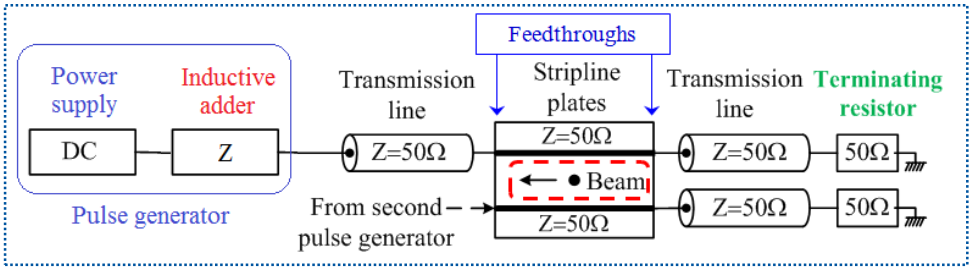
3D model of the CLIC DR stripline electrodes

- **Stripline kicker: both electric and magnetic fields deflect the beam.**
- **Impedances of the striplines are 50 Ω when "off" and 40.5 Ω when "on": both modes are matched with a terminating resistor network.**
- **The total deflecting angle for particles in each bunch during a single kick should be the same.**
- **According to optimization studies of the CLIC DR prototype stripline kicker (by C. Belver-Aguilar), the impedance of the kicker does not remain unchanged during the pulse: in order to generate the same deflection for each bunch, the voltage and current need to be modulated.**
- **The optimum waveforms for two stripline electrodes are identical "controlled decays": these generate a constant "flat-top" for total deflecting field.**

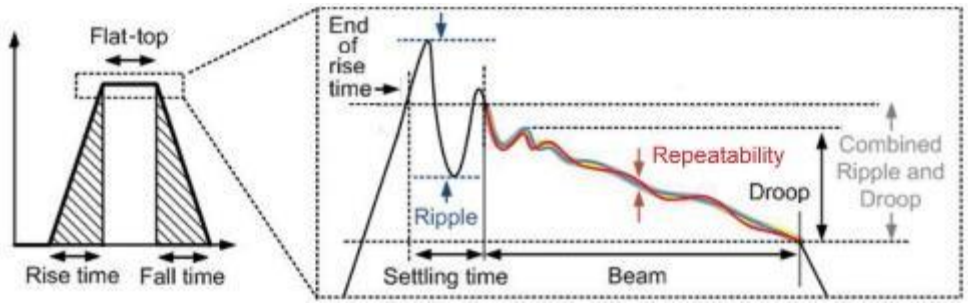
Specifications for CLIC DR Extraction Kicker Systems

	CLIC DR (1 GHz | 2 GHz)
Pulse voltage (per Stripline)	**±12.5 kV**
Stripline pulse current [40.5 Ω load]	**±309 A**
Repetition rate	**50 Hz**
Pulse flat-top duration *900 ns = 160 ns + 580 ns gap + 160 ns	**~160 ns | ~900* ns**
Flat-top repeatability	**±1x10^{-4} (±0.01 %)**
Flat-top stability [droop+ripple]	**±2x10^{-4} (±0.02 %)**
Field rise time	**1000 ns**
Field fall time	**1000 ns**
Beam energy	2.86 GeV
Total kick deflection angle	1.5 mrad (0.09 deg)
Aperture	20 mm
Effective length	1.7 m
Field inhomogeneity [1 mm radius]	±0.01 %

- **Extremely tight requirements for flat-top stability and repeatability!**
- **For rise/fall times, ≤ 100 ns desired.**



Simplified schematic of a kicker system



CLIC DR kicker pulse definition

Prototype CLIC DR extraction kicker (Courtesy of C. Belver-Aguilar)

Measurement Techniques Applied for Testing CLIC DR Inductive Adders

- **Measurements shown in previous slides were carried out with a current tranformer and 16-bit high-end oscilloscope, i.e. with *direct electrical measurement*.**
- **Limits: channel noise of Rohde&Schwarz 16-bit oscilloscope RTO1004 is approximately ±0.2 % of the range (min/max envelopes for e.g. 100 pulses).**
- **Averaging (e.g. 100 or 1000 pulses) applied to filter out asynchronous, arbitrary, noise. However, it is impossible to define 1) stability of a single waveform, and 2) repeatability (min/max envelopes) if smaller than ±0.2 % of the channel range.**
- **Other techniques applied:**
  - **Pulse cancelling method: pulses from two (almost) identical inductive adders, with opposite polarities, measured with a single current transformer. The reading from the current measurement is the net pulse, i.e. the difference of wo pulses. The dynamic range of the measurement was only decreased by factor of ~5, because rise times of the pulses were not prefectly mathced.**
  - **Balanced measurement setup (borrowed from PSI, Switzerland): a differential amplifier with a stable current reference and fast clamping circuits to filter the input signal when it is out of dynamic range. The setup was originally tuned for a sine wave, therefore the results are preliminary. Best measured flat-top repeatability (standard deviation of a mean) was ±0.0004 % (±4 ppm) over 900 ns pulse duration, measured for 105 pulses at 475 V output voltage.**
- **Final measurements will be carried out two full-scale prototype inductive adders powering a prototype stripline kicker installed in the beam line.**