

For ANY amplifier, power supply ripple will find it's way into the signal chain suppressed by PSRR

- Opamp \rightarrow PSRR very high ~ 10⁻⁵ (- 100db or better)
- Nfet based charge amplifier \rightarrow Modest ~10⁻³ (-60 db, my estimate)
- Pfet based charge amplifer \rightarrow Not suppressed \rightarrow PSRR ~1 (0 db)

Amplifier configured as a charge integrator (VMM)





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$$V_{out} = (PSRR) * V_r * (1 + C_d/C_f) * Gain$$

or stated in terms of equivalent input charge (enc) for VMM (PSRR ~ 1)

- Enc ~ $V_r^*C_d$
- Example: for $V_r = 1 uV$, $C_d = 200 pf$ (Micromegas strip)
 - enc ~ 1,200 electrons (0.2 fc)
 - For Gain = 10 mV/fc \rightarrow V_{mo} ~ 2 mV

[For more complete analysis, see "*Impact of Power Supply Ripple on Front End Resolution*" Gianluigi DG, 17-Jan-17 https://indico.cern.ch/event/598168/



Takeaway

- Acceptable ripple on $V_{MO} \sim 1mV 2mV$ (From George Iakovidis)
- For Micromegas, this requires $V_{ripple} < 1 uV$
- Is it possible for V_{MO} to be worse than this, even if Vripple < 1uV?
 - Yes, of course if other mechanisms present, but it can't be better.

Tests at BNL, Jan 2017

- Two day workshop with MMFE8 & small MM chamber
- Myself, Gianluigi, George, Lorne, Vinnie, & Tech from U. A.
- Vddp measured directly with soldered in cable (no scope probe)
- $V_{ripple} \sim 130 \text{ uV}$ (not visible without signal averaging)
- $V_{ripple} > 100x$ too high
 - V_{MO} > several 100 mV @ DC/DC converter frequency (~ 1.2 MHz)

Conclusions

- V_{ripple} must be reduced by more than 100x to ~ 1uV
- Can this be done with DC/DC converters on board?
 - IMHO, probably not but no harm in trying
 - We should certainly look at possibility of removing DC/DC converters from FEBs