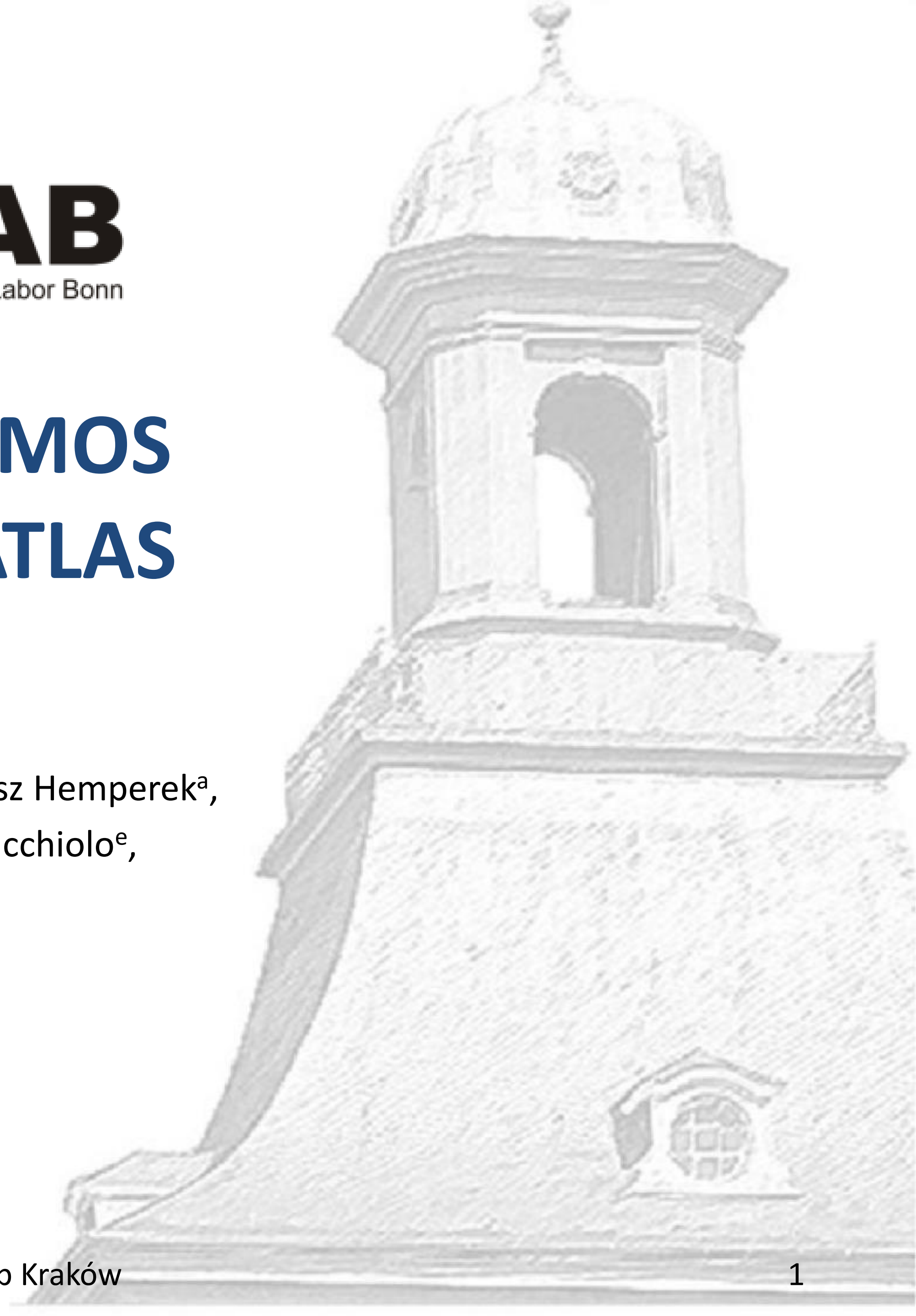
3D-silicon and passive CMOS pixel-detectors for the ATLAS pixel detector upgrade

David-Leon Pohl[a], Cinzia da Via[c], Laura Gonella[b], Tomasz Hemperek[a], Fabian Hügging[a], Jens Janssen[a], Hans Krüger[a], Anna Macchiolo[e], N. Owtscharenko[a], Luigi Vigani[d], and Norbert Wermes[a]

a Physikalisches Institut der Universität Bonn
b School of Physics and Astronomy, University of Birmingham
c School of Physics and Astronomy, University of Manchester
d Department of Physics, University of Oxford
e Max-Planck-Institut für Physik, München



pohl@physik.uni-bonn.de

Motivation

Large **H**adron **C**ollider in 2025: 5-8 x increased particle rate:
→ New, all silicon inner tracker for ATLAS experiment [1]

Main challenges for a hybrid silicon detector concept

Inner layer

Radiation hardness
- TID: 2 MGy → 7.7 MGy
- NIEL: $0.5 \cdot 10^{16}$ N_{eq}/cm^2 → $1.4 \cdot 10^{16}$ N_{eq}/cm^2

?

3D sensors
- Complex technology:
  - 150 mm wafers
  - Low yield / High price
  - Limited production capability
- **Feature: Very radiation hard**

Outer layers

Area
- 64 m² → 175 m²
- Production (hybridization, testing, volume)

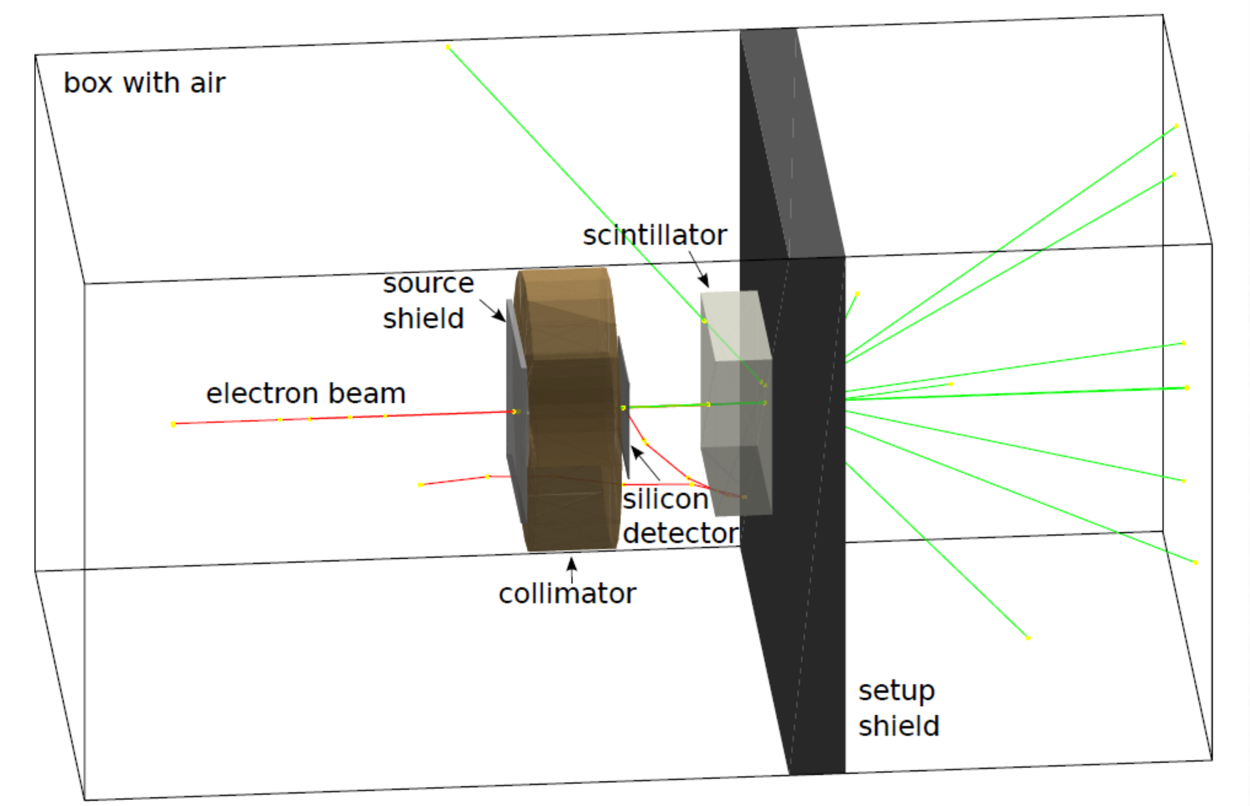
?

Passive sensor in CMOS technology
- Industrial technology:
  - 200 mm wafers
  - High yield / Low price
  - Very high production capability
- **Feature: CMOS process technologies**:
  - AC coupling
  - Many metall layers for power/data redistribution layer(s) → module simplification

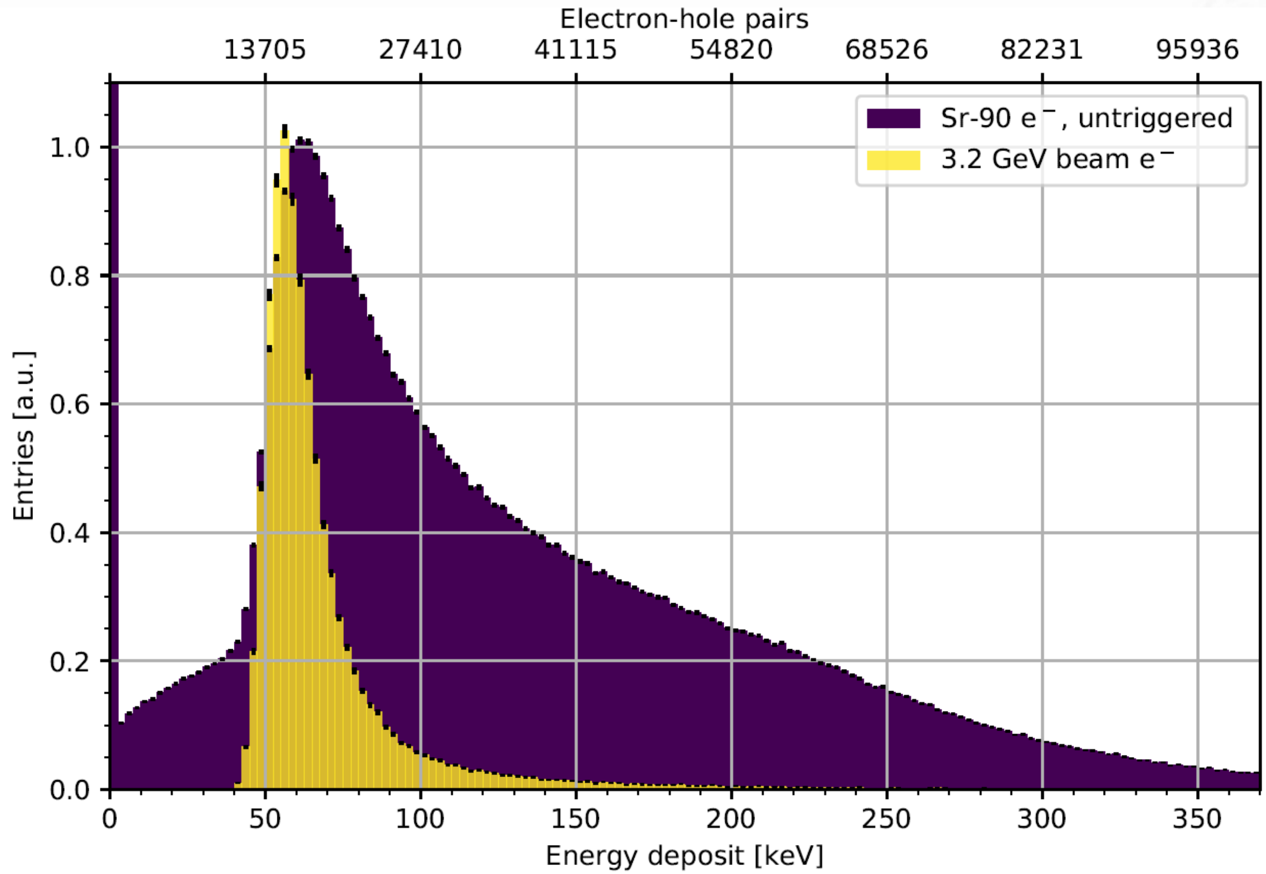
[1] CERN-LHCC-2012-022

Landau measurements: β sources + segmented detectors

- GEANT 4 simulation **SourceSim** (https://github.com/SiLab-Bonn/SourceSim)
- Different setups possible:
  - Trigger, collimator, shields
  - Sensor geometry (meterial, thickness, pixel pitch)
  - Sources (X-ray, Sr-90, MIPs)
- Digitization: charge sharing via 3D Gaussian model, threshold, noise and data driven MC for IBL modules



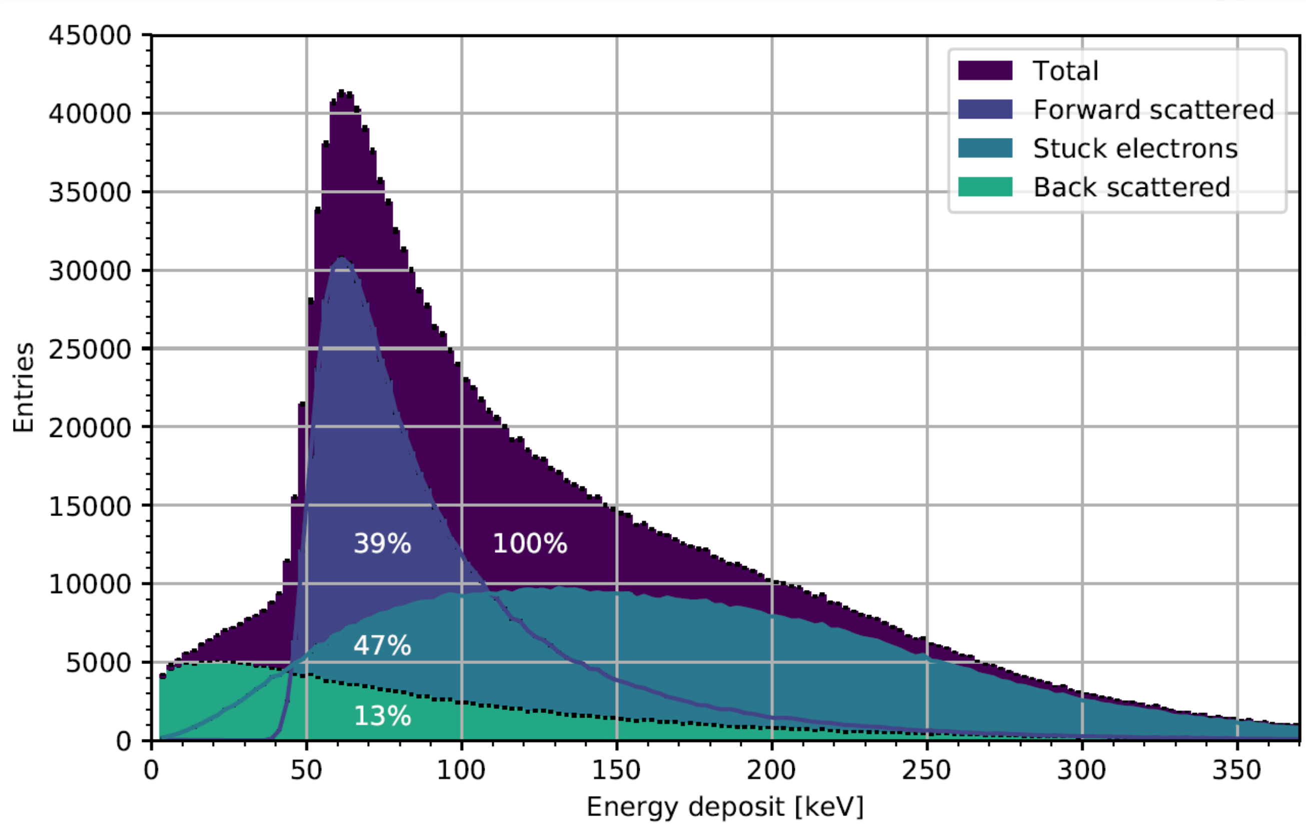
Charge spectra in silicon diodes: MIP vs. Sr-90



SourceSim parameters
- Silicon planar diode
- 200 um thickness
- 2 x 2 cm plane
- No initial beam angle
- No digitization

- 3.2 GeV electrons: **Landau shape** for MIP beam
- Sr-90 electrons: **Broad Landau** like shape with long tail and background

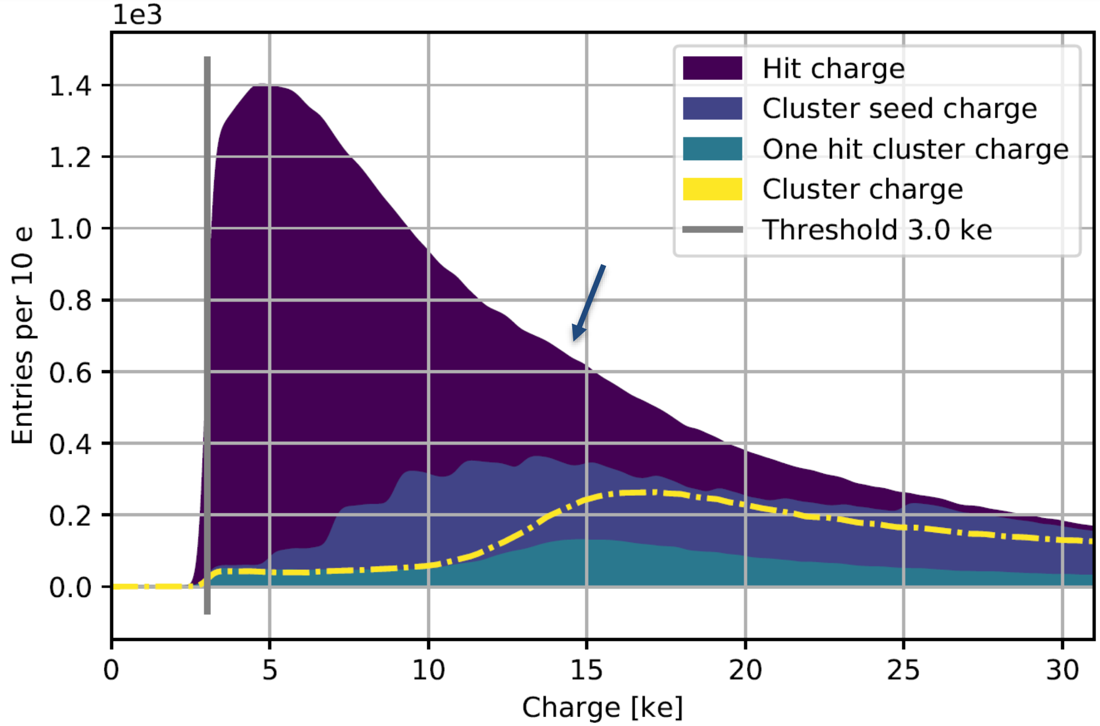
Charge spectra in silicon diodes: Sr-90 with different cuts



SourceSim parameters
- Silicon planar diode
- 200 um thickness
- 2 x 2 cm plane
- No initial beam angle
- No digitization

- **Background from scattered particles**:
  - Stuck and back scattered electrons: ~60 %
  - Traversing electrons: ~ 40%, Landau like shape → triggering usefull to select these, but not mandatory

Charge spectra in segmented silicon detectors, untriggered

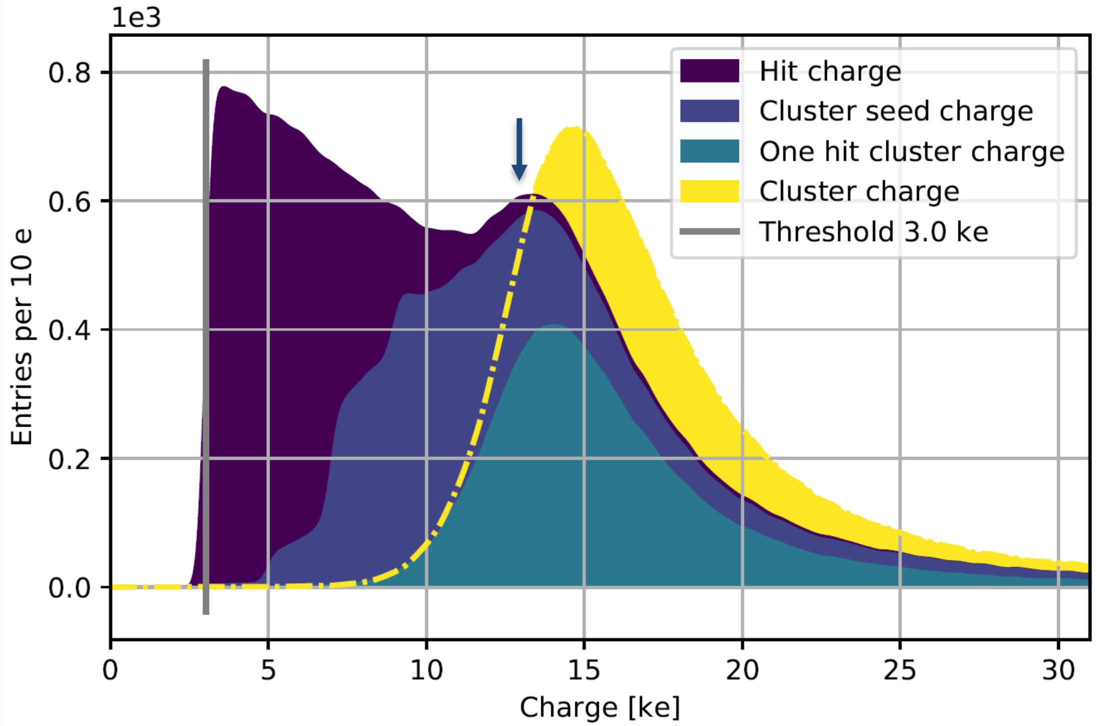


SourceSim parameters
- Sr-90 electron source
- Silicon pixel detector
- ATLAS IBL geometry
  - Planar geometry
  - 200 um thickness
  - 80 x 336 pixel
  - 250 um x 50 um
  - 2 x 2 cm plane
- Digitization:
  - 3000 e threshold
  - 120 e noise
  - Charge sharing
  - T = 300 K
- E-h pair = 3.65 eV
- No initial beam angle

- **Singel channel** distribution (Hit charge): **no fitable Landau MPV** due to scattering in sensor (arrow), depends on pixel geometry (pitch vs. depth) and collimation of source

  → Clustering mandatory: **one hit cluster or cluster charge should be used** (more narrow distribution)
- **Seed charge is broader** due to larger „charge sharing“, one step in distribution per cluster size
- Very broad Landaus give large errors on MPV fits

Charge spectra in segmented silicon detectors, triggered



SourceSim parameters
- Sr-90 electron source
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- ATLAS IBL geometry
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  - 200 um thickness
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  - 2 x 2 cm plane
- Digitization:
  - 3000 e threshold
  - 120 e noise
  - Charge sharing
  - T = 300 K
- E-h pair = 3.65 eV
- No initial beam angle

- **Singel channel** distribution (Hit charge) has **hardly fittable Landau MPV** due to scattering in sensor (arrow), depends on pixel geometry (pitch vs. depth) and collimation of source
- **Cluster charge** and **one hit cluster** charge show **nice Landau like distributions**

SourceSim: Comparison with data

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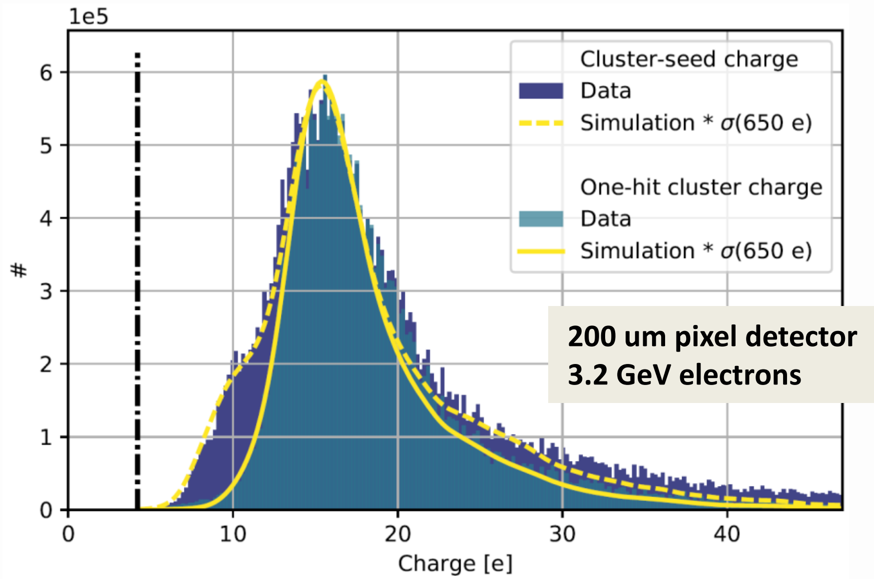
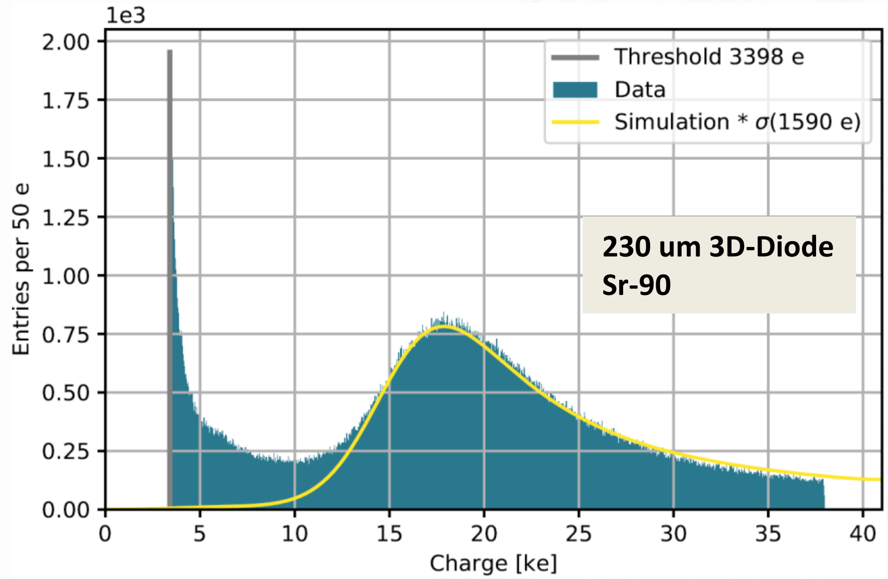
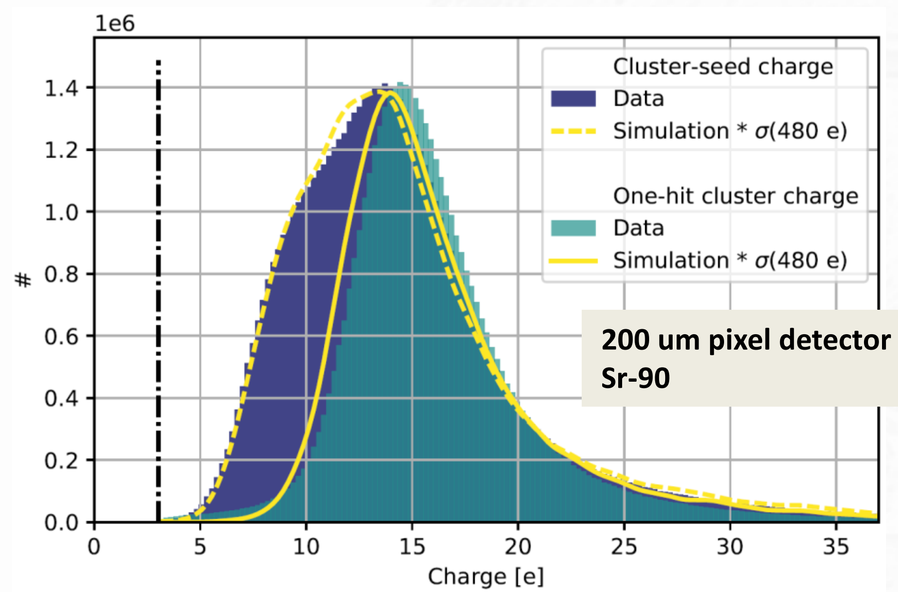




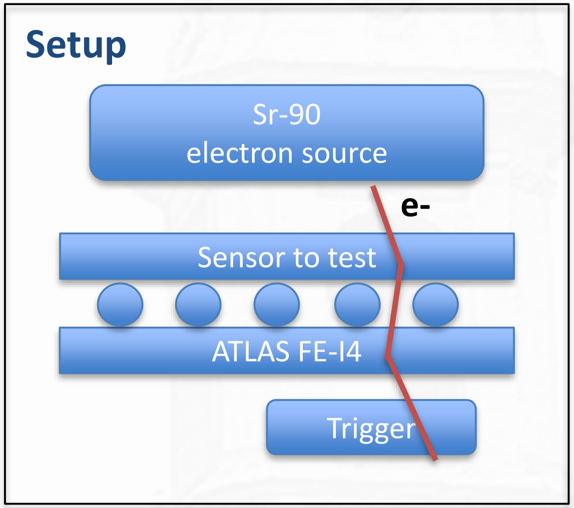
- **3.2 GeV: Measurement and simulation match** (source easy to model: no angular and energy distributions)
- **Sr-90: good agreement**, can be improved (source model is simplified: angular and energy distributions approximated)
- Summary:
  - Sr-90 deposites more charge than MIP in silicon layer, but less charge per channel (strip, pixel) → should not be used to deduce absolute values (e.g. depletion depth)
  - Triggering reduces Landau width → increases MPV fit resolution
  - Clustering (often) needed to get fittable peak
  - Constant setup for relative measurements needed



SourceSim parameters
As before but data driven MC digitizazion to simulate readout electronic response

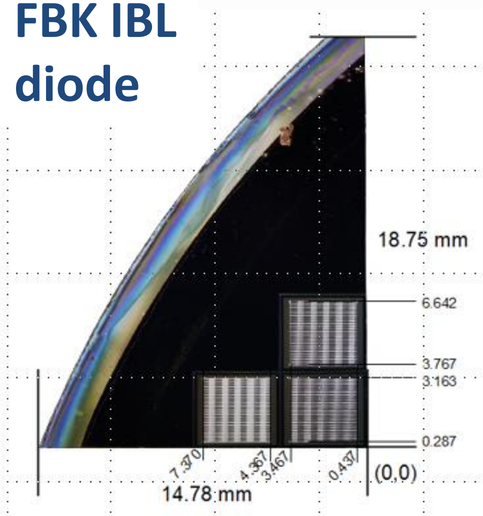
Measurement procedure

- **Constant setup in fridge**
- **ATLAS pixel detector modules / diodes from production [2]**:
  - ATLAS-FE I4 readout chip; 50 um x 250 um pixels
  - N-in-n planar sensors; thickness: 200 um/250 um
  - N-in-p 3D sensors from FBK/CNM; thickness 230 um
  - N-in-p 3D sensor diodes from FBK, shorted pixel matrix
- **Successive irradiation** with 24 MeV Protons to **$7 \cdot 10^{15}$ N_{eq}/cm^2**
- **Annealing after each step:** 80 min @ 60° C

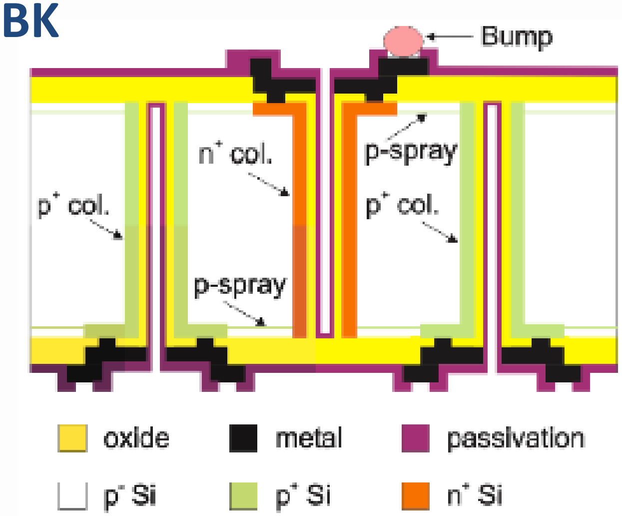


[2] Prototype ATLAS IBL modules using the FE-I4A front-end readout chip

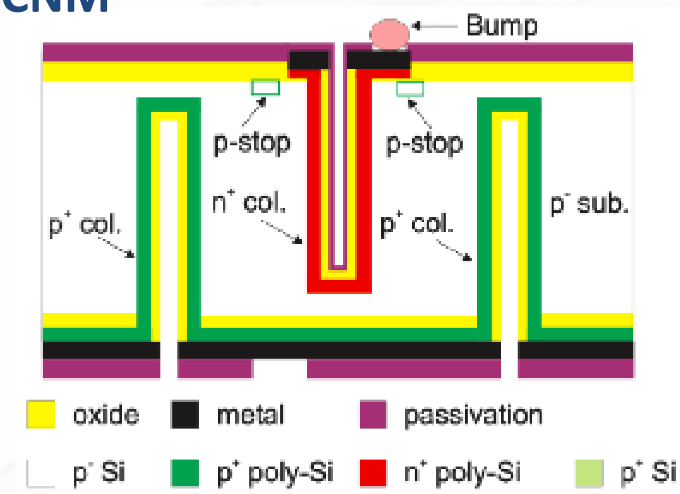
FBK IBL diode



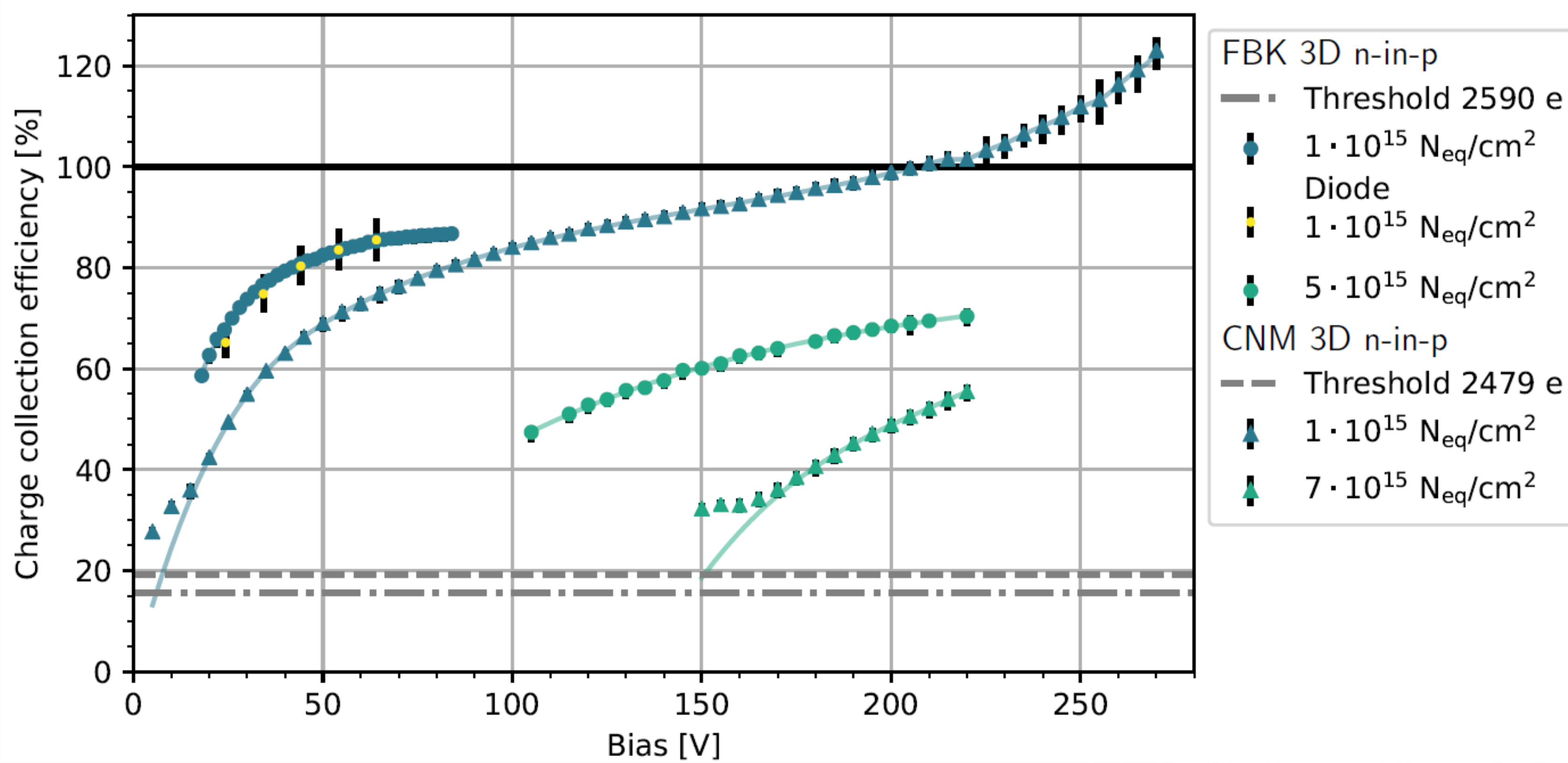
FBK



CNM



Charge collection efficiency: IBL 3D modules / diode



[3] Aaron Mac Raighne et al., Physics Procedia 37 (2012) 1016 – 1023

- **Independent measurement** pixel module / diode show **same results**
- **Very different behavior for FBK/CNM**, likely because columns not fully through in CNM design
- **Charge multiplication** for CNM (in high field regions, cannot be used to enhance efficiency, [3])
- CCE > 55 % for 7 $\cdot 10^{15}$ N_{eq}/cm^2

Charge collection efficiency: IBL modules

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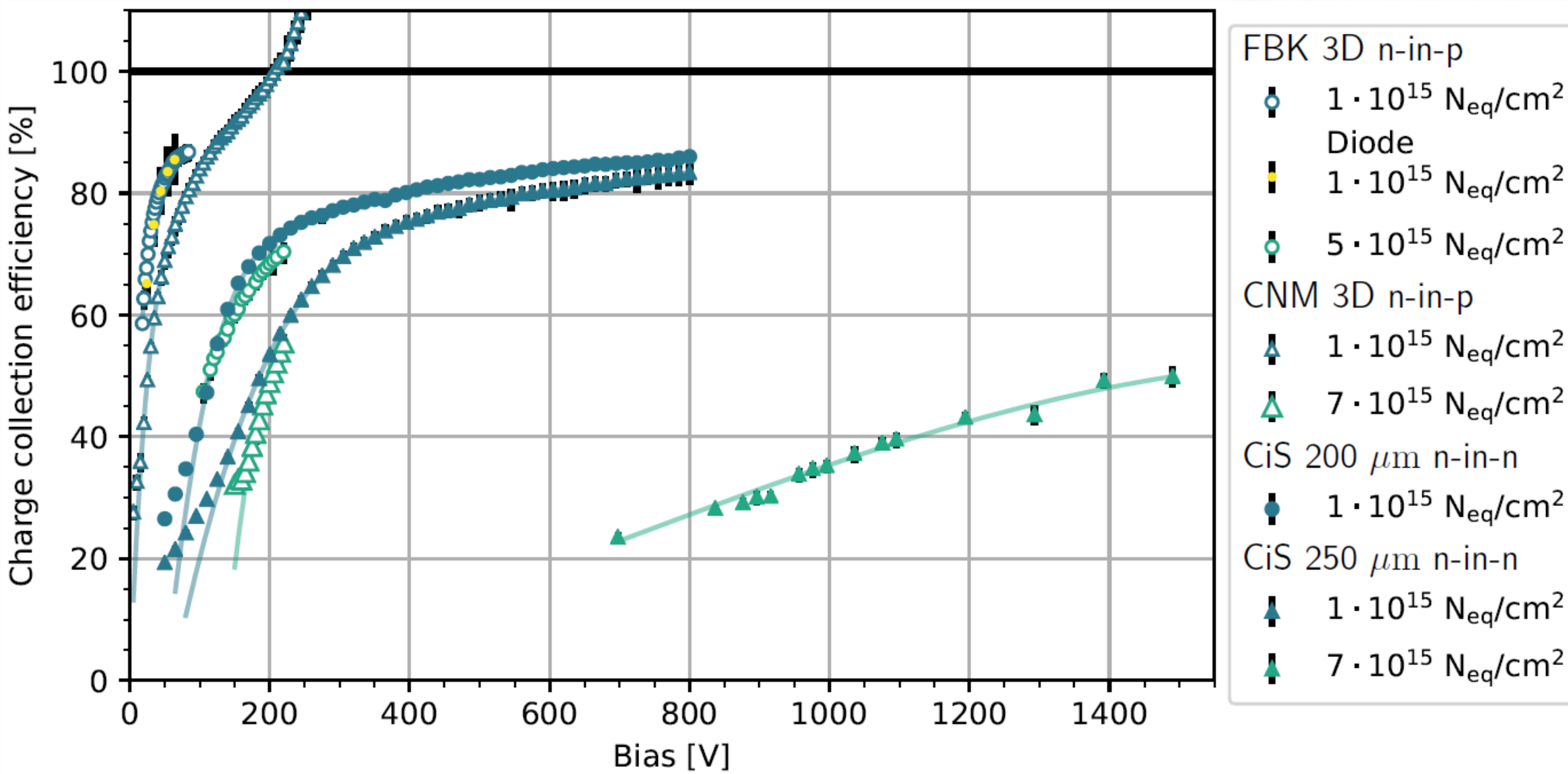
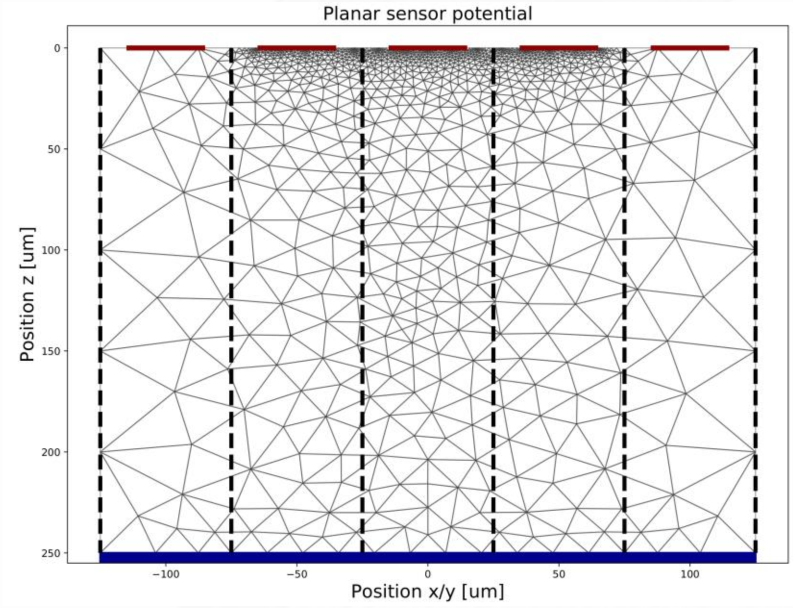
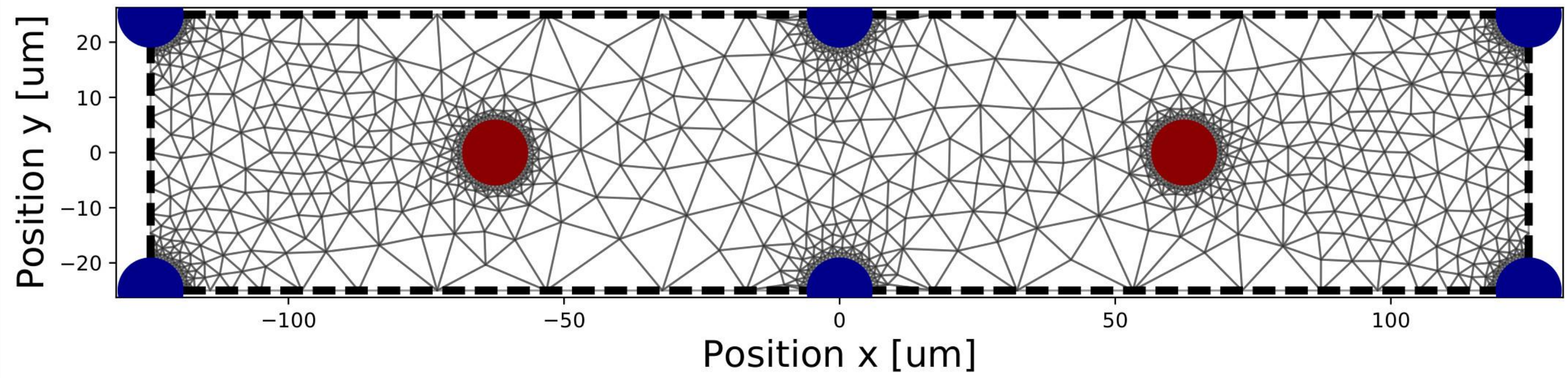


- **Thinner** planar sensor shows **higher CCE**
- 250 um planar sensor has 50 % CCE at $7 \cdot 10^{15}$ N_{eq}/cm^2 at very high bias V=1500, no break down
- But: **Power consumption 4 x higher than 3D for same CCE**

Simulation of Charge Collection Efficiency with SCARCE

- Simulation with new Python package: **SCARCE** (https://github.com/SiLab-Bonn/Scarce)
- Based on:
  - **Gmesh**: A three-dimensional finite element mesh generator
    - About 400k nodes (Reduced by O(100) for plotting)
    - Increased density at high E-Field gradients
    - Increased density in pixel under tests
    - Ability to store and load precomputed fields





Simulation of Charge Collection Efficiency with SCARCE

– FiPy: **Finite Volume PDE Solver** from NIST (http://www.ctcms.nist.gov/fipy/) for potentials

Weighting potential

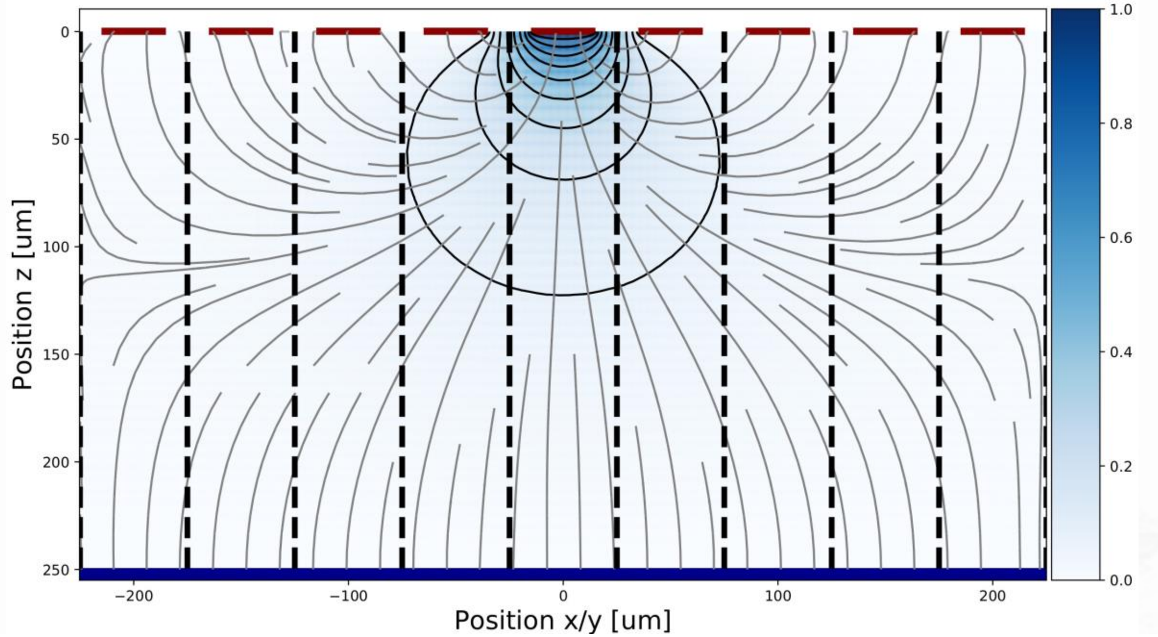
$$\nabla^2\Phi = 0$$
$$\Phi_b = 0, \Phi_r = 1$$

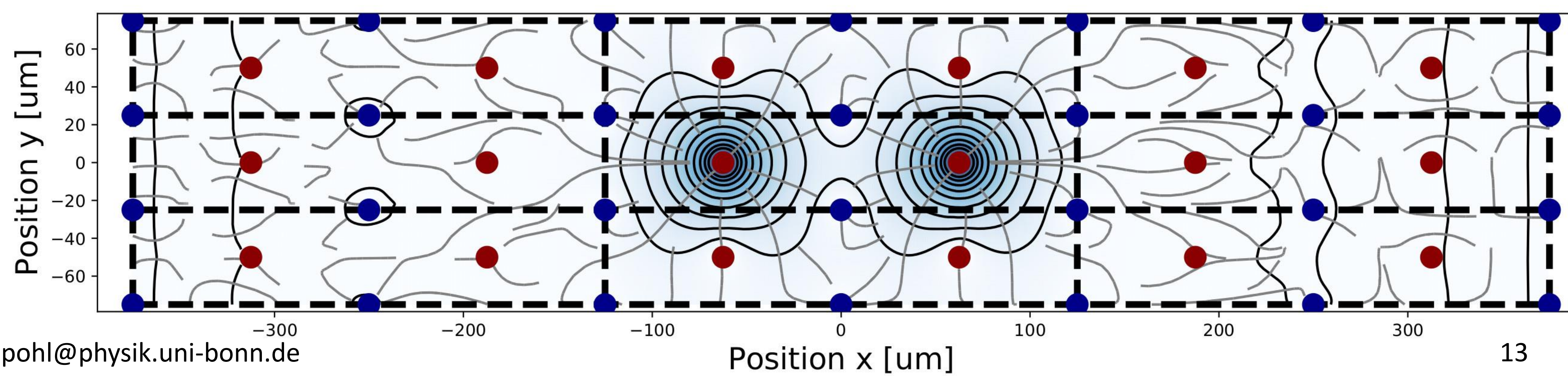
- Surrounding pixels for correct boundaries needed!

Weighting field

$$\vec{E} = -\nabla\Phi$$

- Numerical differentiation after smoothing





Drift and diffusion

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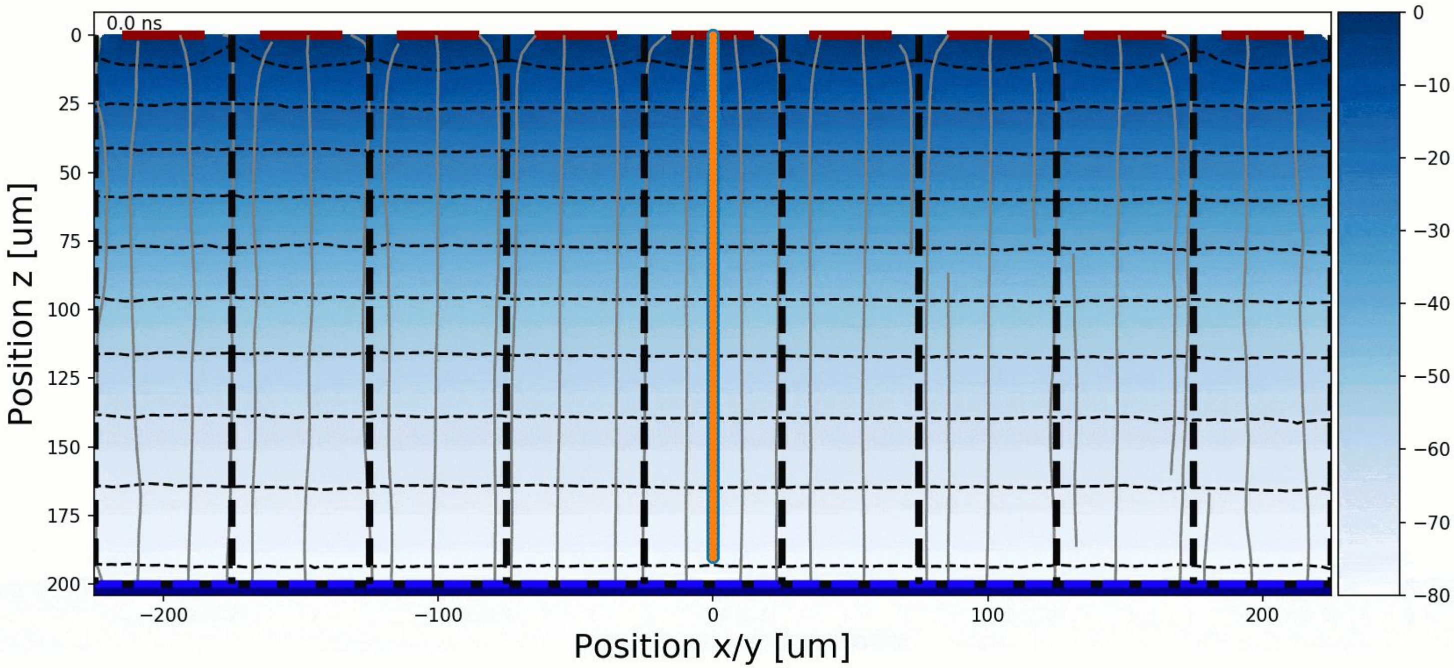
Movement

$$v_{e,h} = v_{\text{drift}} + v_{\text{diffusion}}$$

$$v_{\text{drift}} = v_m \frac{(|E|/E_c)}{\left[1+(|E|/E_c)^{\beta}\right]^{1/\beta}} \text{ [4]}, \quad v_{\text{diffusion}} = \left(\frac{3k_B T}{m_{\text{eff}}}\right)^{\frac{1}{2}} \text{ [5]}$$

Collected charge

$$Q_{\text{tot}} \sim \int_{t=0}^{t_{\text{coll}}} e^{-\frac{t}{\tau}} \cdot v_{e,h}(t) \cdot \vec{E}_w(\vec{x}(t))\, \text{dt}$$



[4] C. Jacononi et al., Solid state electronics, 1977, vol 20., p. 87
[5] Manhee Jeong, IEEE VOL. 56, NO. 3, JUNE 2009

Data vs. simulation: CCE IBL FBK 3D sensor

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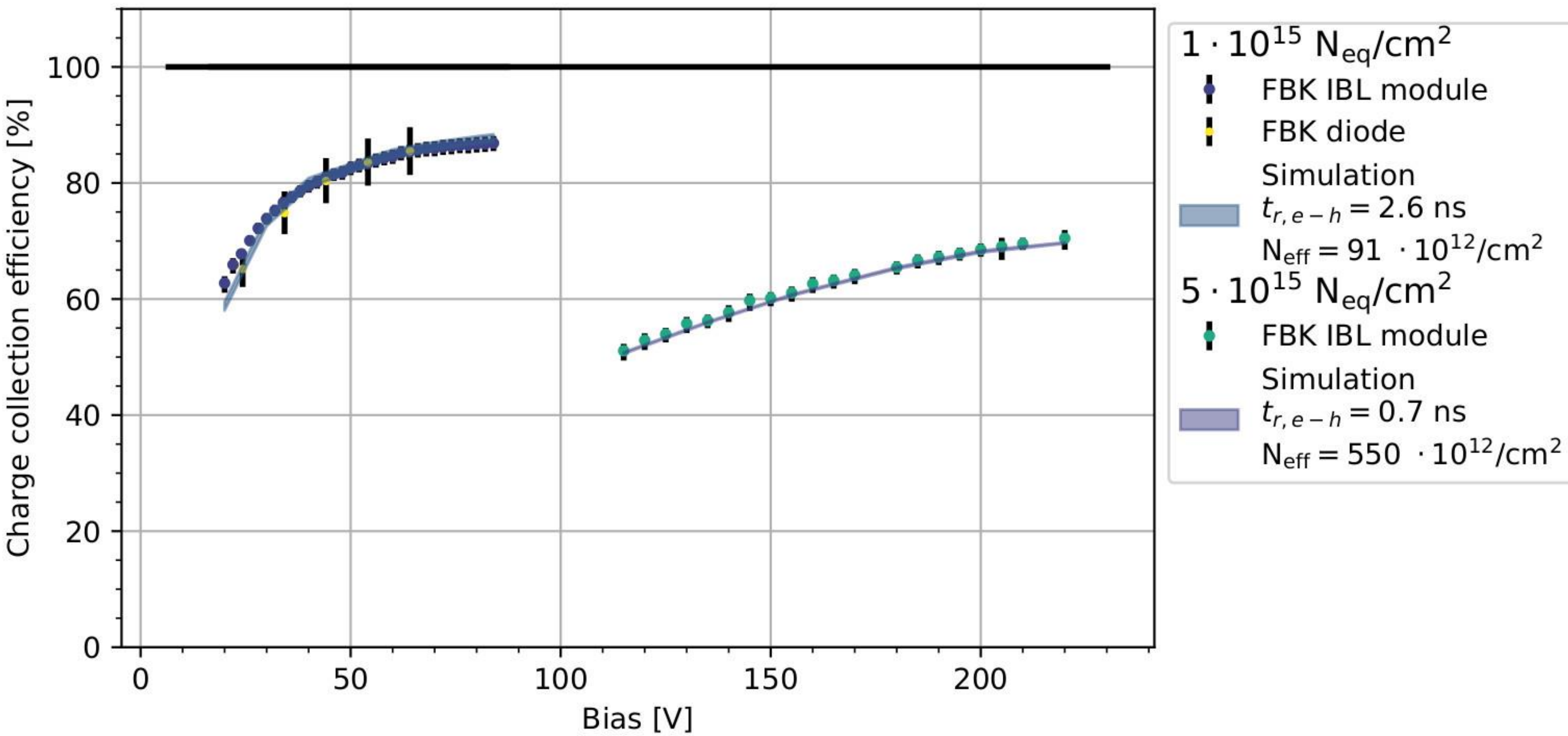
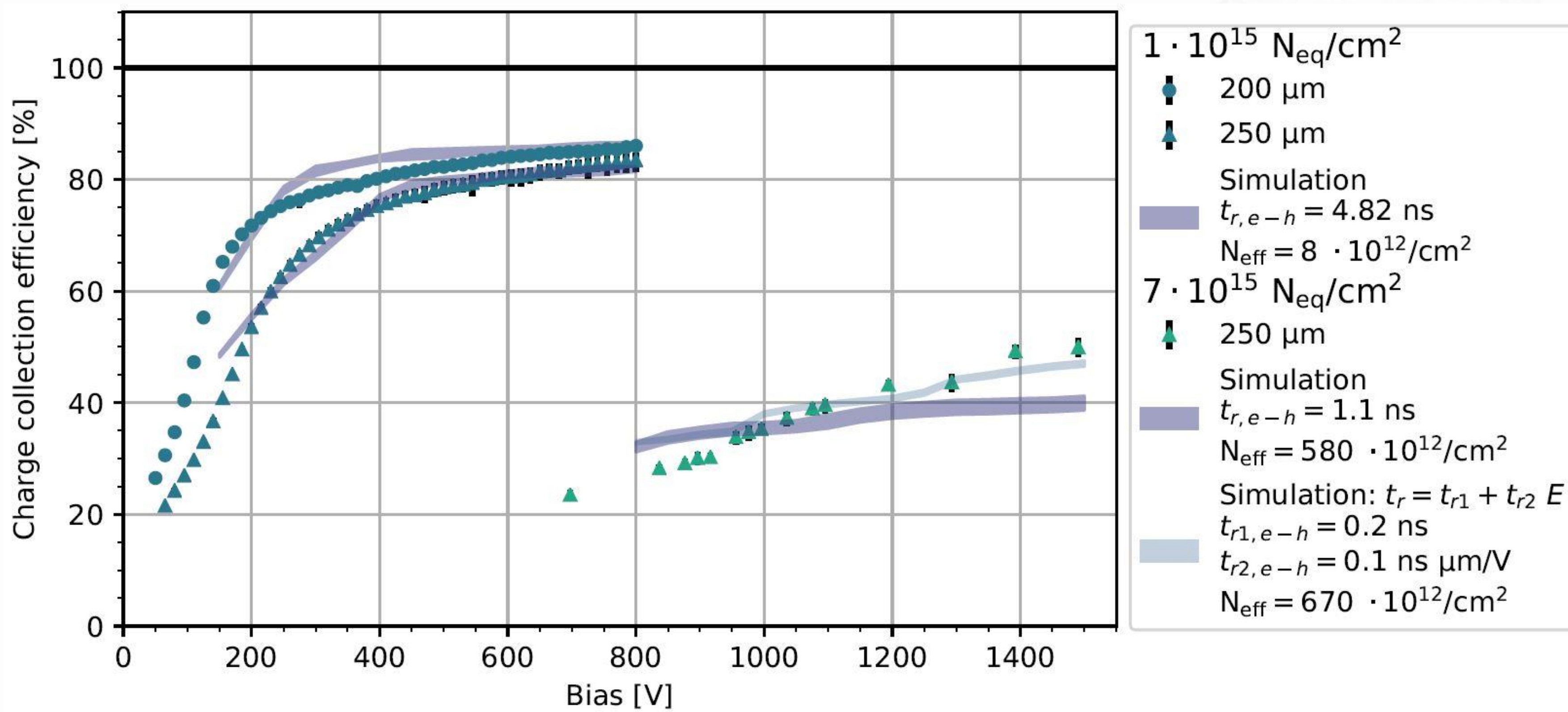


- **N_{eff}, t_r optimized by χ^2scan** on Bonn computational grid
- Simulation error: RMS of repeated scans with same „optimal“ input parameters
- A lot of tuning to optimize time <-> resolution trade off: Time step optimization, pre-calculation of meshes and fields, Mesh optimizations, number of e-h pairs, …

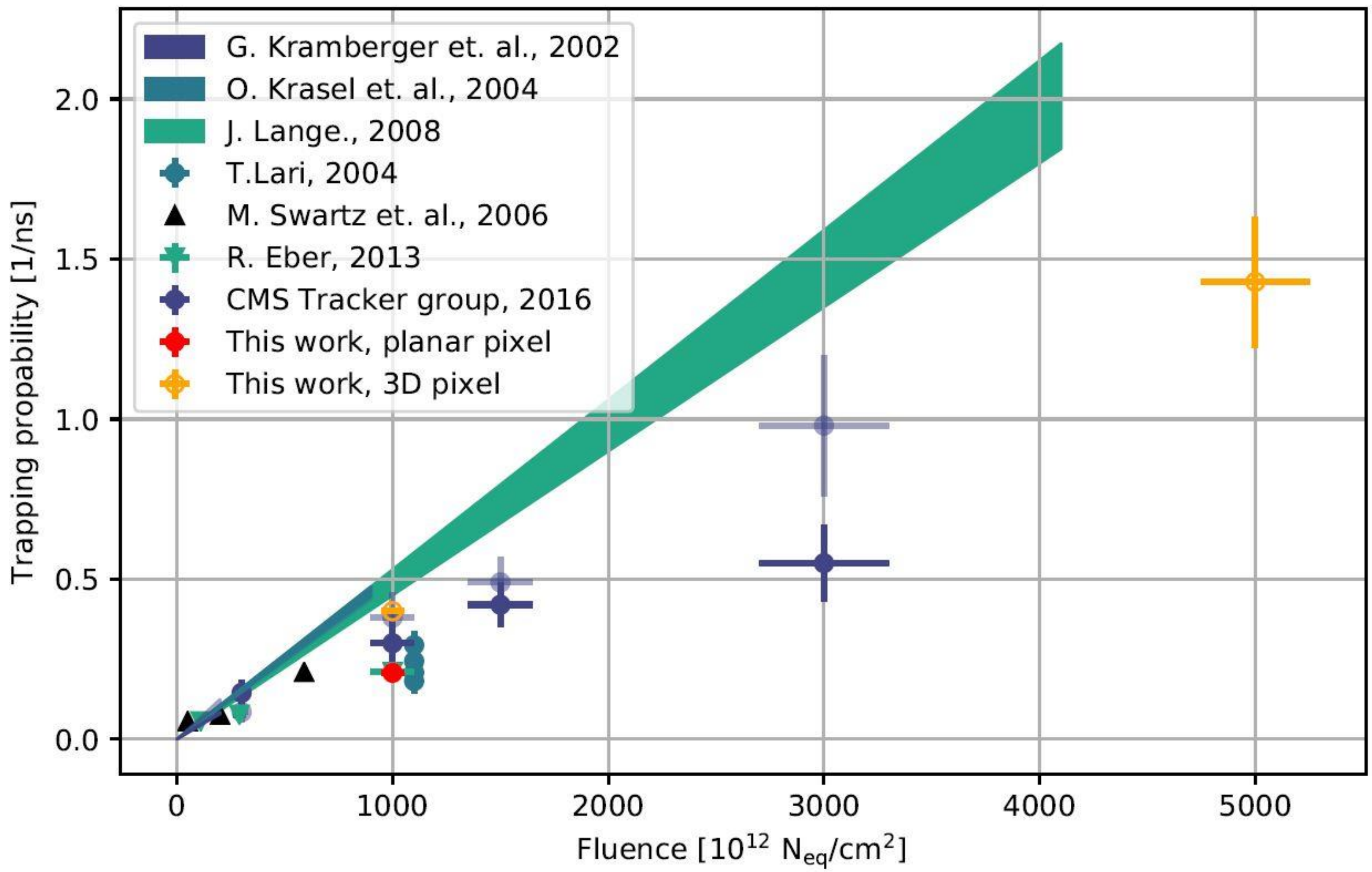
Comparison data vs. simulation: CCE IBL CiS planar sensor



[6] J. Lange, DESY-THESIS-2009-022 (2008)
[7] T. Pöhlsen DESY-THESIS-2010-013 (2010)

- N_{eff}, t_r optimized by χ^2scan on Bonn computational grid, with condition: $\boldsymbol{N_{eff}(250\mu m) = N_{eff}(200\mu m), t_r(250\mu m) = t_r(200\mu m)}$
- $\boldsymbol{7 \cdot 10^{15} N_{eq}/cm^2}$ **cannot be described** even with field dependent trapping [6, 7] ansatz: $t_r = t_{r1} + t_{r2} \cdot E$

Comparison to literature

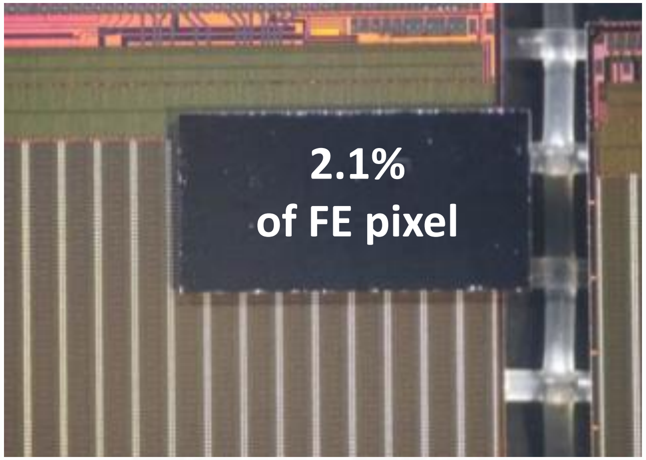


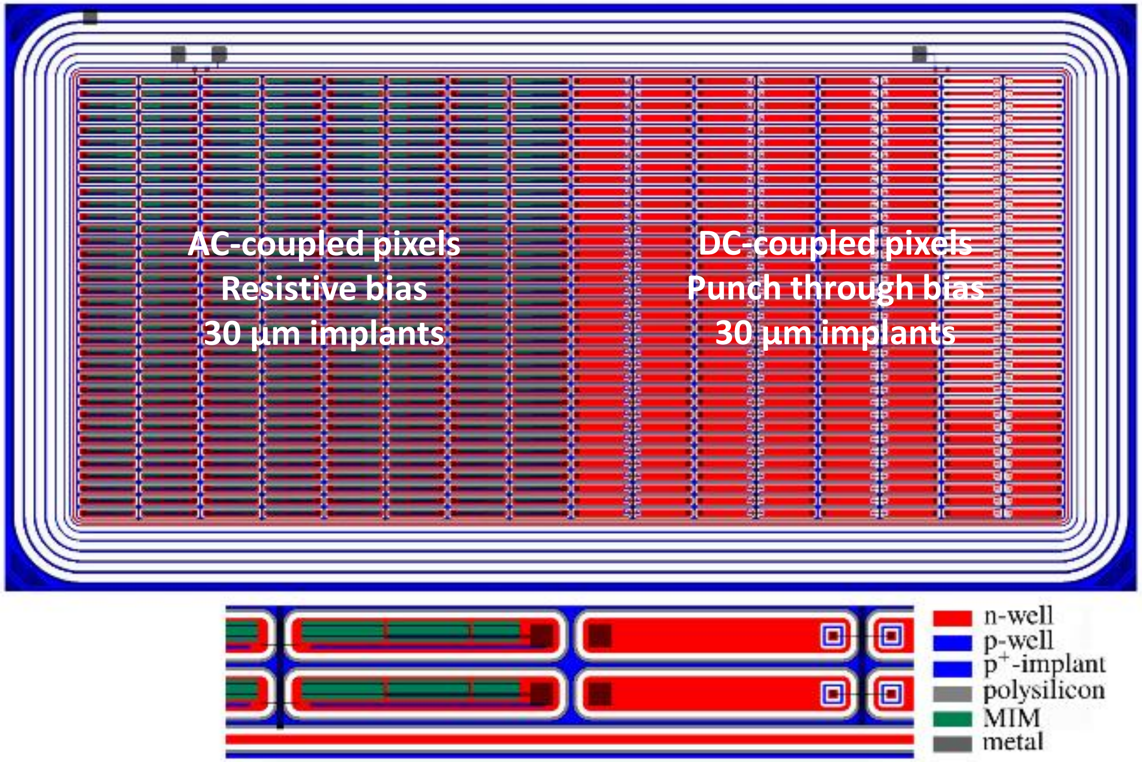
Description:
- Filled areas: Results from TCT measurements, area is 1 sigma confidence
- Dots: Results from CCE measurements
- Dark/light colors when e/h trapping probability is distinguished

- **Reasonable trapping propabilities** determined

A passive sensor in CMOS technology

- LFoundry 150 nm CMOS technology
- Substrate wafer: ~ **4 kΩ-cm**, CZ 200 mm, p-type
- **100 / 300 µm thick**, backside processed
- Bump bonded to the ATLAS FE-I4
- Pixel size: **50 µm x 250 µm**
- Matrix size: 16 x 36 pixels (1.8 mm x 4 mm)





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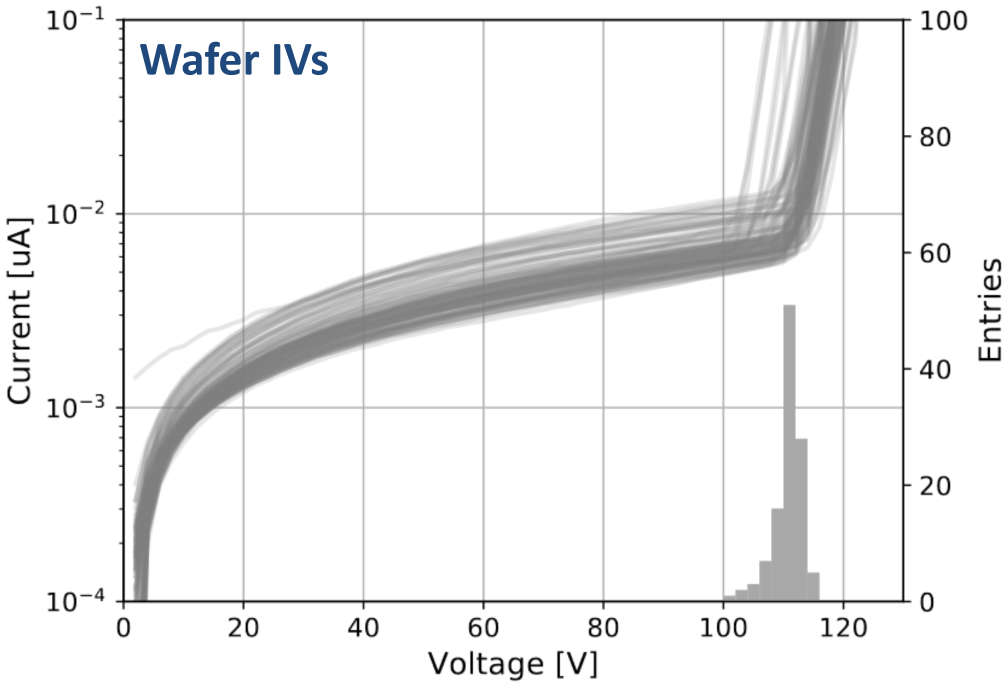
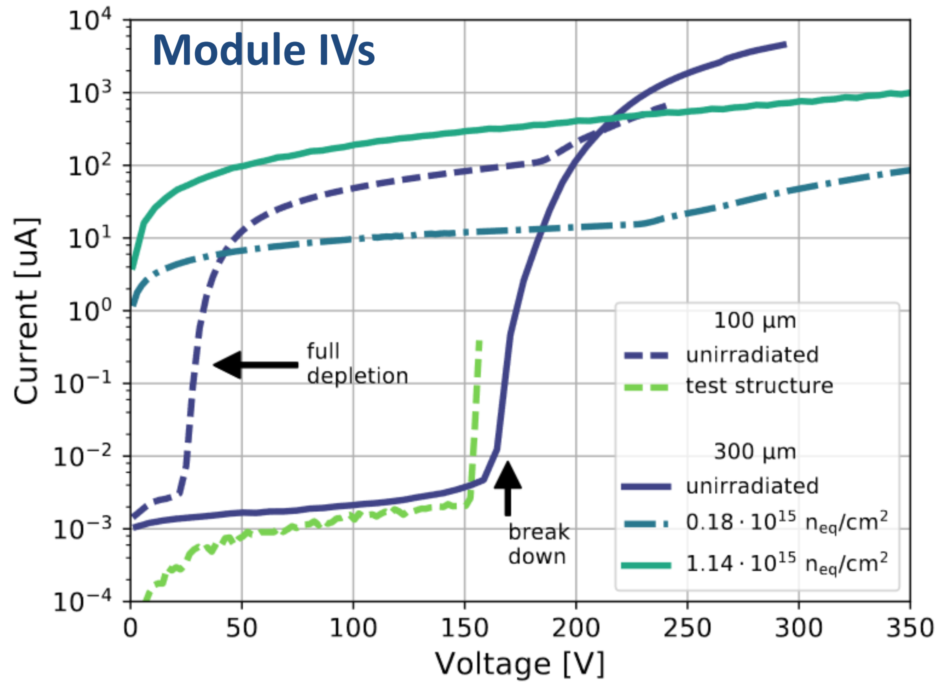
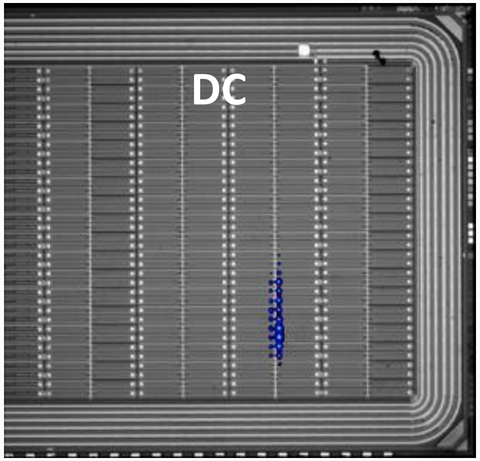
IV curves

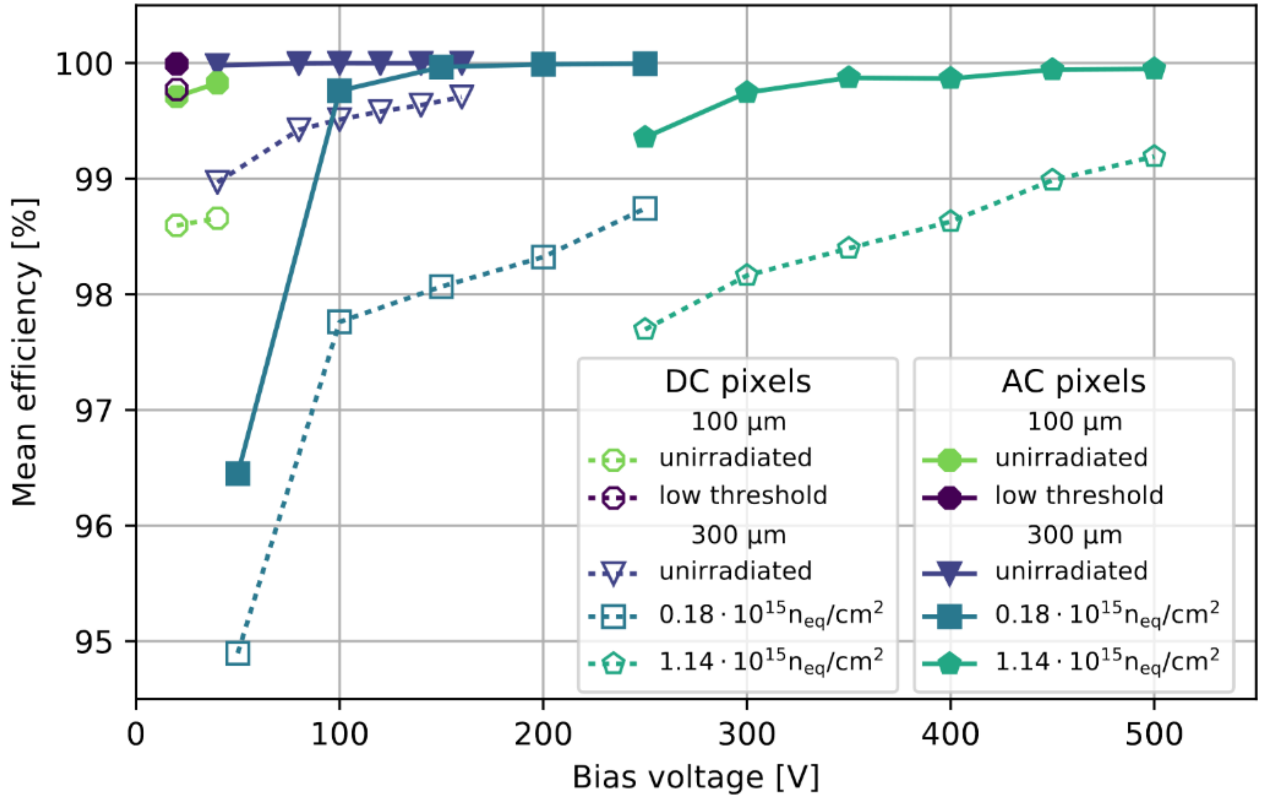




- **Wafer IV show similar curves** for 113 / 114 300 um devices
- **Additional leakage when depletion zone touches backside**, due to missing edging step
- **Dry etching step** (plasma edging) successfully tried on 8“ wafer, **leakage mitigated** (figure: *test structure*)
- **Break down** always in DC part **at bias dot**



Passive CMOS sensor efficiency after irradiation



- **Efficiency > 99.97 % for AC pixels**
- **Efficiency ~ 99.2 % for DC pixels**
- 100 um device at $1 \cdot 10^{15}$ N_{eq}/cm^2: > 96% (not shown)

Conclusion and Outlook

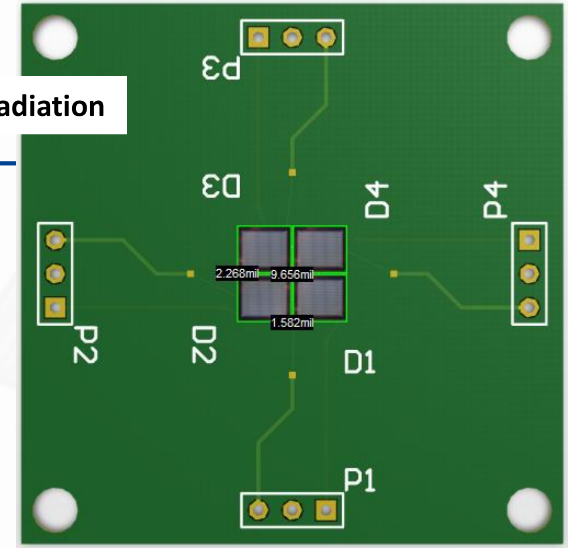
- 3D and planar concept:
  - CCE efficiency measured with newest, fast shaping ATLAS pixel ship up to $\mathbf{7 \cdot 10^{15} N_{eq}/cm^2}$
  - For actual ATLAS pixel geometry: **3D has 80 % higher CCE with 25% of the planar power dissipation**
  - **CCE(V) Curves can be described by simulation**, except $7 \cdot 10^{15}\mathrm{N_{eq}/cm^2}$ planar
  - Reasonable trapping probability deduced

- Passive CMOS sensor:
  - Working as well as the state-of-the art planar sensors
  - **AC coupling improves efficiency** due to missing bias dot
  - More info in: https://arxiv.org/abs/1702.04953
  - Backside process experience, bulk material and fill factor studies also useful for our fully monolithic pixel chip in the same technology (LFoundry 150 nm)

- Next:
  - Try to simulate CCE for HL-LHC pixel detector (smaller pixel, higher irradiation levels)
  - Dedicated **full size passive CMOS sensor submission** this year
  - **Investigate passive CMOS sensors with small pixels designs**

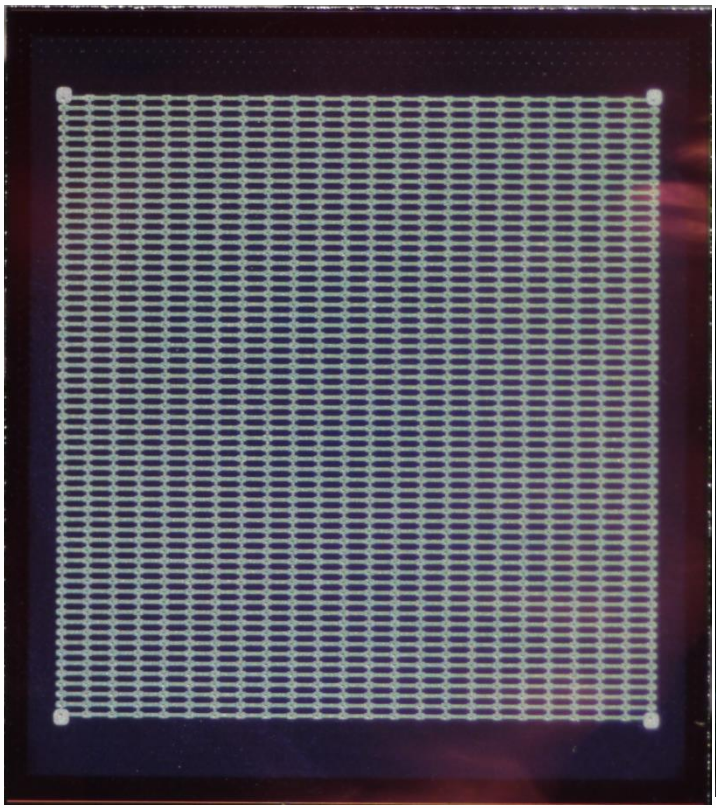
3D FBK Diodes from IBL production

PCB for irradiation

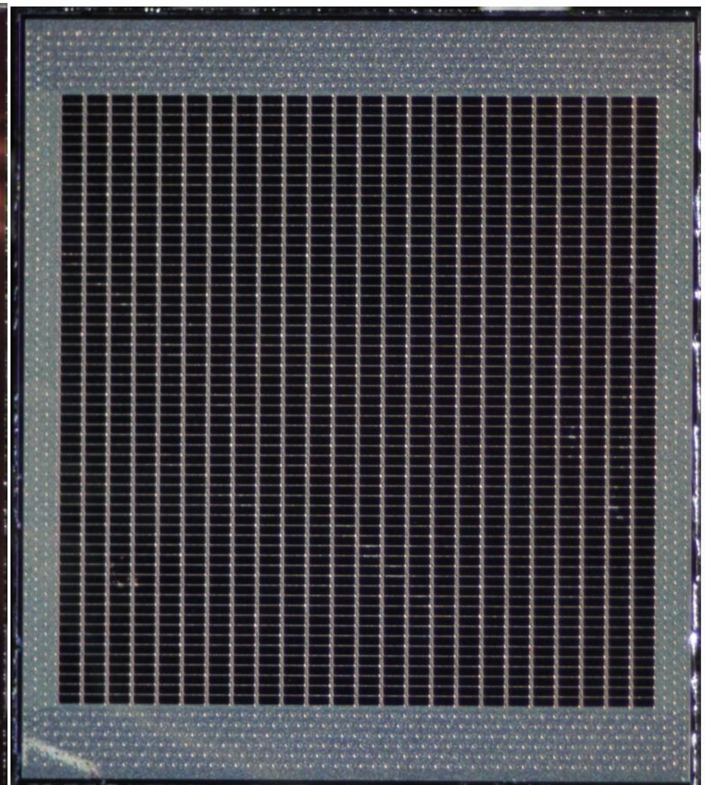


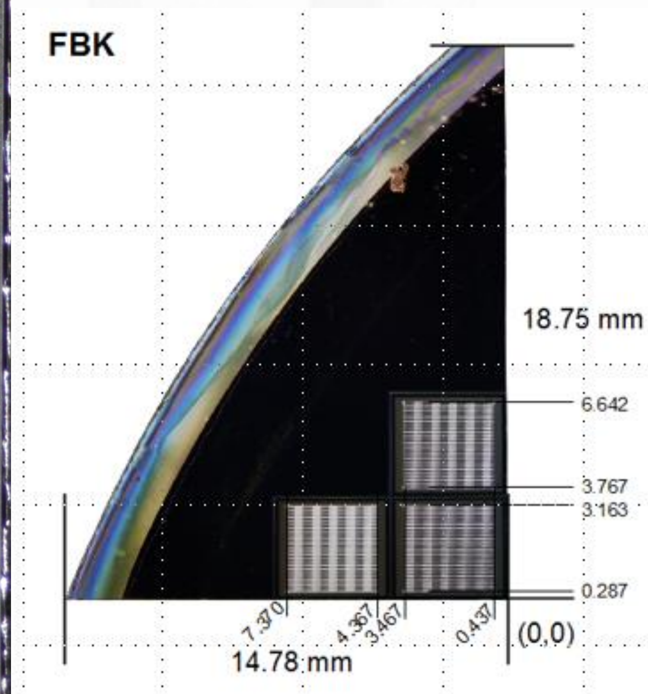
- 12 x 60 pixel
- 3D pixel ~ 180 fF → **130 pF**

Front



Back





3D FBK Diodes from IBL production

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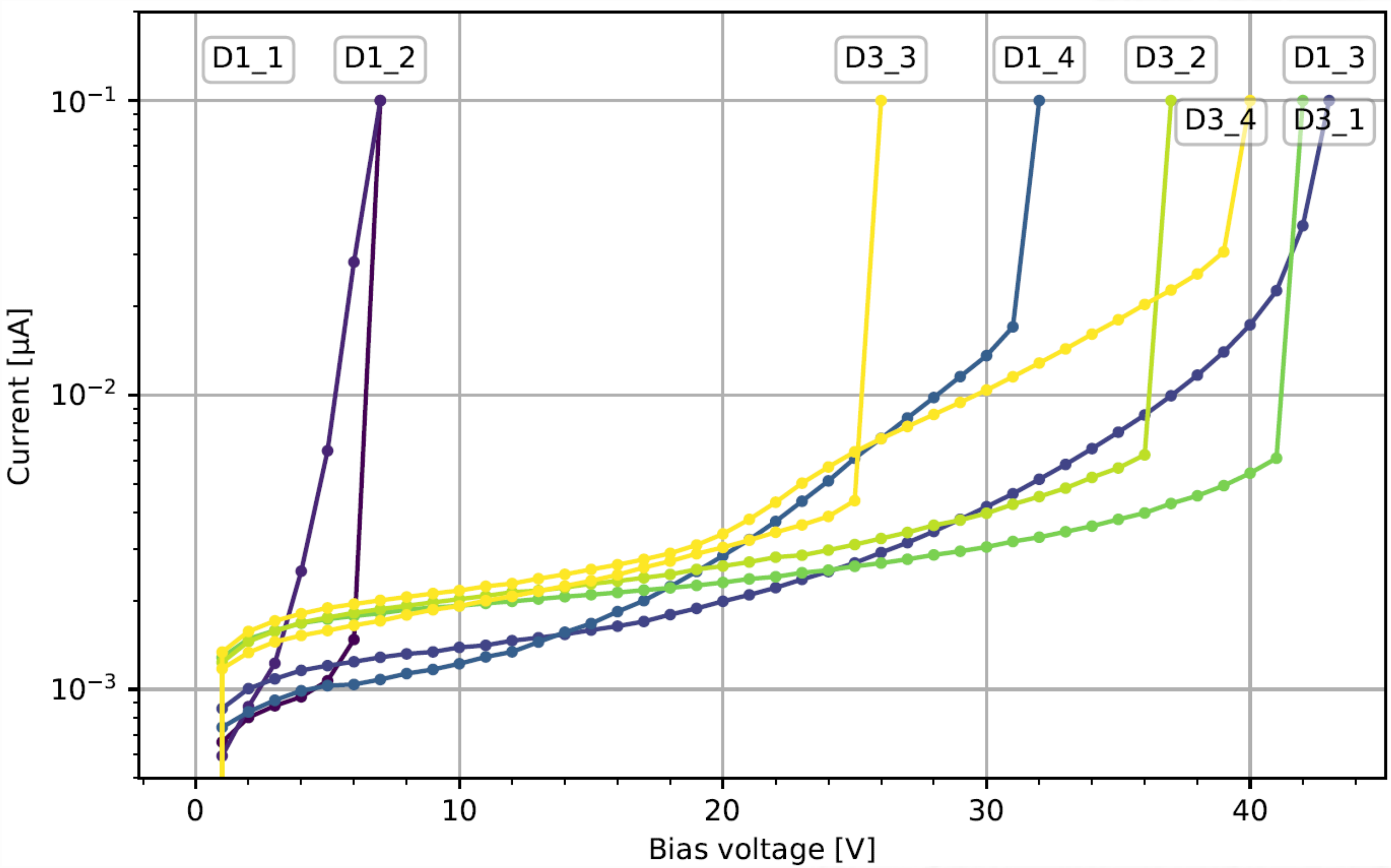
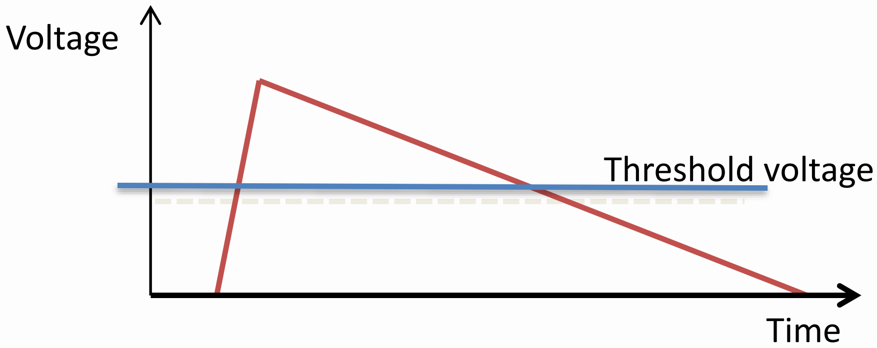
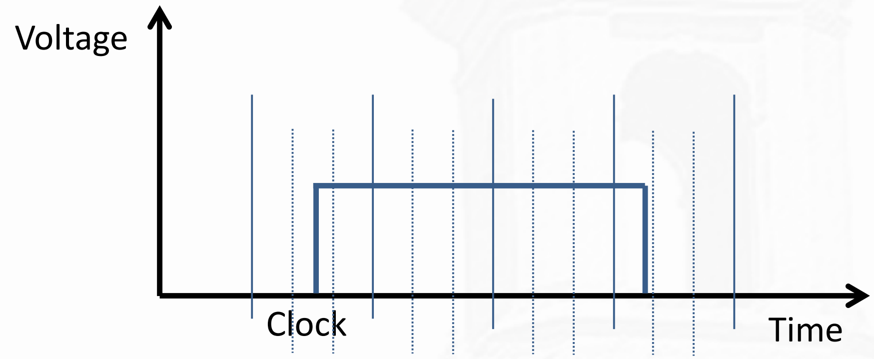
- Located on production wafer edges
- Very low yield, IBL requirement > 40 V breakdown only seen for 2/12 → only D3_1 used

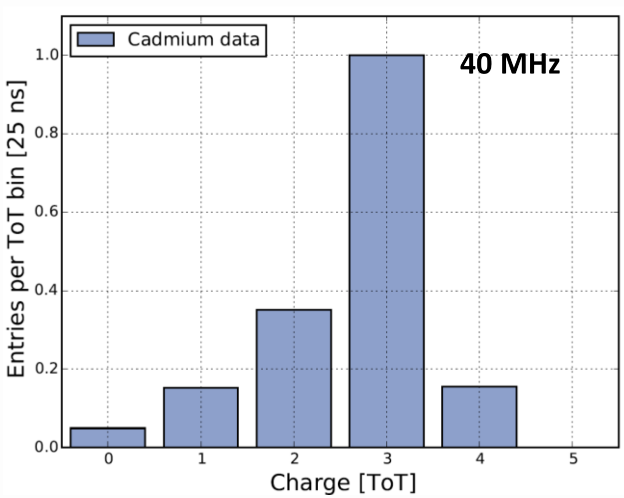


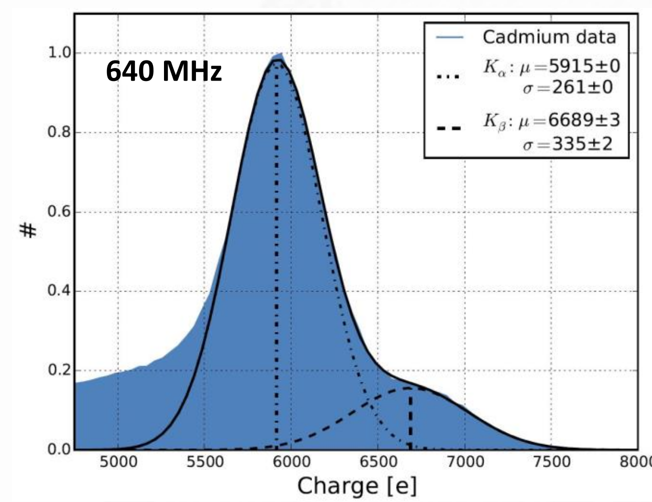
Charge measurement with ATLAS FE-I4: TDC method

- Time-over-threshold technique with 4-bit resolution only, 40 MHz clock
- Idea: Sample charge signal externally with fast FPGA TDC, 10-bit, 640 MHz clock





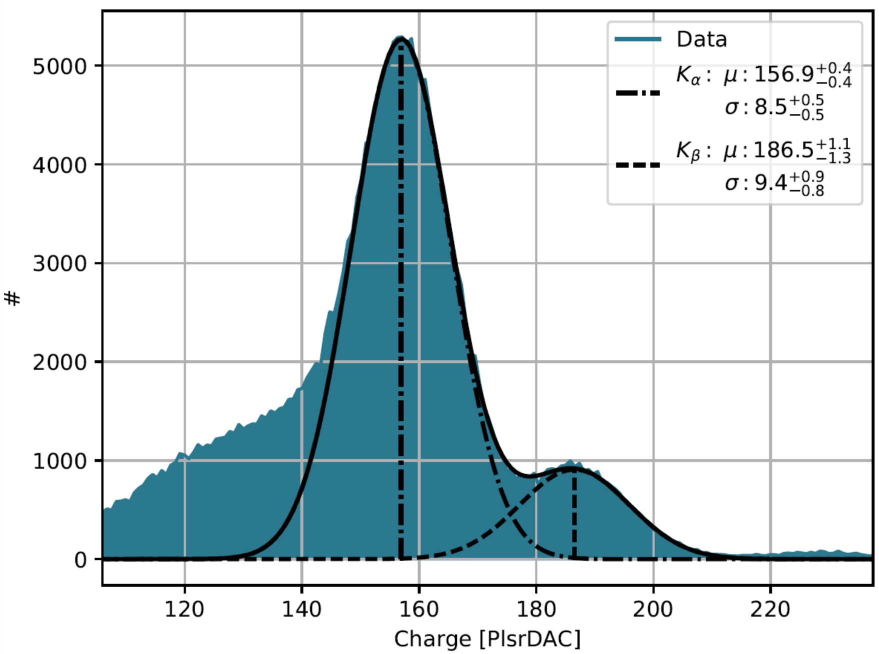


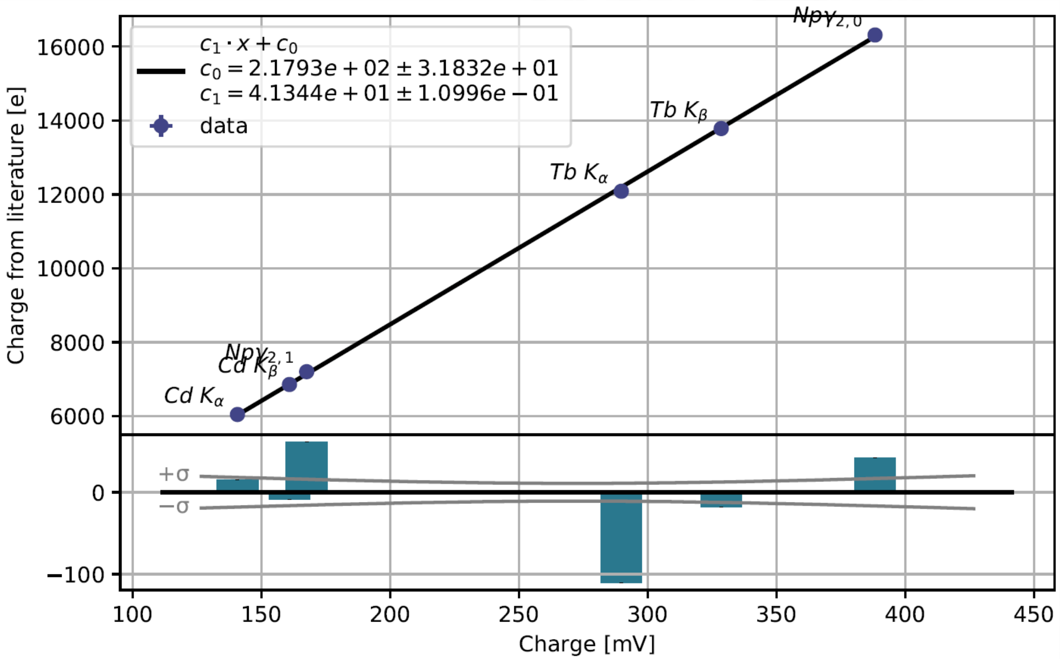


- Disadvantage: signal is ORed for all pixels, only seed pixel charge can me measured directly

Calibration with X-Ray sources

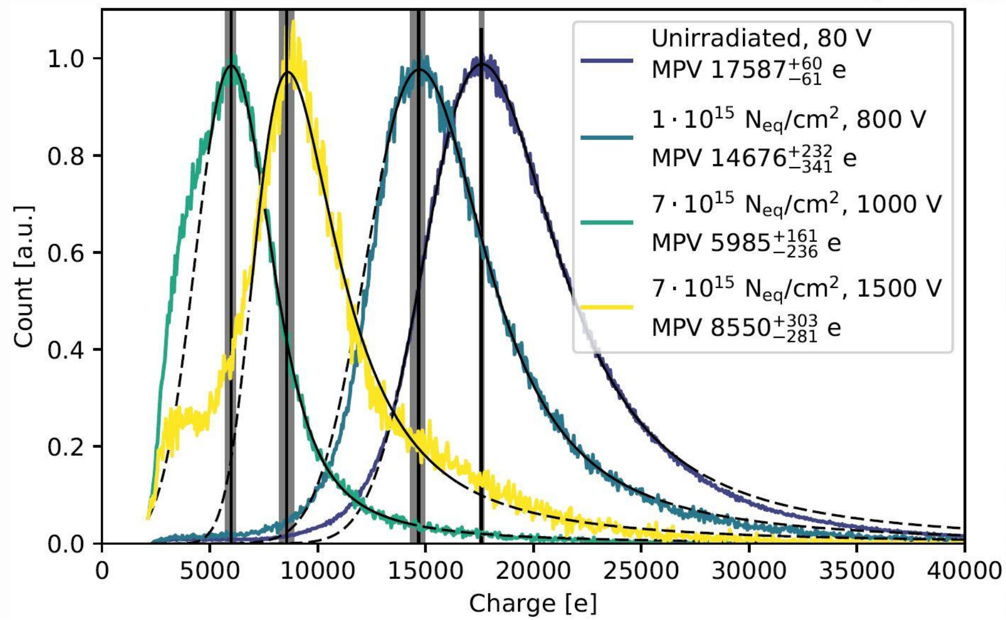
1. **Calibrate** internal charge injection circuitry of readout **chip using X-Ray sources** on unirradiated sensors
2. For each irradiation step:
    1. **Correct** and measure changes in internal **charge injection circuitry** due to TID (up to **800 MRAD**!!)
    2. Do a **TOT(Q) calibration** per pixel using the internal charge injection circuitry
    3. **Measure** changes in **CCE with Sr-90**



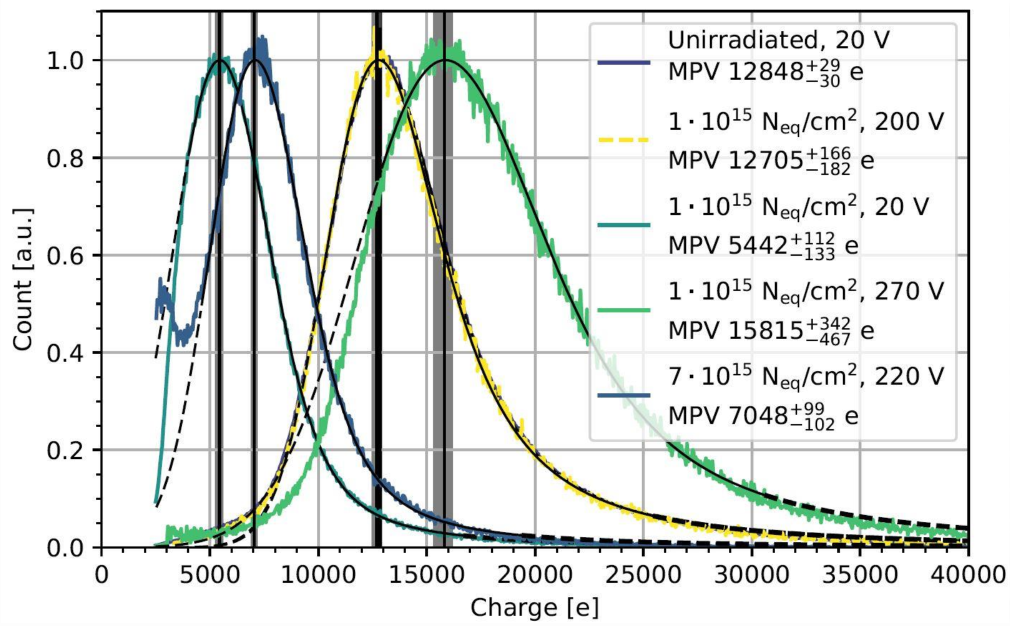


Example Landau fits

- Langau MPV determined from deconvoluted Langau * Gauss(σ_{noise}), otherwise more noise means higher MPV!
- **ROOT definition of Landau cannot be used** to get correct errors (μ != MPV, μ=μ(σ))
- New Landau * Gauss Python package created: https://github.com/SiLab-Bonn/pyLandau
- Asymmetric errors from iminuit + migrad

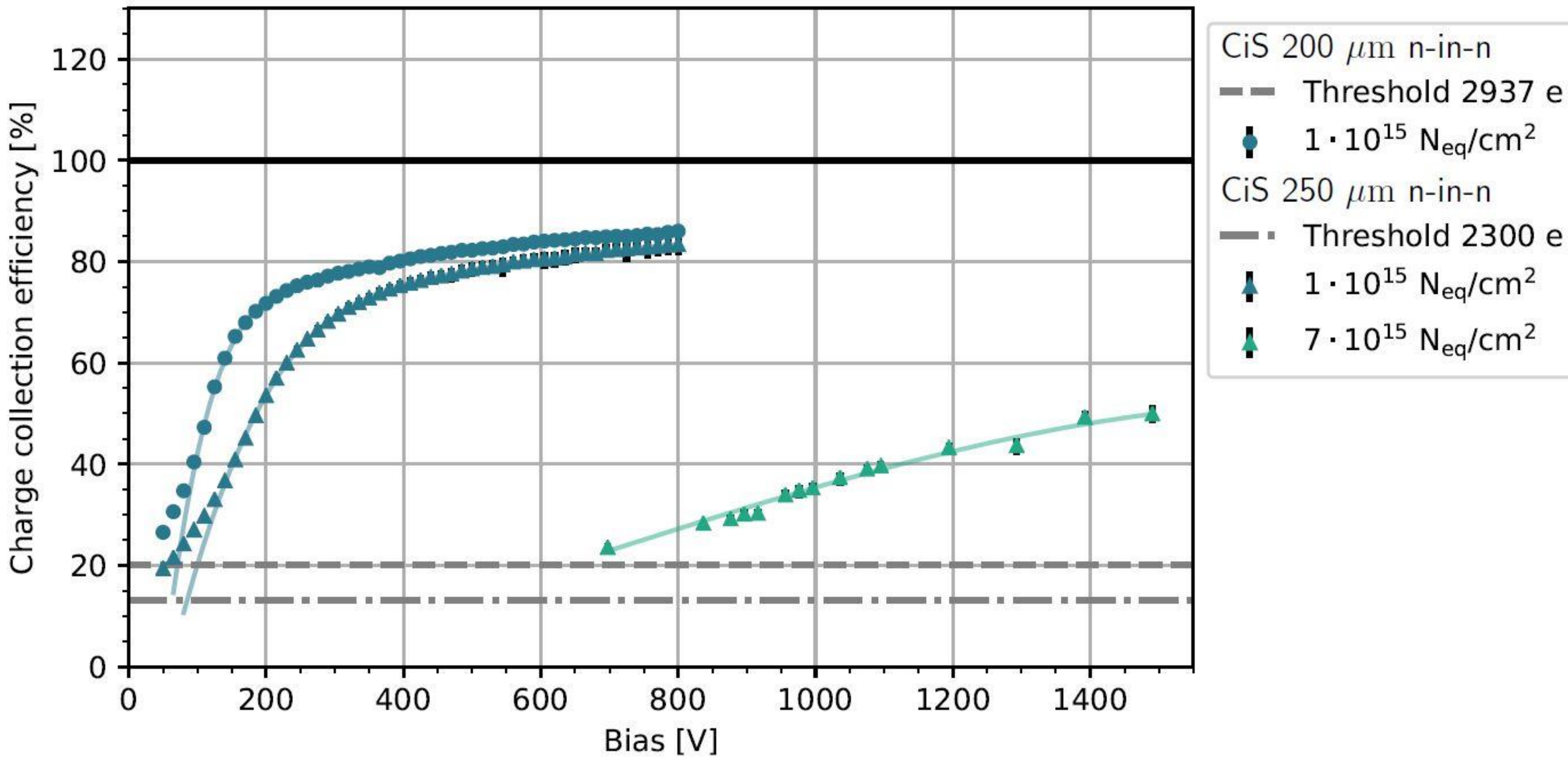


Planar 250 um n-in-n sensor



3D 230 um CNM n-in-p sensor

Charge collection efficiency, IBL planar modules



Simulation of Charge Collection Efficiency with SCARCE

- FiPy: Finite Volume PDE Solver from NIST (http://www.ctcms.nist.gov/fipy/) for potentials

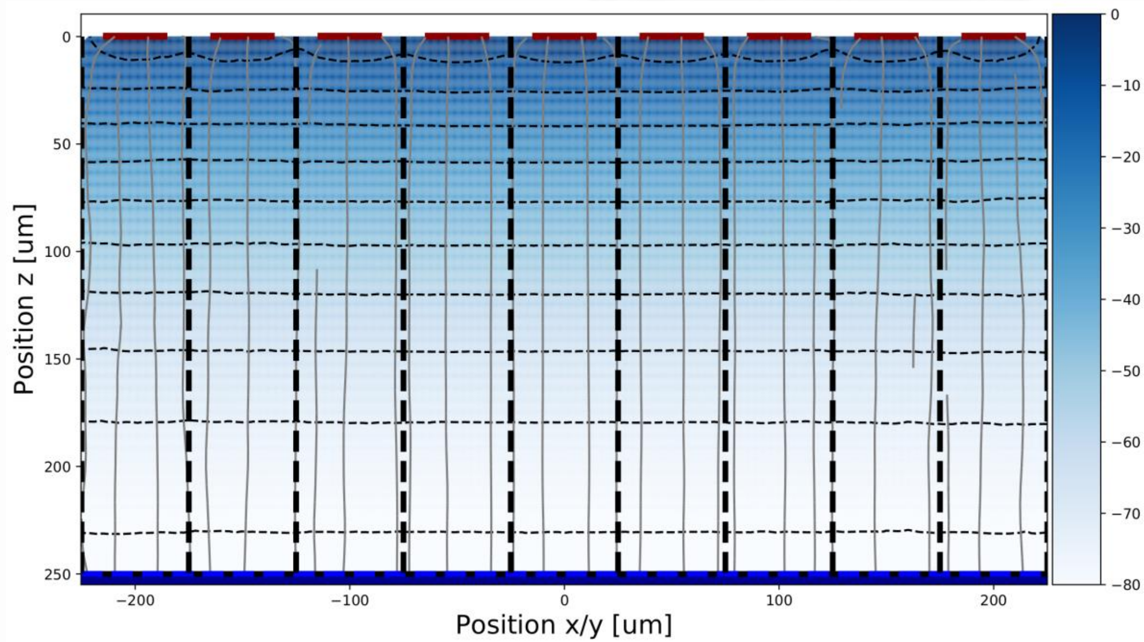
Drift potential:

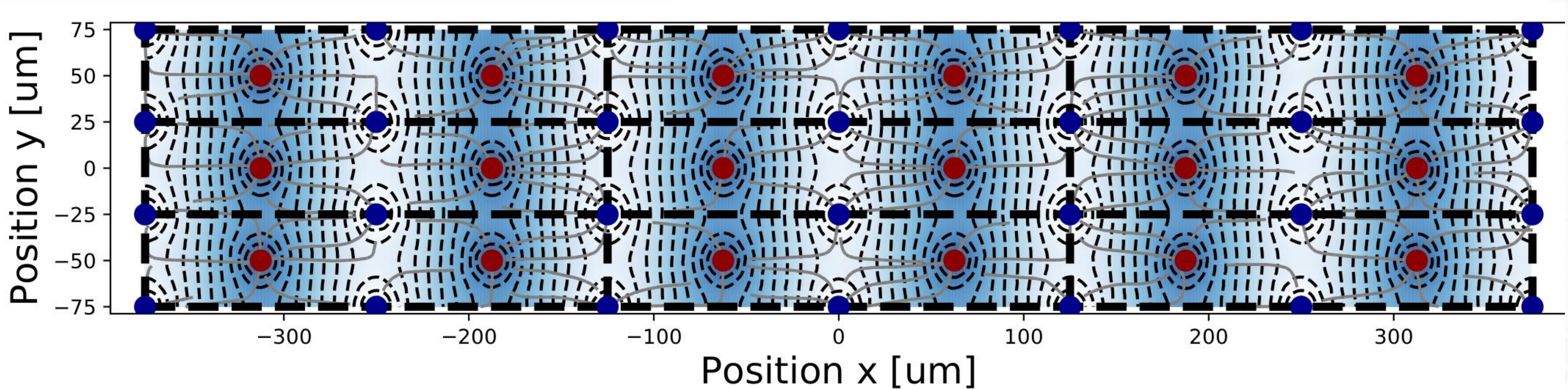
$$\nabla^2\Phi = \frac{\rho}{\epsilon}$$
$$\Phi_b = V_{bias}, \Phi_r = V_{readout}$$
$$\rho = const.$$

Drift field:

$$\vec{E} = -\nabla\Phi$$

- Numerical differentiation after smoothing





Charge collection efficiency for different fluences

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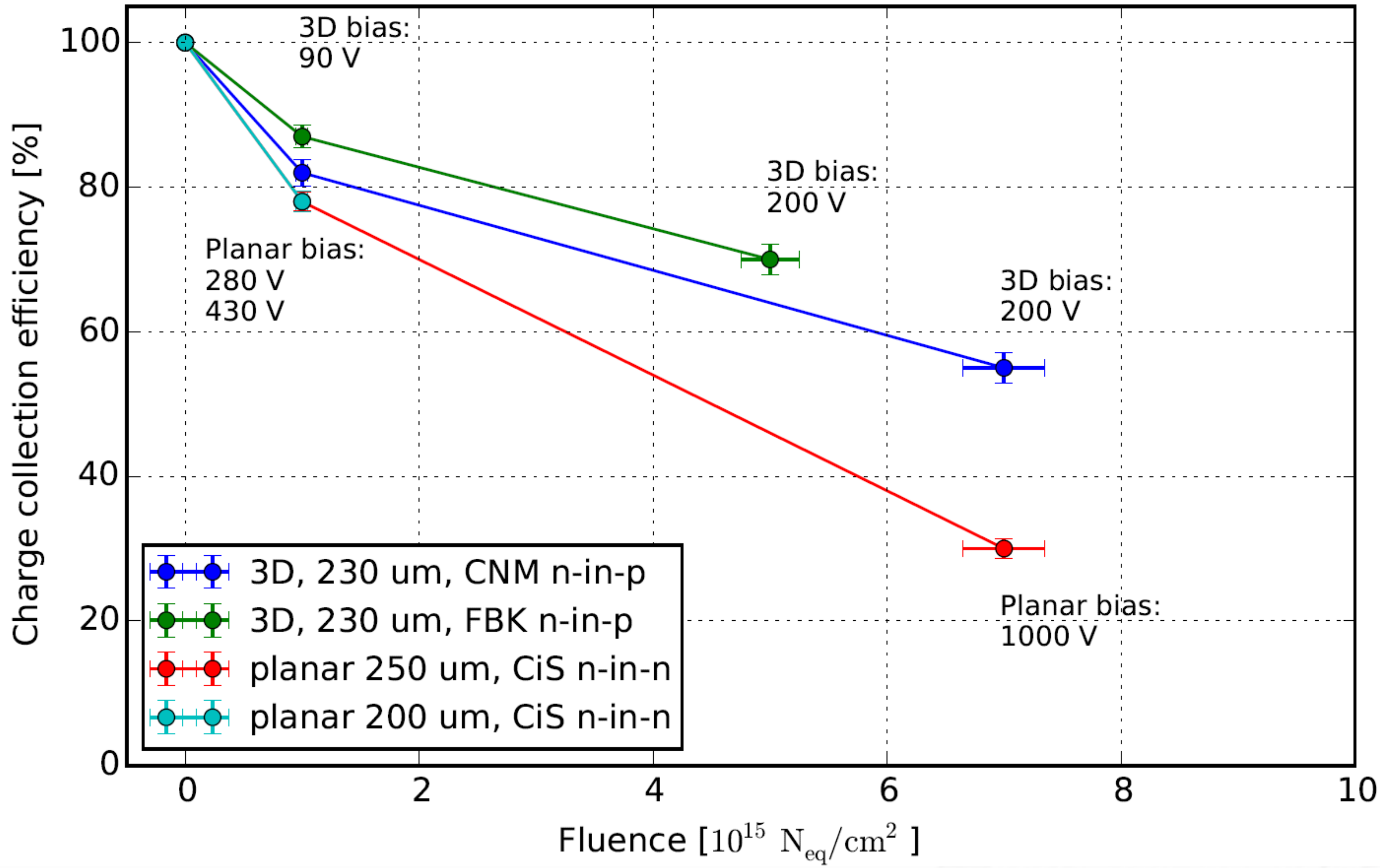

- 3D sensor vs planar: 80 % higher CCE with 25 % power dissipation

Pixel layout: AC coupled pixels

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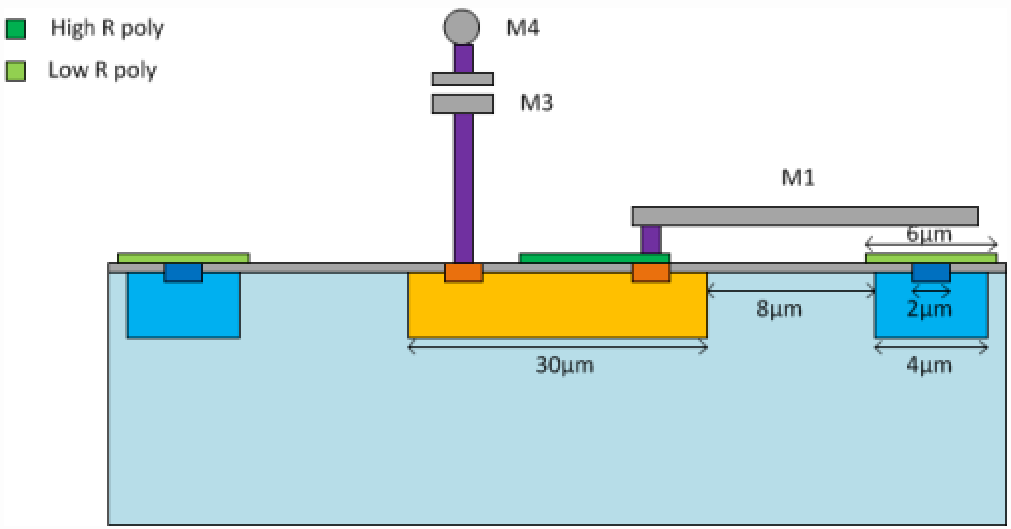
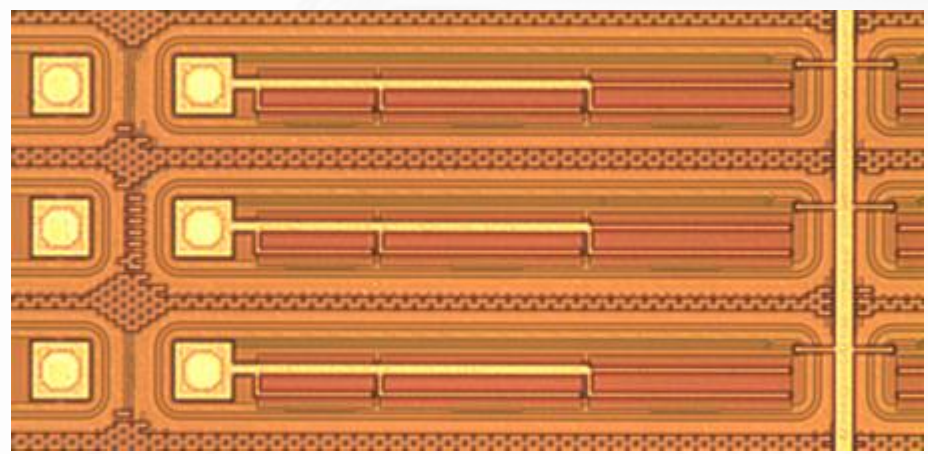
- 10 pF MIM capacitor for the AC coupling (between M3 and M4)
- High resistive poly-silicon layer used for bias resistor
  - 15 MΩ resistor in each pixel
  - Contributes to the input capacitance → relevant for noise
- Low resistive poly-silicon layer used for field plate on top of p-stop
  - P-stop consists has a contact to apply an external voltage (possible improvement of breakdown behavior)





Passive CMOS resistivity estimation

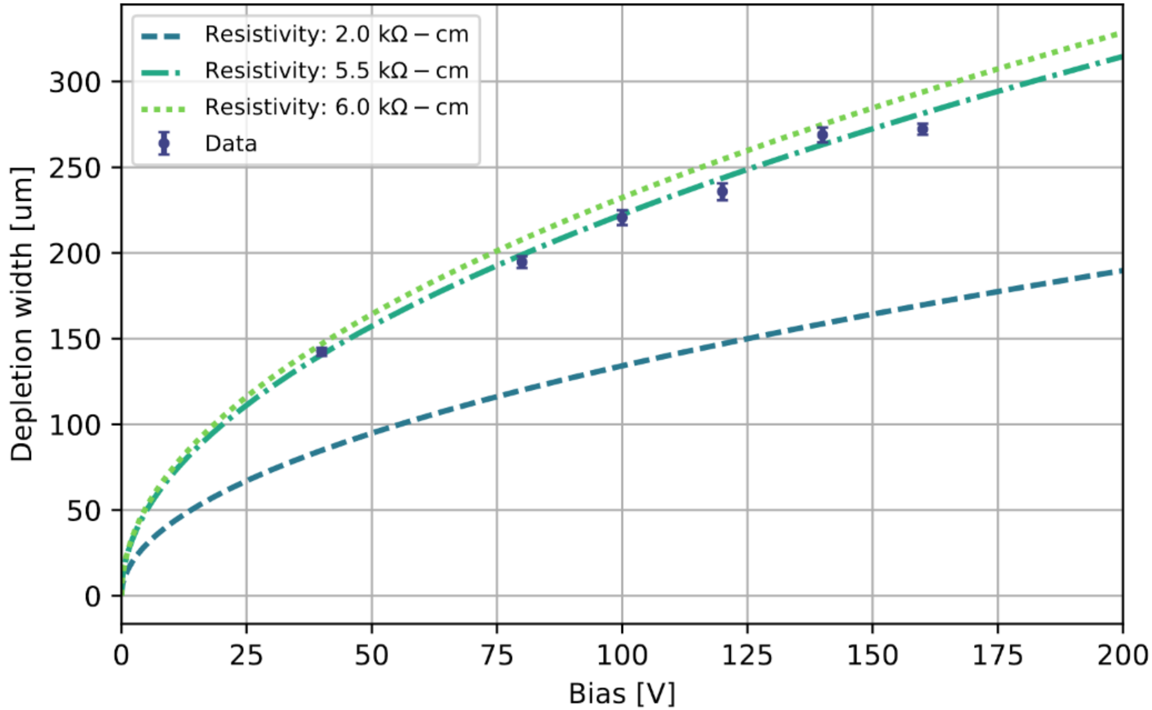


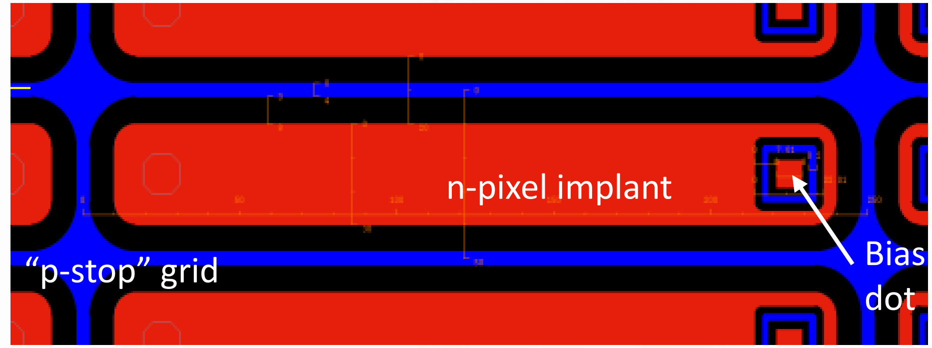
Figure 4. Depletion depth as a function of bias voltage for the 300 µm thick LFoundry passive pixel sensor. The depletion depth was calculated using Langau fits as in figure 3 assuming 71 e/h pairs created per micrometer. Theoretical depletion curves for three bulk resistivities given by 4.1 are shown for comparison.

$$d = \sqrt{\frac{2\epsilon_0\epsilon_r}{eN_{\text{eff}}}(V_{\text{bi}} + V_{\text{bias}})} \quad \Rightarrow \quad d\,[\mu\text{m}] \approx 0.3\sqrt{\rho\,[\Omega\,\text{cm}] \cdot V_{\text{bias}}\,[\text{V}]}$$

- Resistivity ~ 5 kΩ-cm
- Assumption: drift only due to fast shaping, 71 e/h pairs per micron

Pixel layout: DC coupled pixels

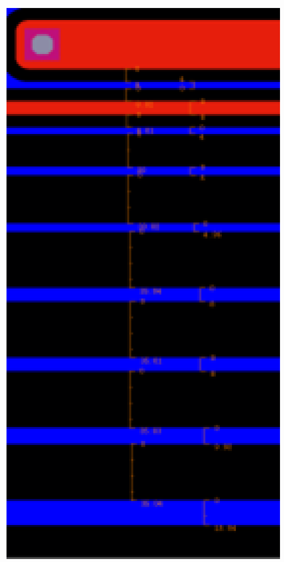
- Only p- and n-implants shown (blue and red)
- „Standard“ pixel geometry:
  - 30 µm n-implant width
  - 20 µm gap
  - 4 µm „p-stop“ grid
  - punch-though bias for DC pixels

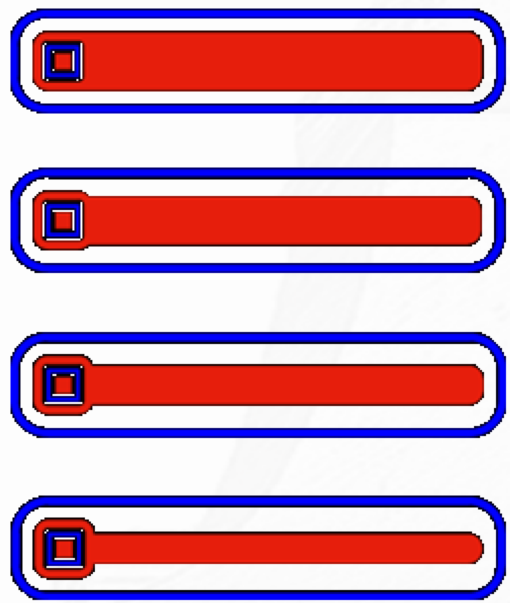


Special edge pixel with reduced n-implant width for Cap / Efficiency R&D:

p-implant („p-stop“ grid)
n-implant (inner guard ring)

p-implant guard rings





30 µm n-implant width

25 µm n-implant width

20 µm n-implant width

15 µm n-implant width

Pixel Layouts (DC-coupled version)

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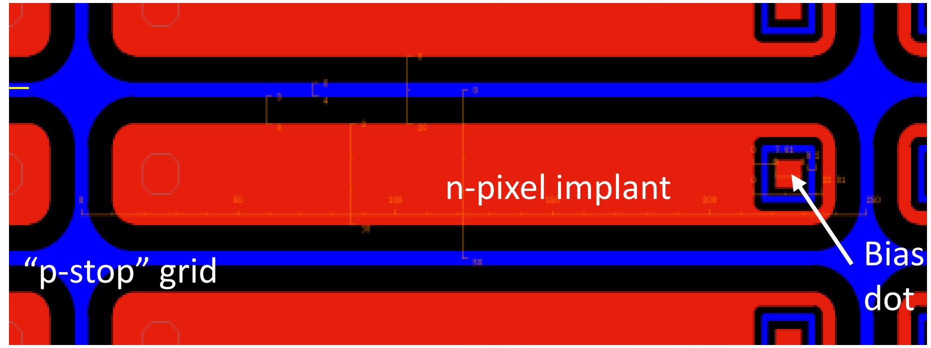
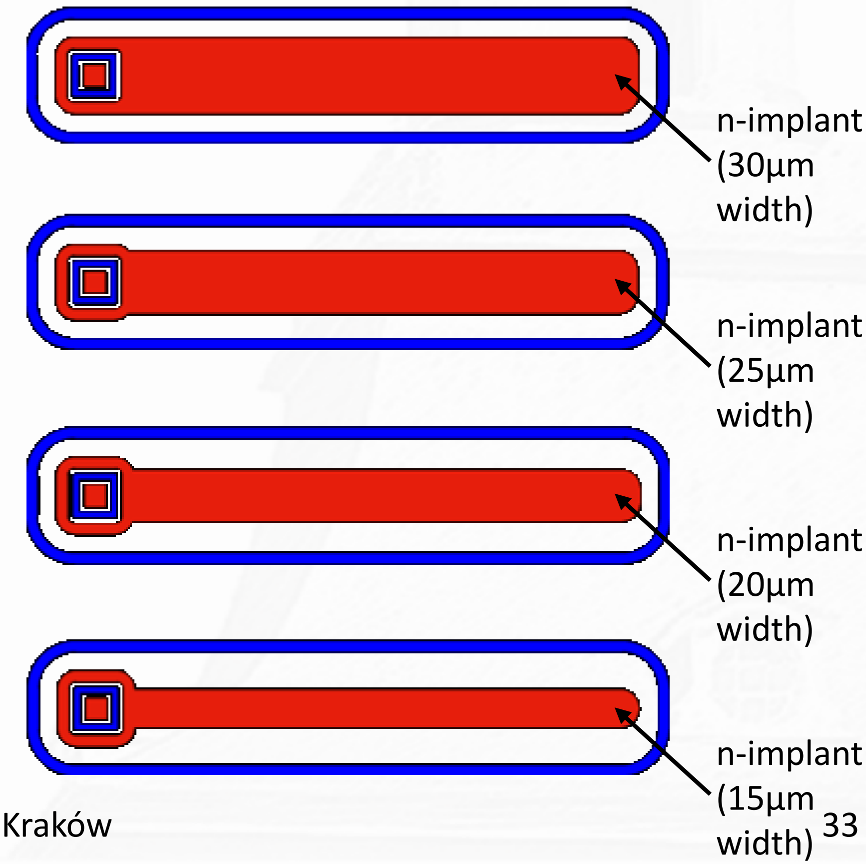
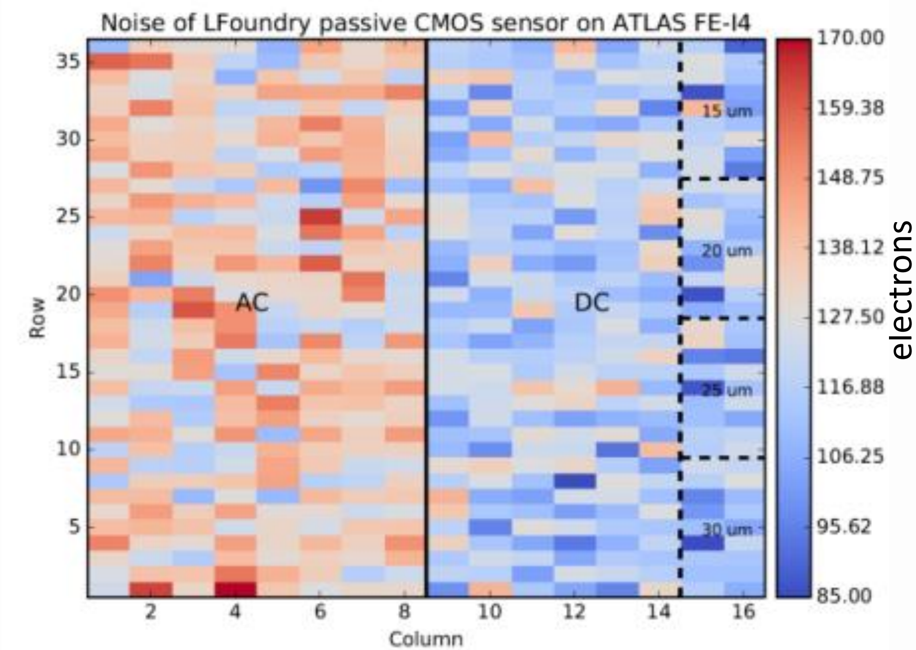
- Only p- and n-implants shown (resp. blue and red)
- „Standard“ pixel geometry:
  - 30µm n-implant width
  - 20µm gap
  - 4µm „p-stop“ grid
- Pixel layout variants:
  - Bias dot (punch-though) layout not changed
  - Implant length not changed
  - Implant width variation covers ~200µm of the implant length

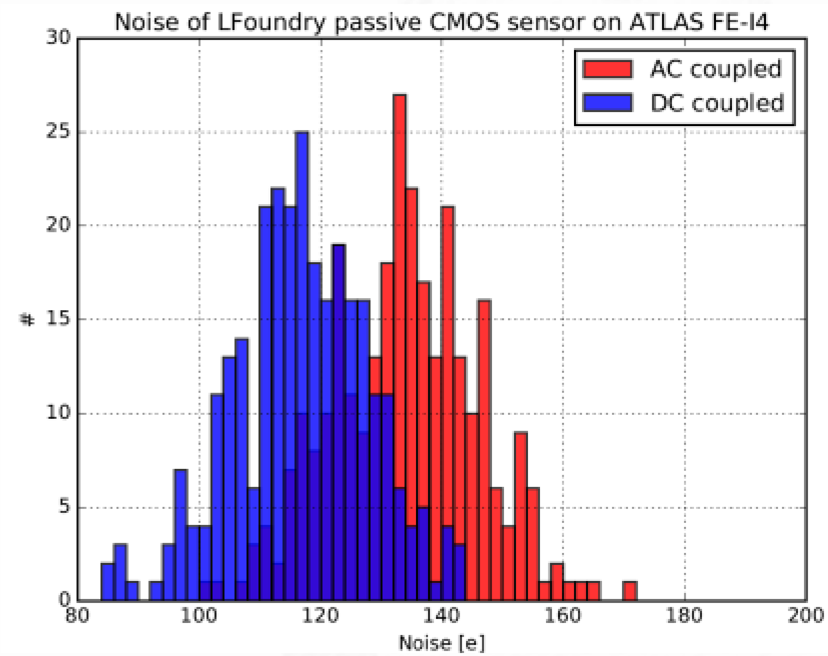
Implant width	Gap width
30µm	20µm
25µm	25µm
20µm	30µm
15µm	35µm





Noise and input capacitance





- **AC** couples pixels: **(133 ± 1) e^-**
- **DC** couples pixels: **(117 ± 1) e^-**
- *ATLAS IBL n-in-n planar pixel: ~ 120 e^- @ 117 fF input capacitance*
- *ATLAS IBL 3D pixel: ~ 150 e^- @ 180 fF*
- → **AC pixel < 180 fF, DC pixel <120 fF**
- First design: AC coupling R / C values not optimized!

AC coupling advantage: no bias dots

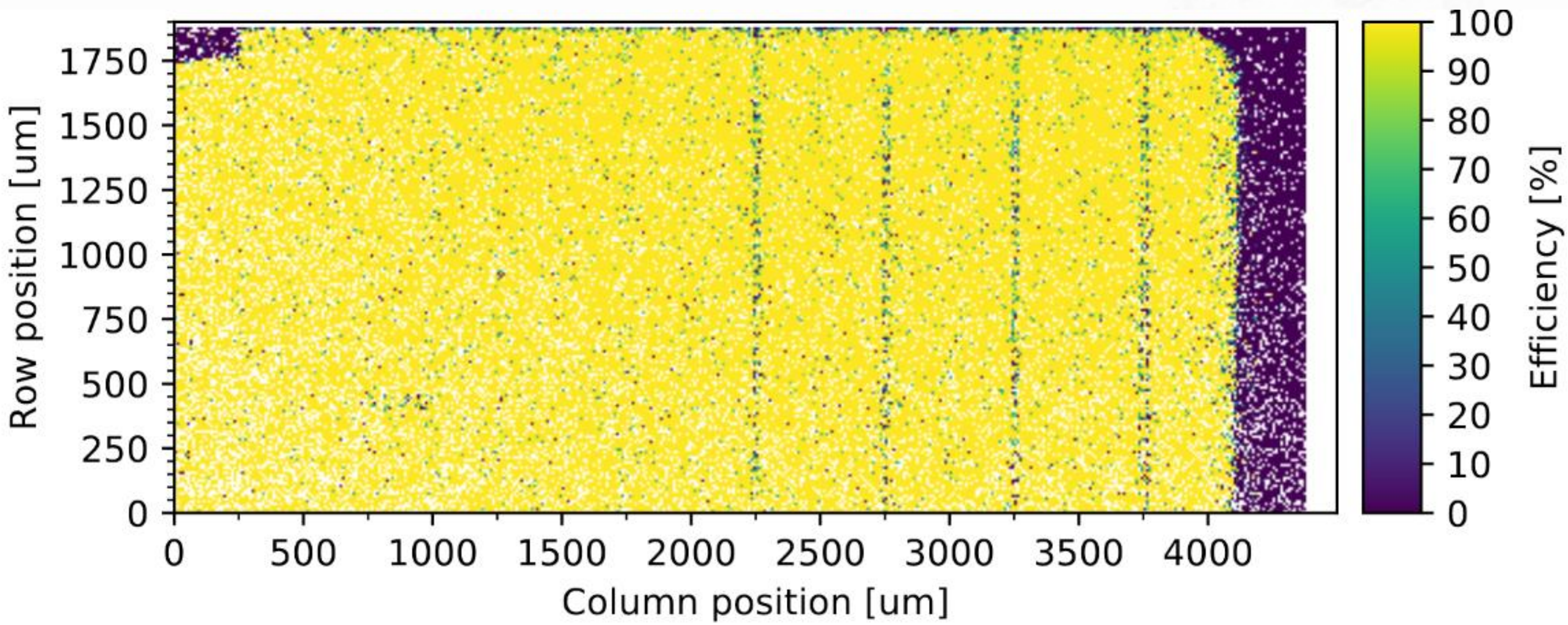


Figure 6. Hit detection efficiency map of the LFoundry passive pixel sensor with 300 µm thickness at 160 V bias. Bins of 10 µm x 10 µm size have been used and are labeled by a white color where the efficiency determination is not possible due to low statistics. The efficiency is not correct on an absolute scale (see section 3), but shows the efficiency loss at the location of the bias dots. The upper left inefficient area are two disabled pixels during analysis and the inefficient area to the right marks the edge of the active sensor area.