30th RD50 Workshop
STFC RAL

E. G. Villani

Overview

- TCAD simulation of CMOS devices (OVERMOS/DECAL).
- Radiation effects investigation on CMOS Si using Schottky diodes proposal

DECAL: CMOS MAPS for Linear Collider

- Mature, high volume industrial devices: no proprietary processes → reduced costs
- Low(-ish) power, depends on duty cycle
- Low material budget, can be very thin
- Radiation hard (few >Mrad)
- Very granular (pixels ~10um)

New features developed for LC

- TPAC et al. (digital ECAL)
- Deep p-well implant/InMAPS process
  - Makes MAPS viable
  - Improved charge collection efficiency
- High resistivity/HV epitaxial layers
  - Further charge collection and radiation hardness improvements

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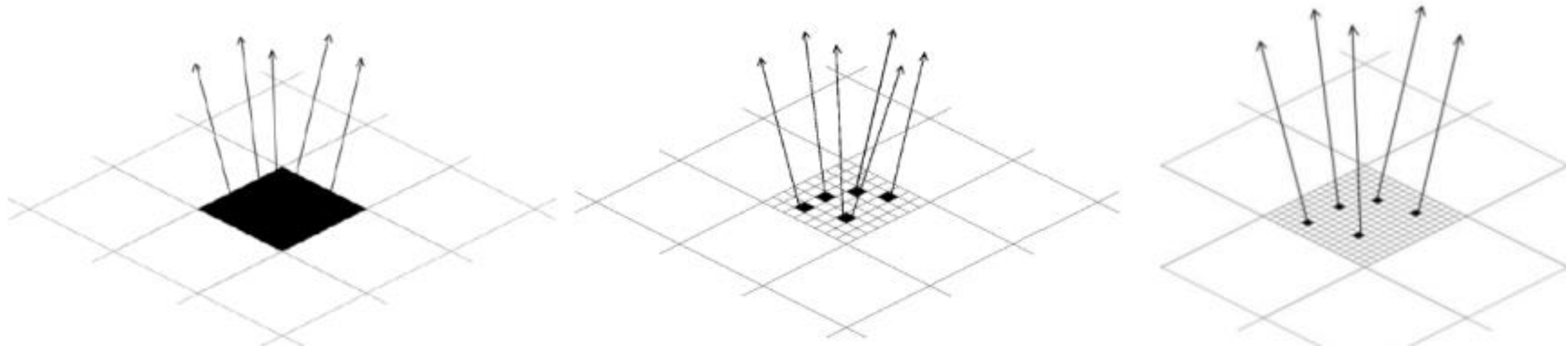
DECAL Concept

- Concept, swap ~0.5x0.5 cm^2 Si pads with small pixels ("Small" := at most one particle/pixel, 1-bit ADC/pixel)
- How small to avoid saturation/non-linearity?
  - EM shower core density at 500GeV is ~100/mm^2
  - Pixels must be<$100\times100\mu m^2$
    - Used baseline $50\times50\mu m^2$
  - Gives ~10^{12} pixels for ECAL – "Tera-pixel APS"
  - Mandatory to integrate electronics on sensor



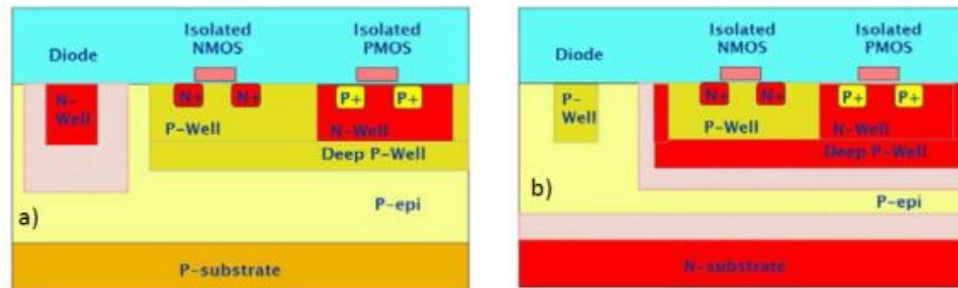


Figure 3. a) Original deep P-well pixel designed for TPAC as well as for ALICE and b) proposed new pixel architecture

Imaging MAPS technologies suffer from poor radiation tolerance due to slow (diffusion) charge collection and related loss of signal due to increased recombination rate and trapping

OVERMOS : CMOS TJ Hi-res demonstrator

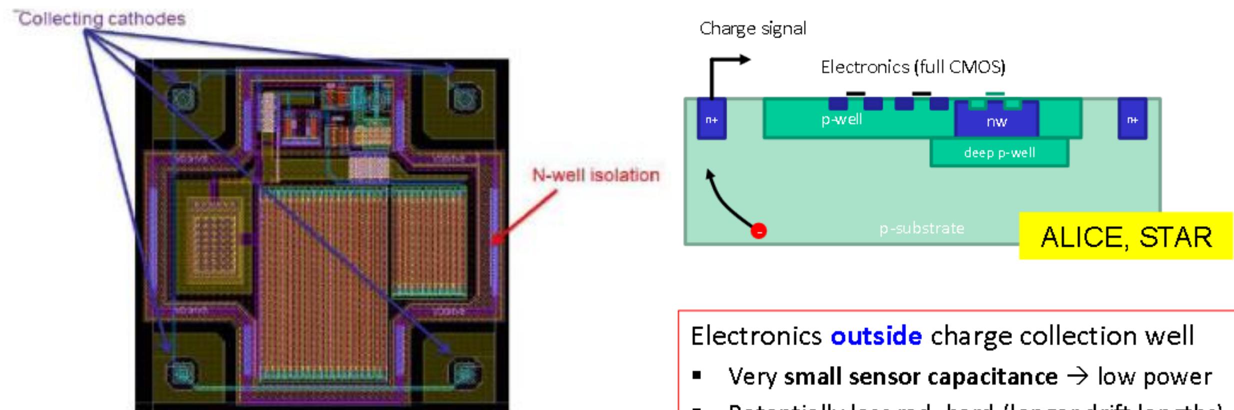


Figure 4 Example Pixel Circuit in ToweJazz 180 HR-CMOS

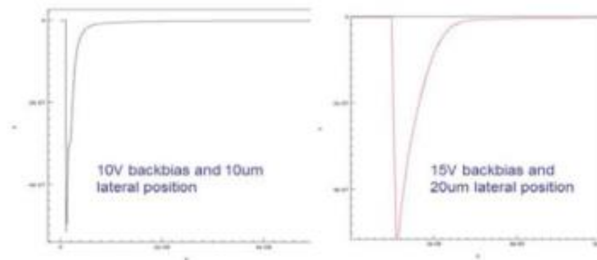
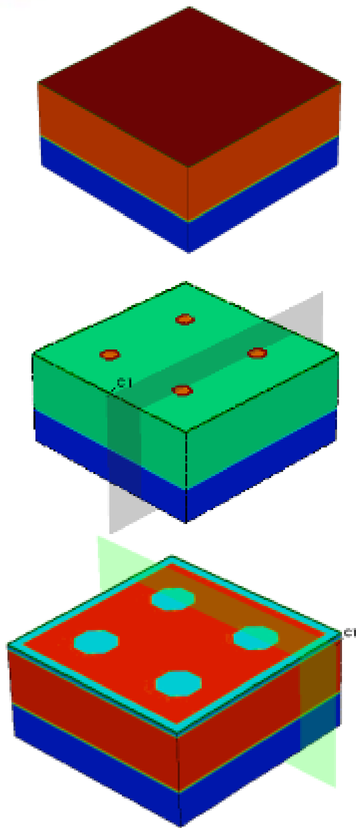
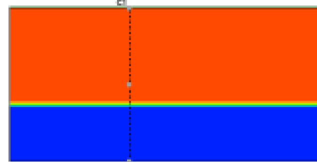


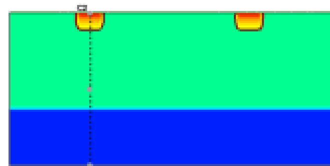
Figure 5 Example of simulated current pulse for signals at different bias settings and distance to charge collection node



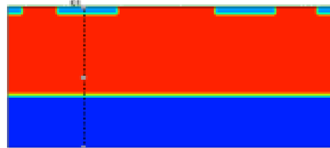
Epi-Bulk

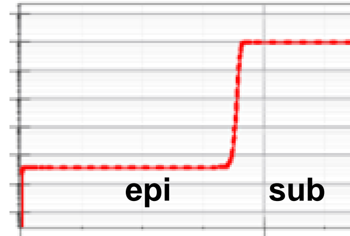


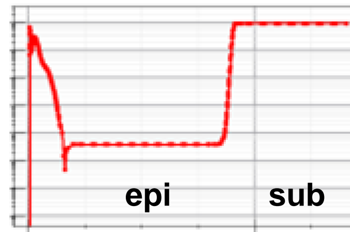
NW

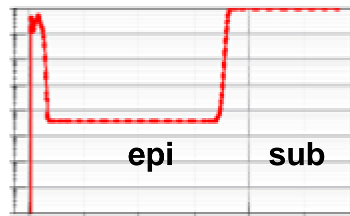


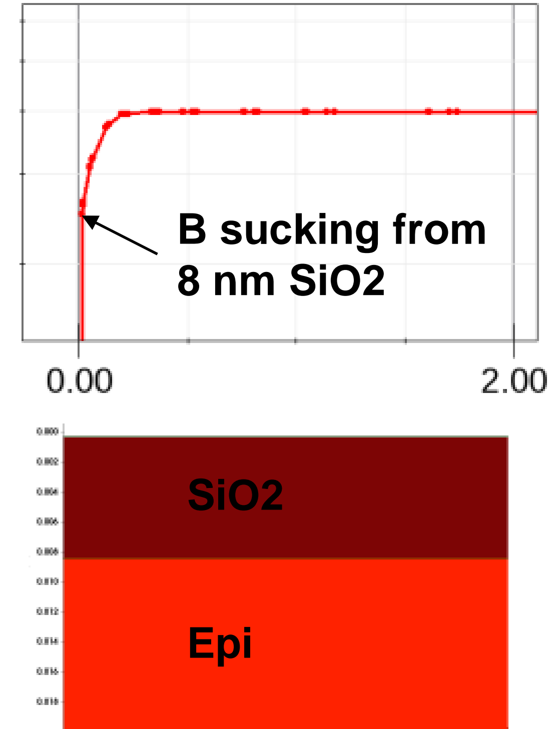
PW



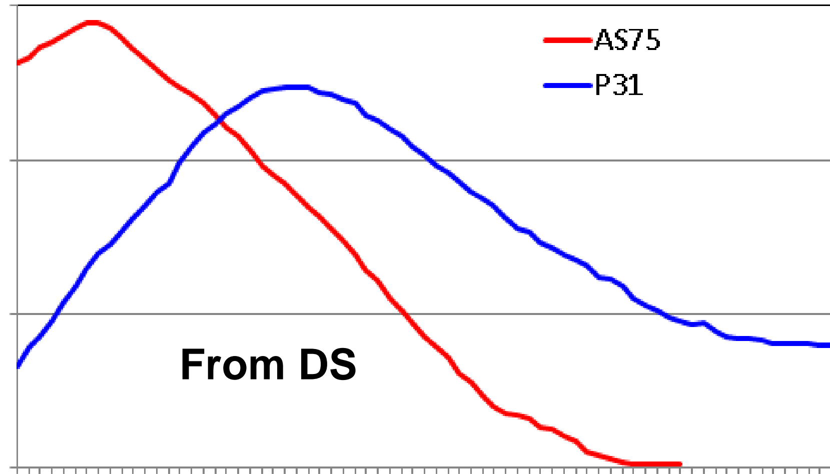








- Individual doping profiles for OVERMOS/DECAL were obtained using SPROCESS, to simulate a (simplified) CMOS fabrication by TowerJazz
- These (1D) doping profiles were then implemented in SDE
- Huge reduction in mesh size and computation time
- Some approximations as a result but more affordable for big 3D simulations



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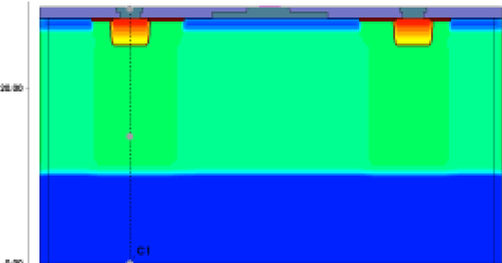

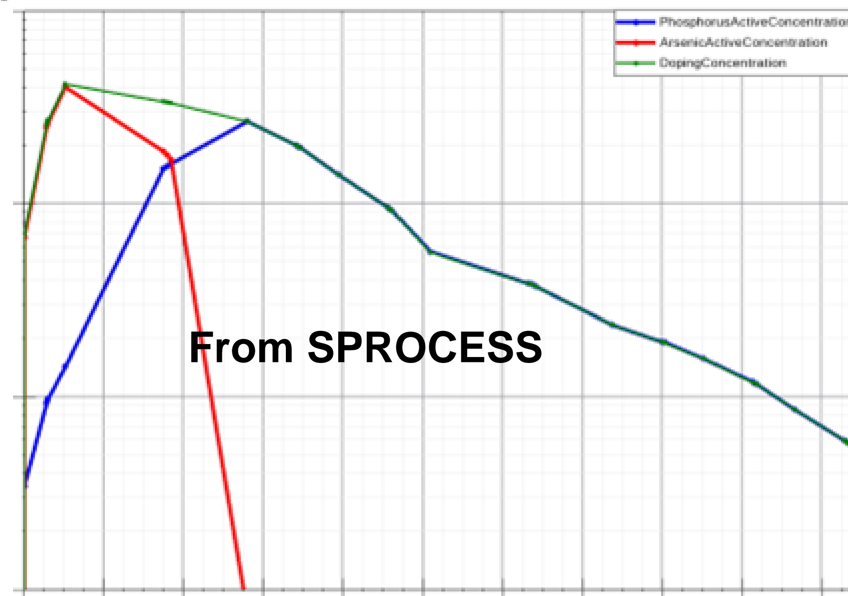

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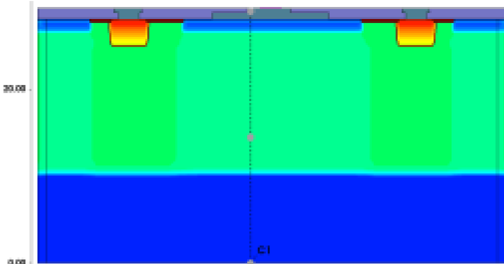

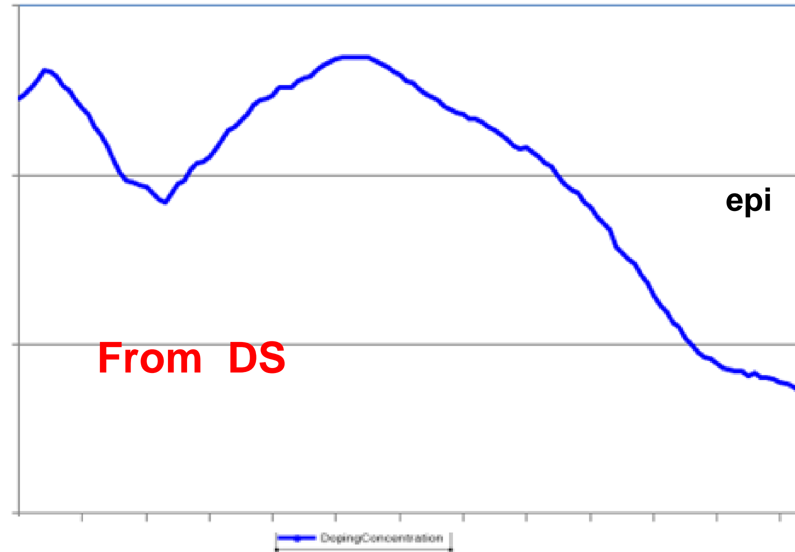

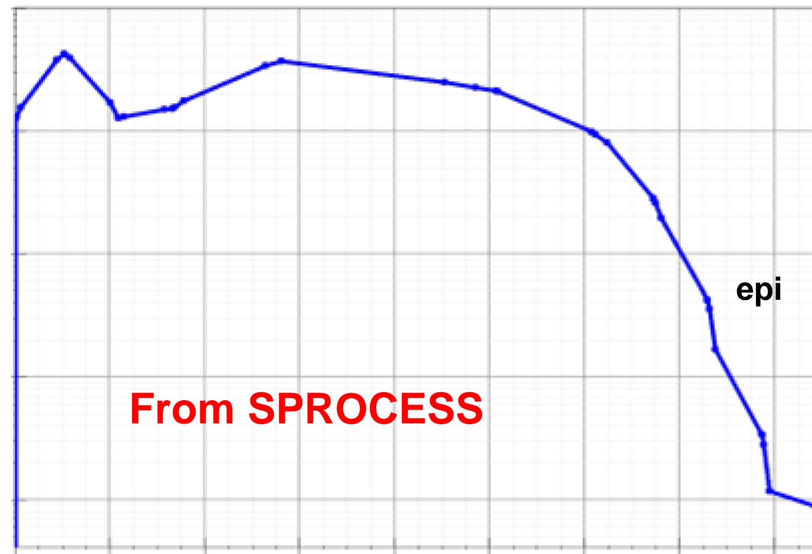

- SPROCESS: used the same process steps but starting on an EPI of different doping than standard

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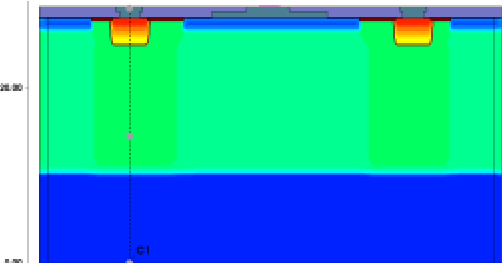
EPI-BULK

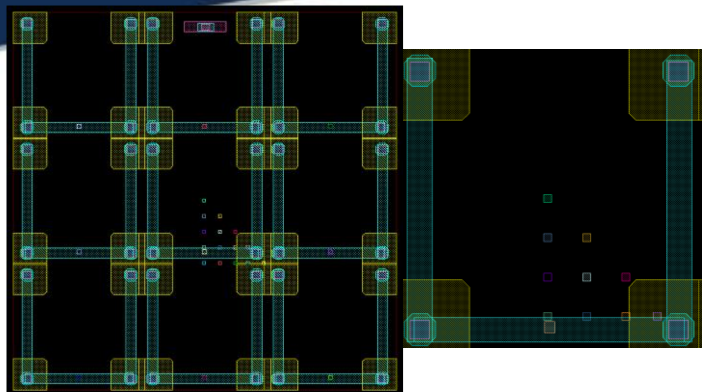


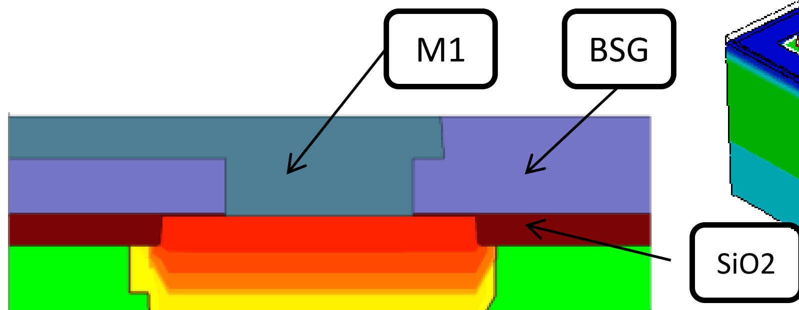
PhosphorusActiveConcentration
ArsenicActiveConcentration
DopingConcentration

EPI region

SUB region

From SPROCESS





10V

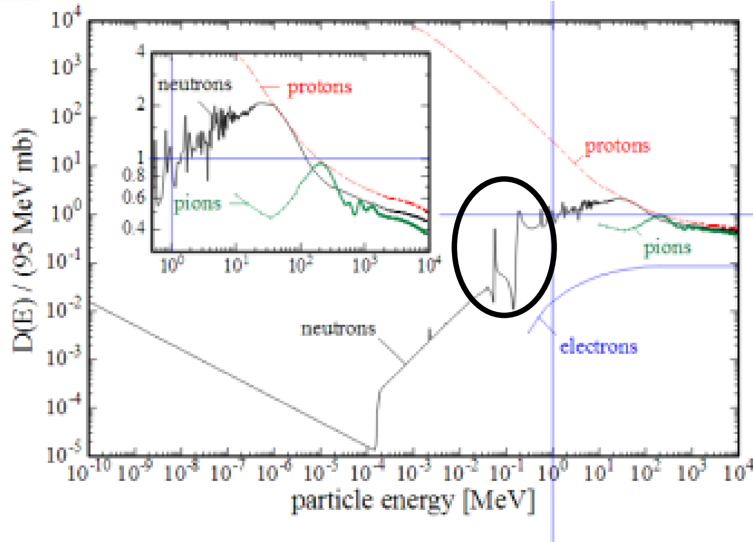
0V

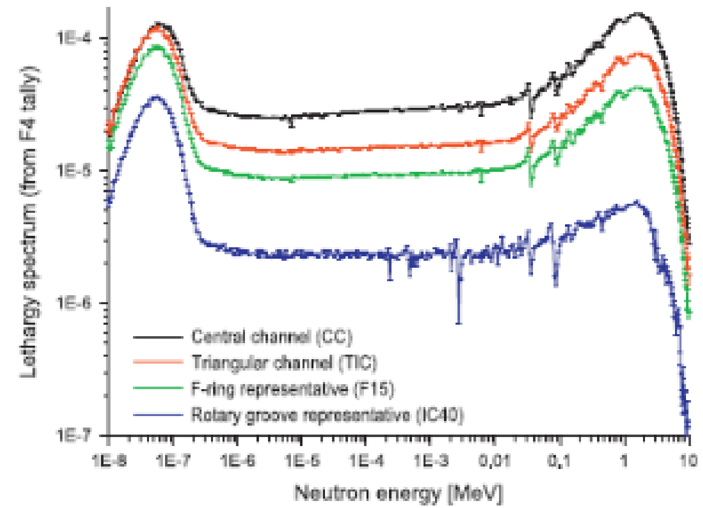
OVERMOS 1.0 3x3 pixel array simulation

- Pixel size 40x40um2
- EPITAX thick **18um**, medium/high resistivity P-type
- STI 400 nm
- SUBS thick **10um**
- MESH size: 555139, up to M1
- BSG dielectric

```
Traps (( eNeutral Level EnergyMid = 0.39  fromMidBandGap Conc = @<2.42*@RadiationFluence@>@
ElectricField eXsection=1e-14 hXsection=5.5e-13   )
          ( eNeutral Level EnergyMid = 0.13  fromMidBandGap Conc = @<3.55*@RadiationFluence@>@
ElectricField eXsection=2e-15 hXsection=1.2e-14   )
          ( eNeutral Level EnergyMid = 0.035 fromMidBandGap Conc = @<0.581*@RadiationFluence@>@
ElectricField eXsection=1.2e-15 hXsection=1.2e-14 )
          ( hNeutral Level EnergyMid = -0.045 fromMidBandGap Conc = @<0.523*@RadiationFluence@>@
ElectricField eXsection=1.2e-14 hXsection=1.2e-14
         ( hNeutral Level EnergyMid = -0.2 fromMidBandGap Conc = @<2.42*@RadiationFluence@>@
ElectricField eXsection=1.5e-14 hXsection=2e-14 )
```

- **TCAD Radiation simulation:**
  - Radiation model used : 24 GeV p+
  - 3 acceptors traps and 2 donor traps with concentration $\propto \Phi$
  - Neutron irradiation on OverMOS devices performed at Ljubljana. Fluences: 2E14, 5E14,1E15



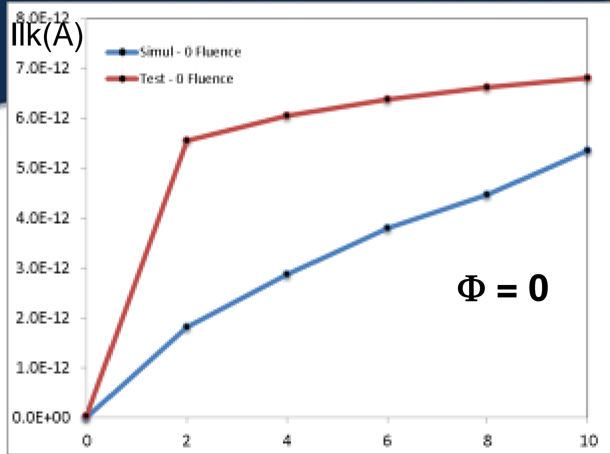


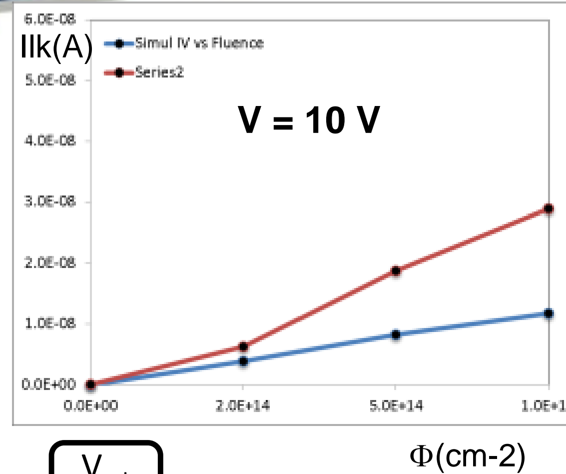
Normalization of TRIGA reactor spectrum to 1 MeV n-eqv:

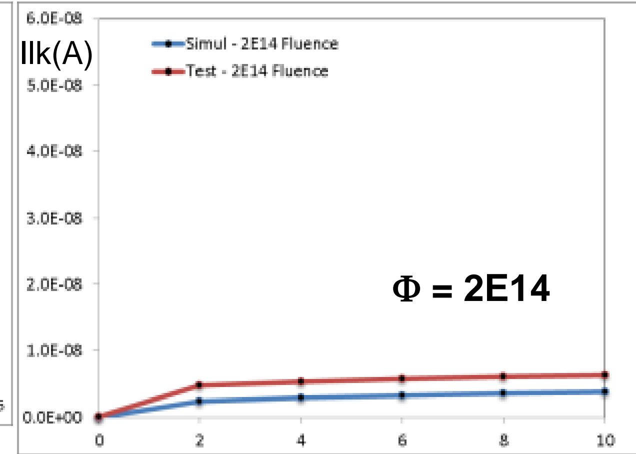
TRIGA	**1 MeV n eqv coeff ~0.75**	**24 GeV p+ eqv ~0.5**
2E+14	1.5E+14	3E+14
5E+14	3.75E+14	7.5E+14
1E+15	7.5E+14	1.5E+15

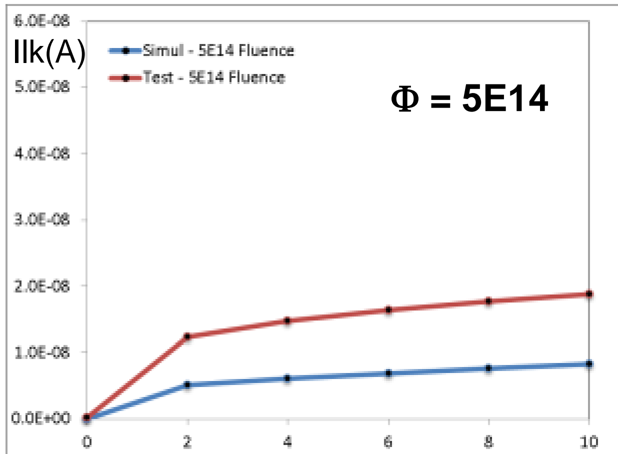
3x3 array simulation: compare TCAD results with experimental results: I_{lk} from **8** pixels around the central pixel

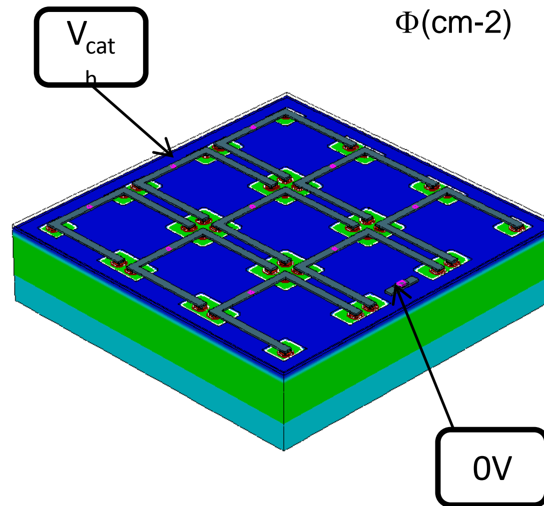
- **TCAD Radiation simulation:**
  - **Ilk vs. n-eqv fluence : 0, 2E14, 5E14,1E15**
  - **Breakdown Voltage**

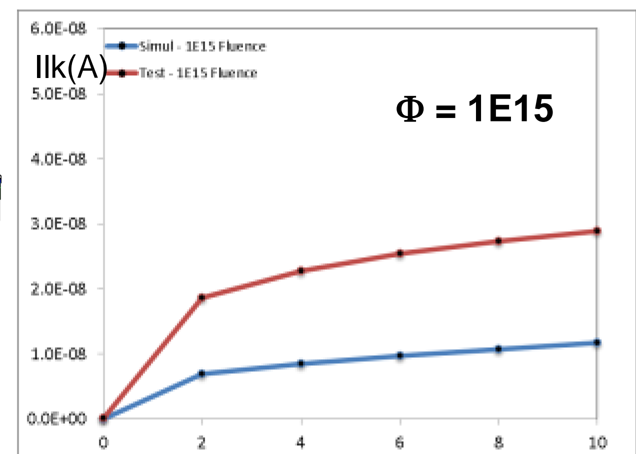




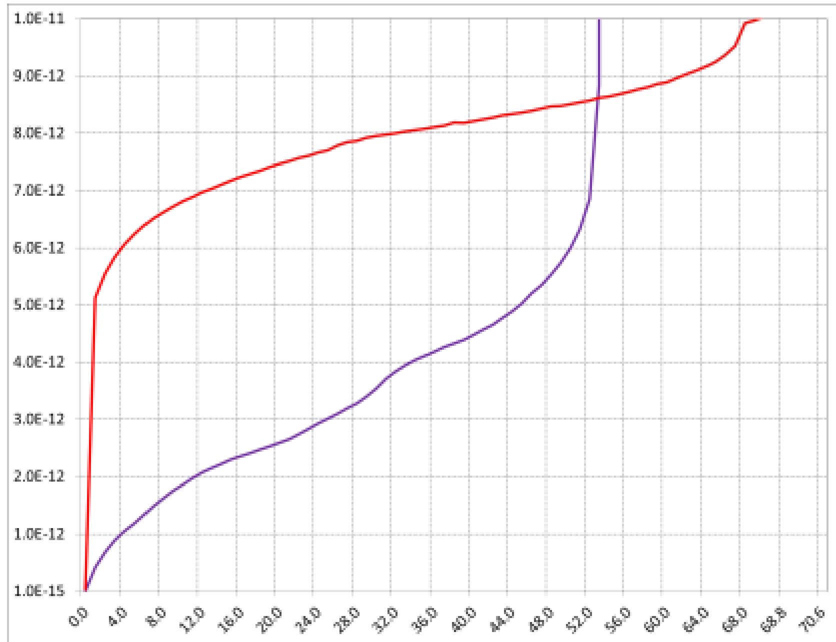


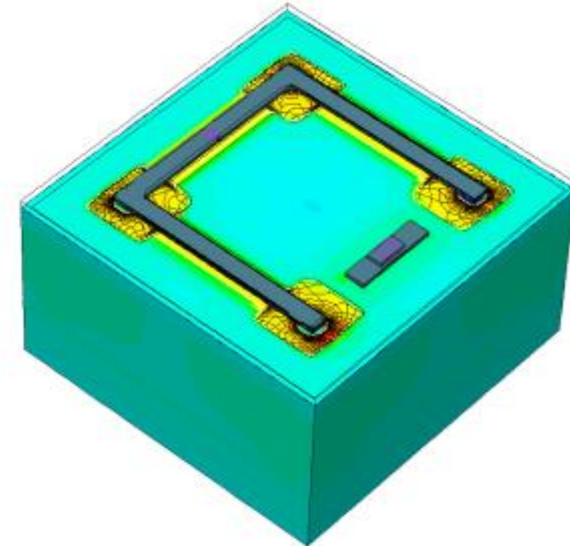




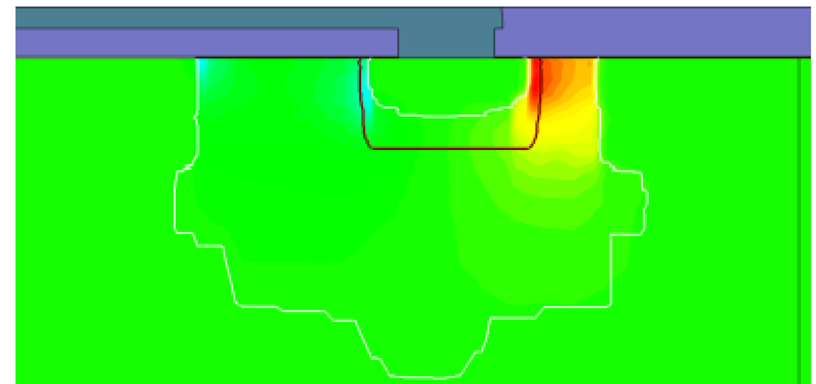


- TCAD Radiation **simulations** and **Test** results comparison @ T = 300K
- Not a (too) bad result, considering the several uncertainties in (Silicon technology, fluence…) (~ factor of **3** off)
- It is crucial to know the technology and properly implement it into TCAD
- It is crucial to implement the ‘right’ radiation models

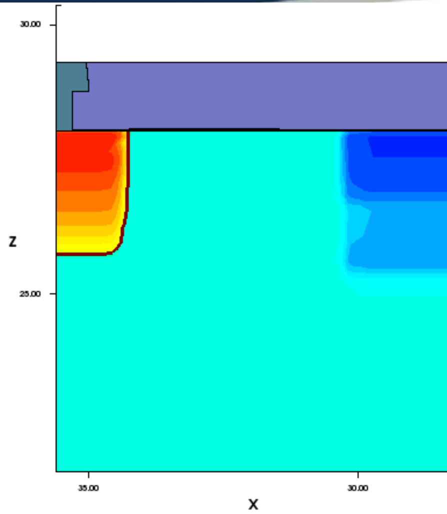


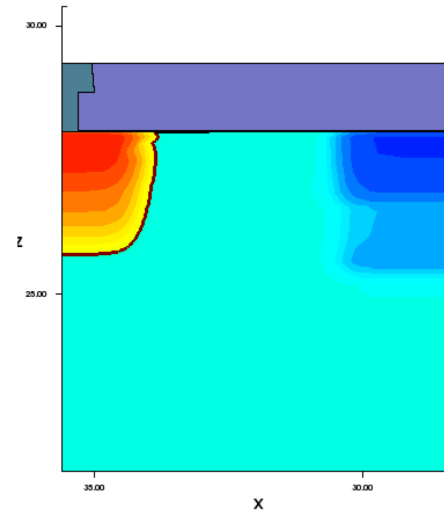


ElectricField-Y (V*cm^-1)



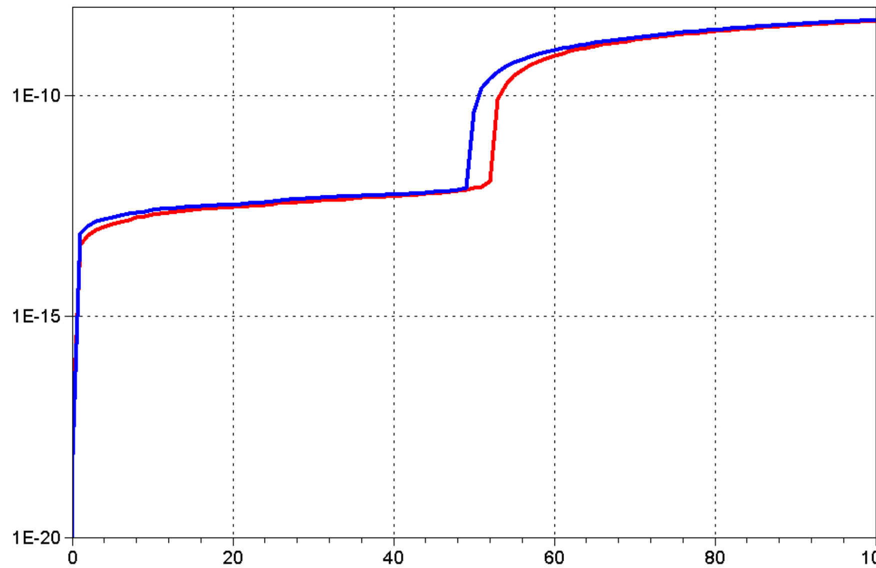
BV for test structure ~ 68 V
BV for TCAD structure ~ 52 V

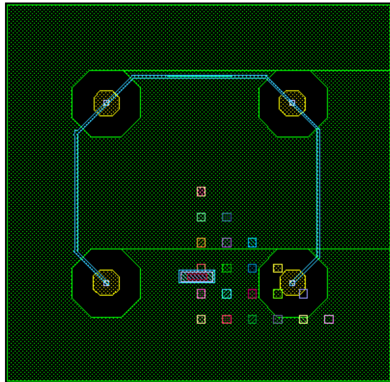


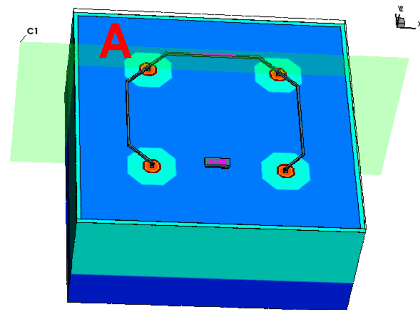


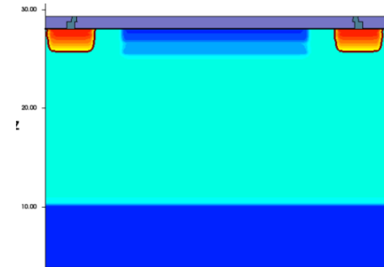
LF = 01
BV~ 52 V

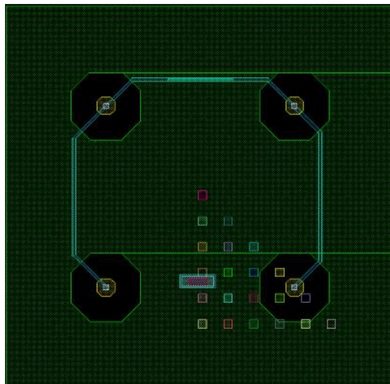
LF=03
BV ~ 49 V

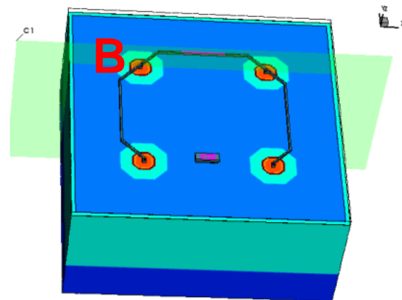


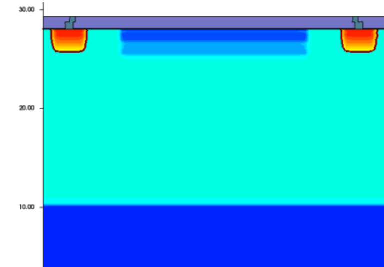






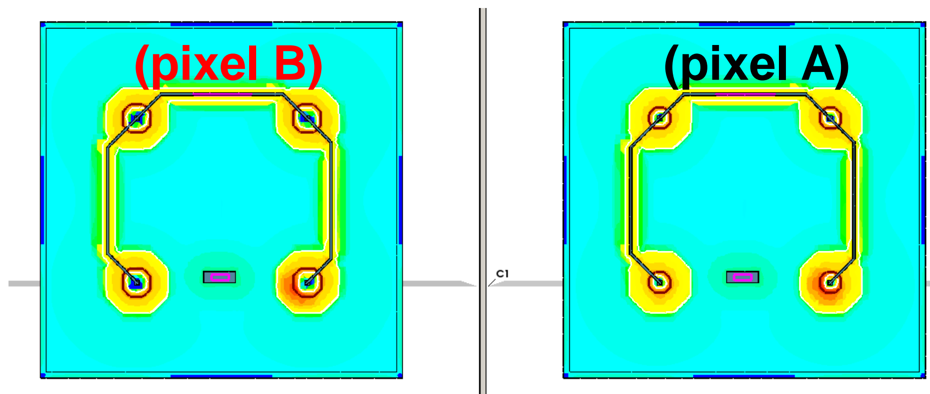


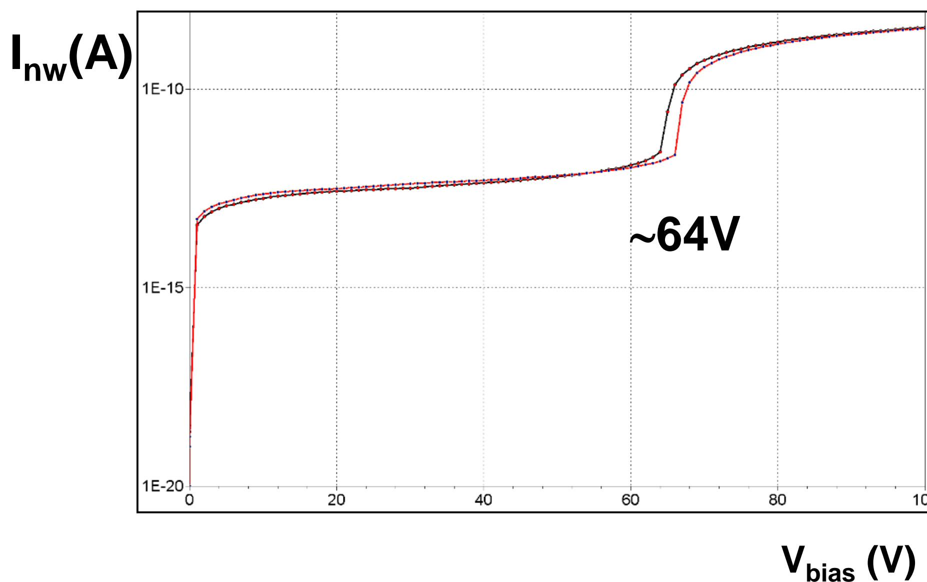


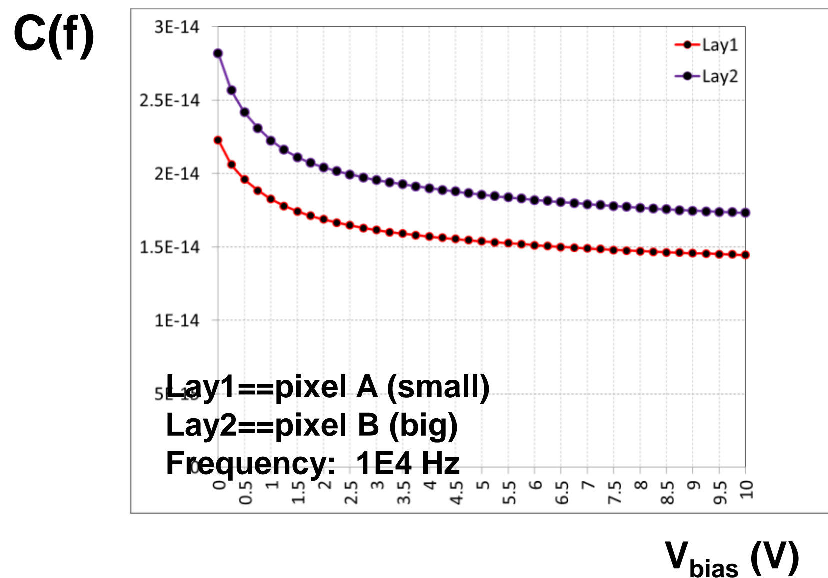


- **DECAL** pixel studies
- Investigation of 2 pixel layouts

DECAL single pixel
Avalanche breakdown studies (Rseries = 1E10 Ohm)







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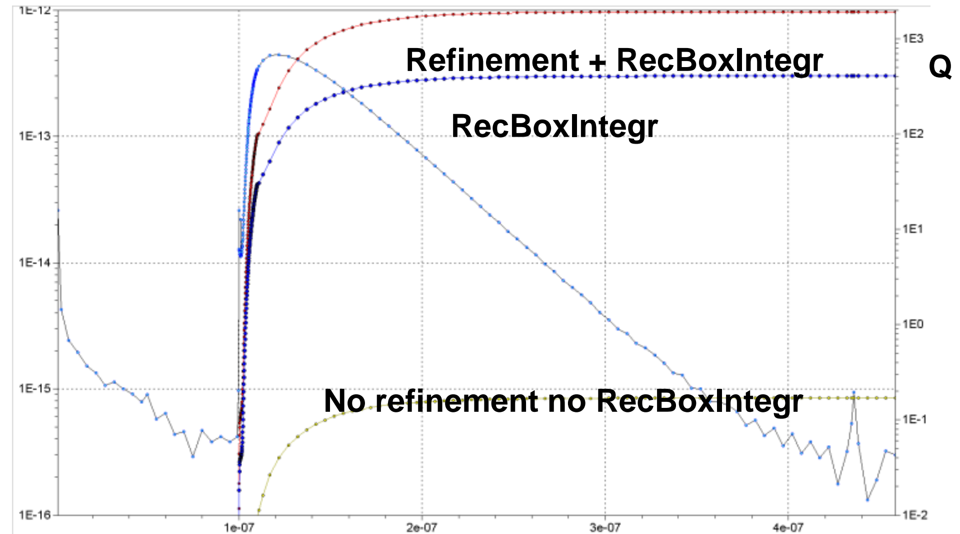
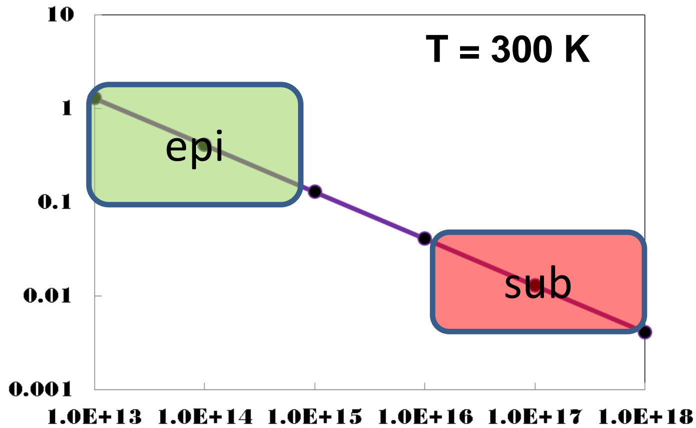
Charge collection simulation
<80> /um generated
21 hitting points simulated
Refinement along particle track
Size wt_hi*K1
Spatial Resolution Ld*K2
Time Resolution tdr

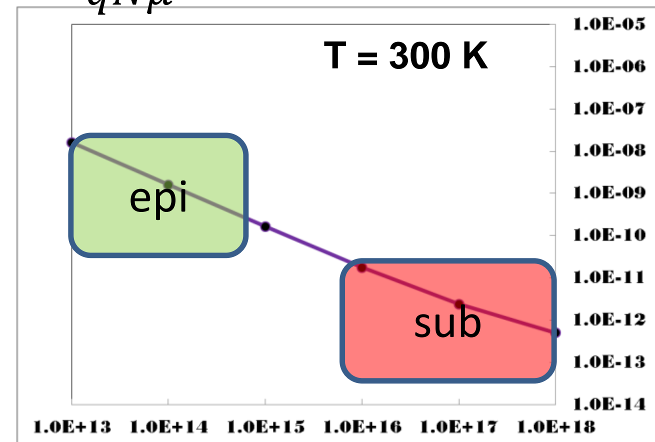
$$L_D = \sqrt{\frac{\varepsilon k_B T}{q^2 N}} \qquad C * L_D$$



$$t_{DR} = \frac{\varepsilon}{qN\mu}$$

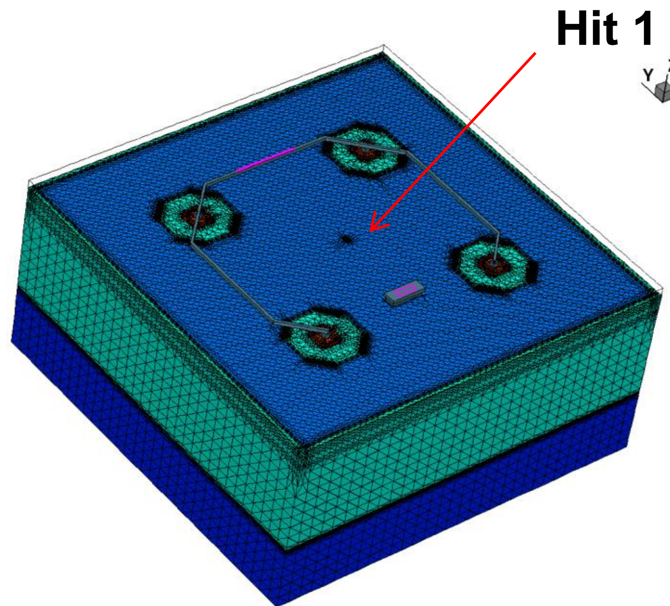


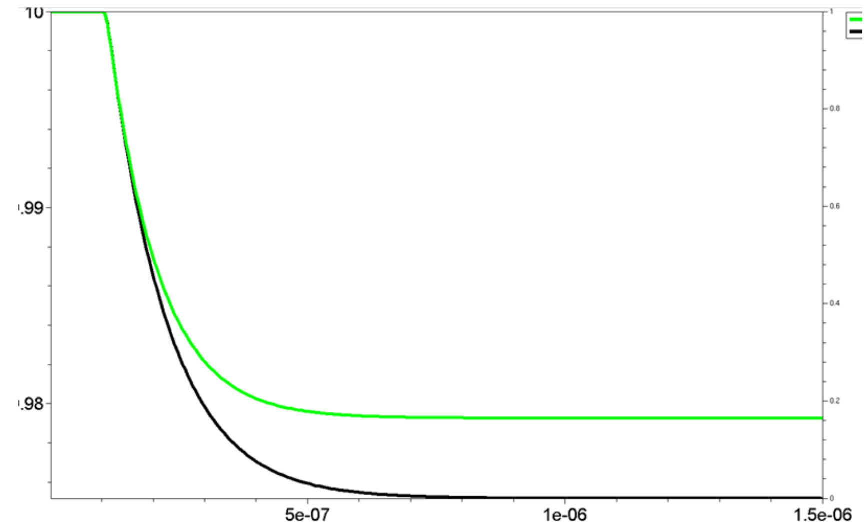
Debye length (um) vs. Doping (cm-3)



Dielectric relaxation time (s) vs. Doping (cm-3)

Charge collection simulation with SRH disabled
<80> /um generated
3 hit points simulated (central and close to boundaries)
The minimum spatial meshing ~ 1 x Debye length (Epi), ~ 50 x Debye length (Sub)
The initial temporal meshing is 50 ps
In all cases the Qgen = 2240 e (<80>*(10(sub)+18(epi)))
Qcoll is Qgen *(1+/- 0.1%)





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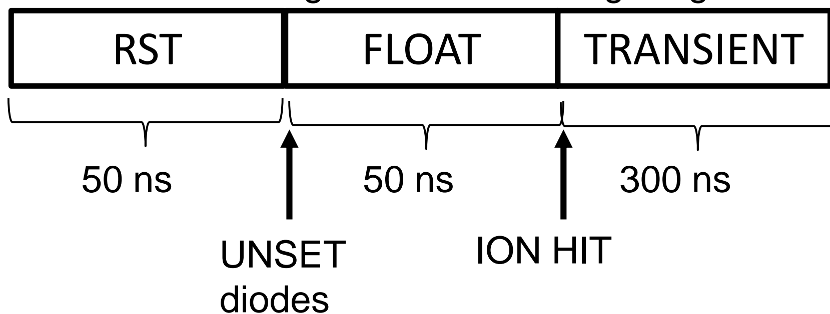
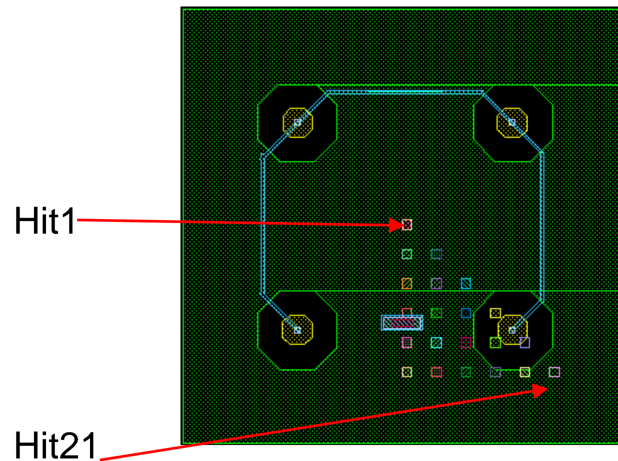
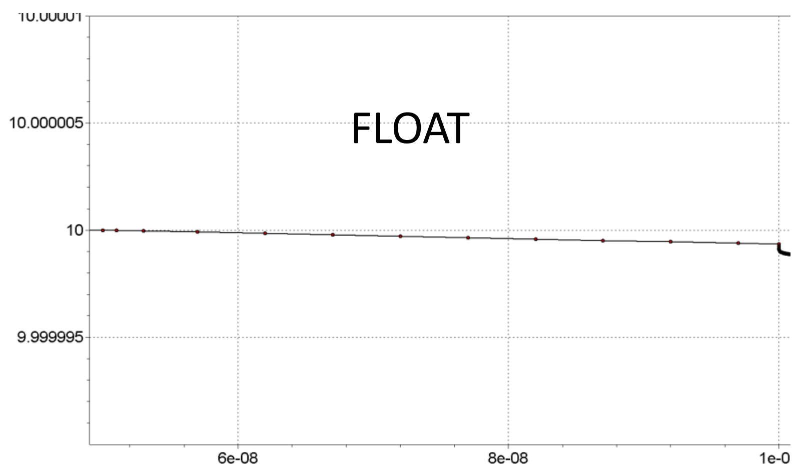
Charge collection simulation with SRH enabled
21 hitting points simulated, 4um steps

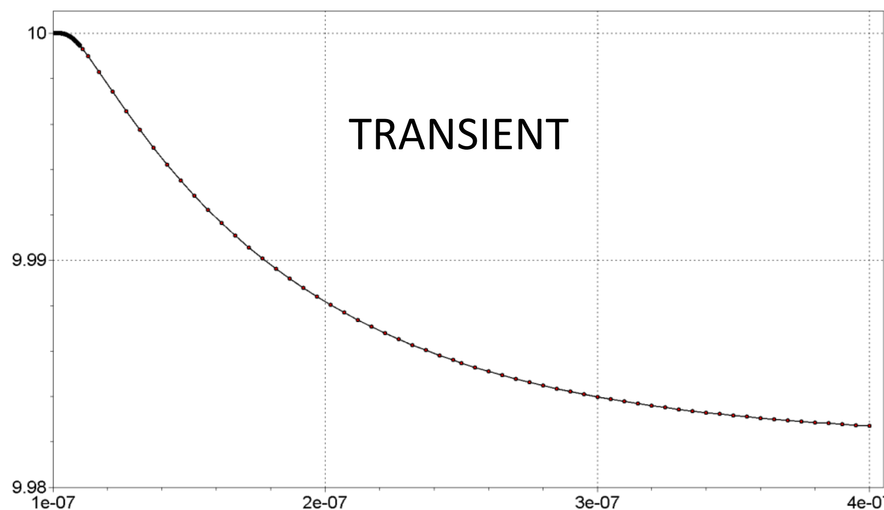
Single cell simulation

- Transient and Charge collection Voltage Signal









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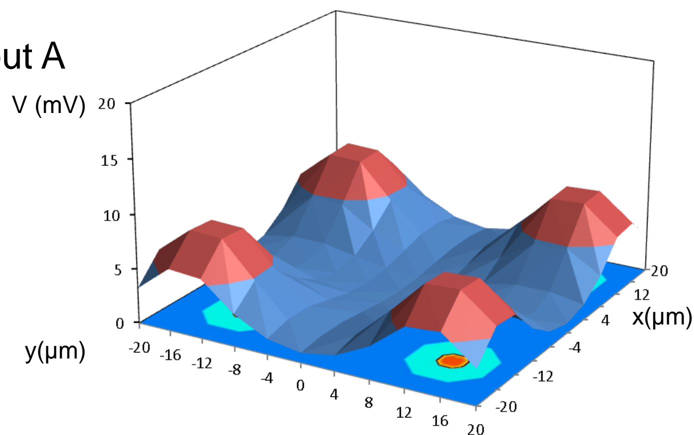
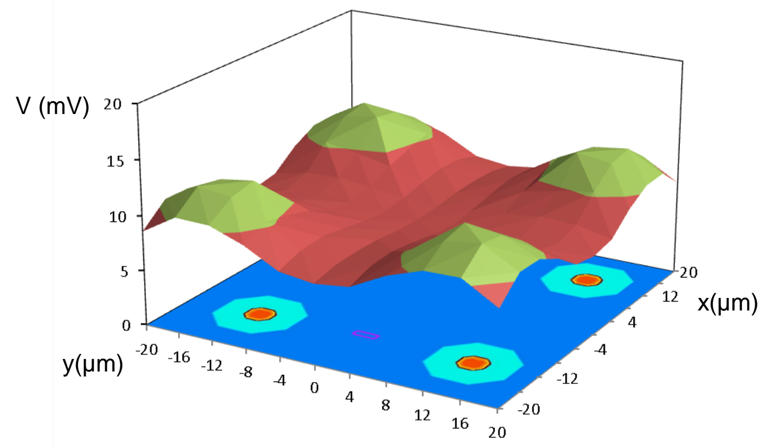
Charge collection simulation: V_{drop} (x,y)

Layout A

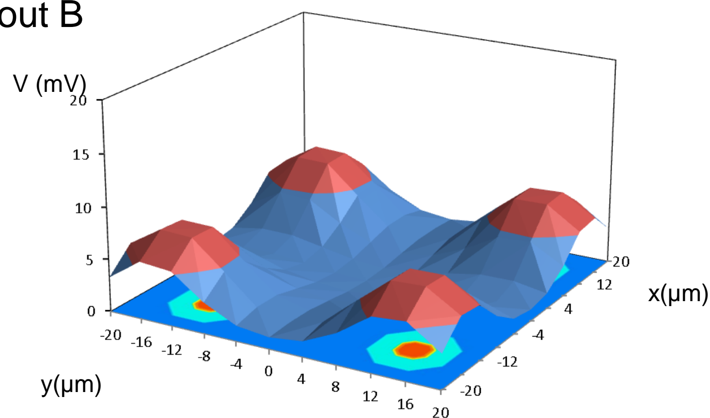


<ΔV>=3.449 mV Δ t=10 ns

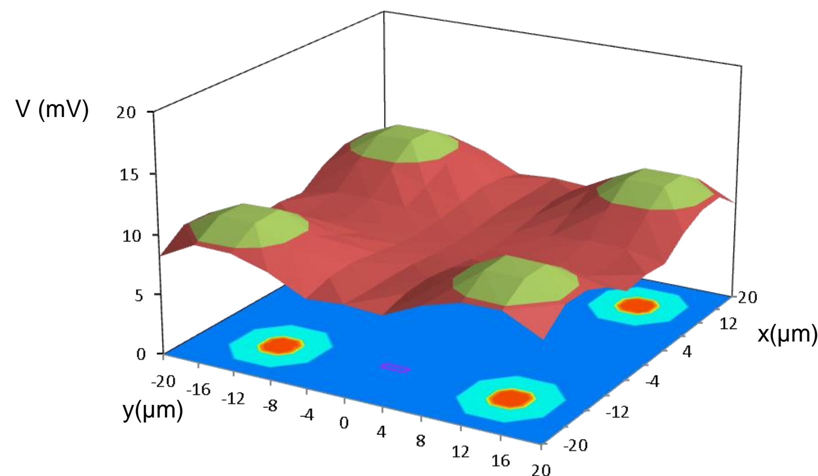


<ΔV>=9.991 mV Δ t=50 ns

Layout B



<ΔV>=3.348 mV Δ t=10 ns



<ΔV>=8.803 mV Δ t=50 ns

P -1e13

FZ

P -1e14

FZ

P -1e15

CZ

P -1e16

CZ

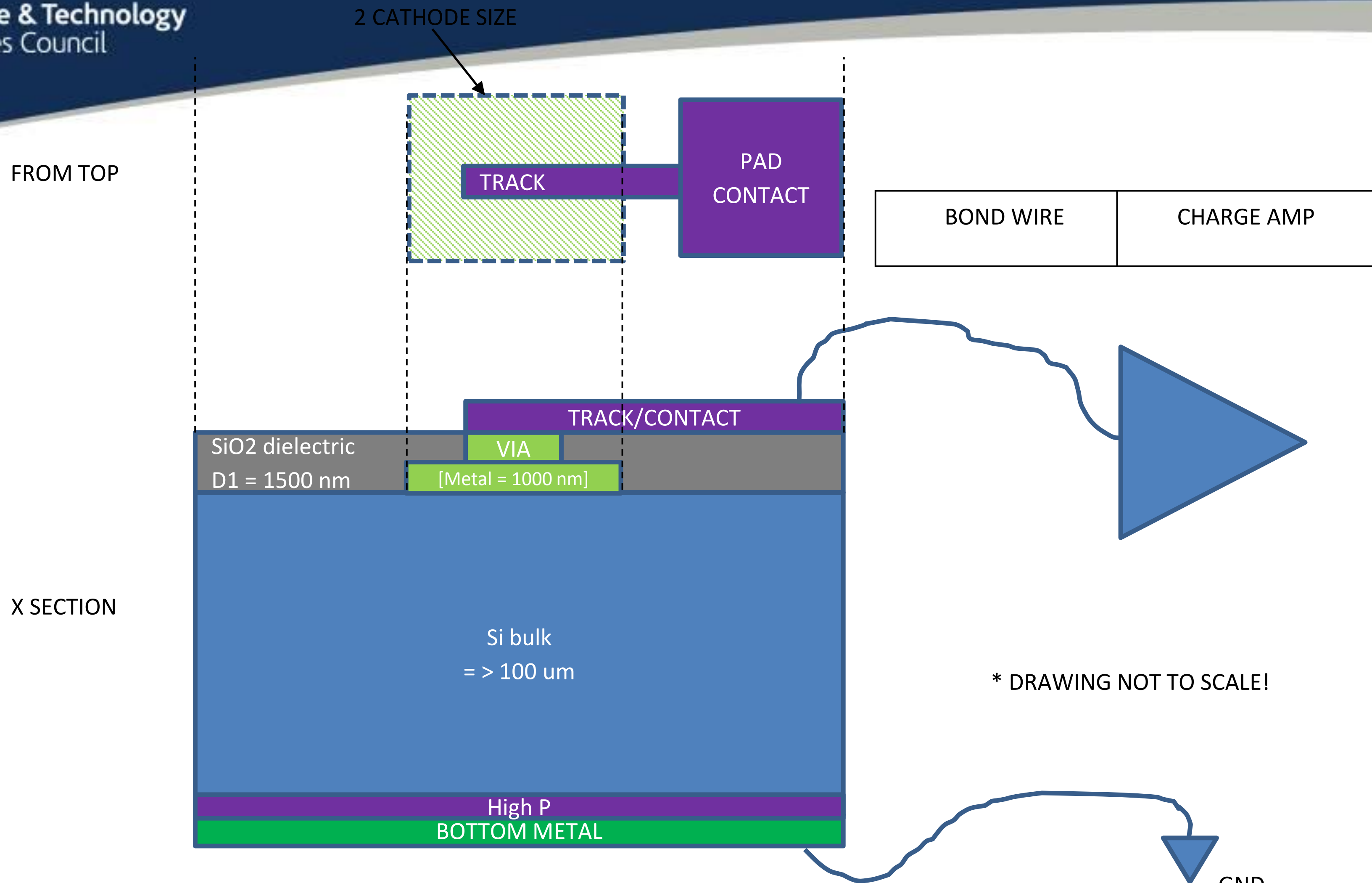
P -1e17

CZ

- Schottky diode for Radiation damage studies
- Silicon substrate of doping levels comparable to those used in CMOS technology (1E13 – 1E17) to study radiation damage effects
- The (3 inch) Si wafers are P type doped with different doping levels : 1E13, 1E14, 1E15, 1E16, 1E17.
- The devices on each wafer are the same (i.e. two flavours) only the wafer doping changes

On each wafer, the devices could be as follows:

- Flavour 1, ‘big’ size devices (DLTS)
- Flavour 2, ‘small’ size devices (CCE)
- Each device is within a say 5 x 5 mm2, which still should guarantee >100 devices / wafer



- X section: Al (or other metal) vias through the SiO2 connect to Al track on top (for wire bonding)
- The **Metal** contacting Si substrate could be Al/Ni or metal to make good Schottky contact with barrier high enough for DLTS studies
- High doping at the back / ohmic contact + bottom layer metalized to allow grounding of the substrate

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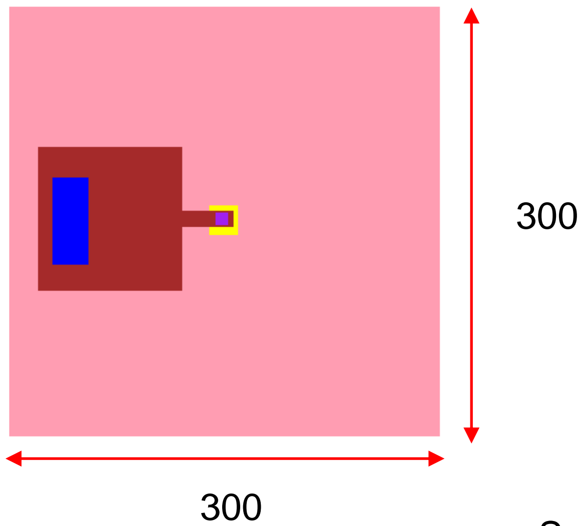
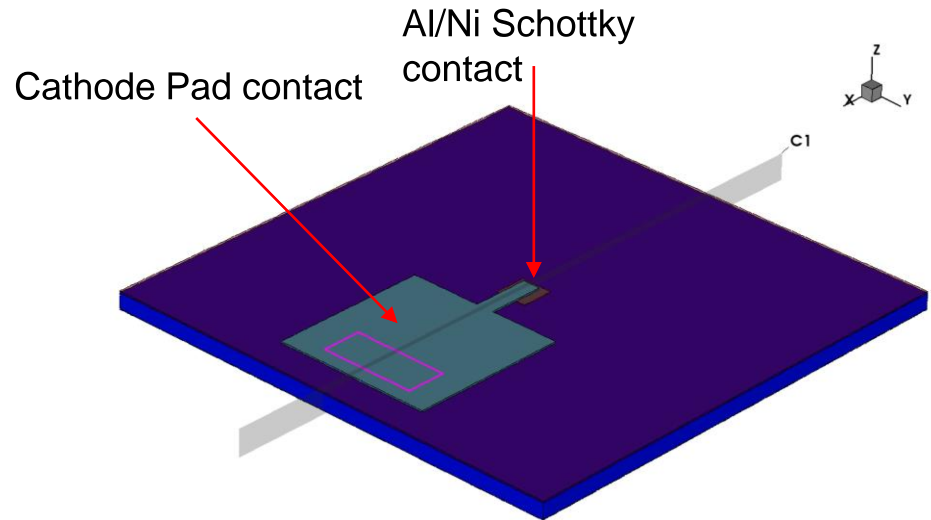
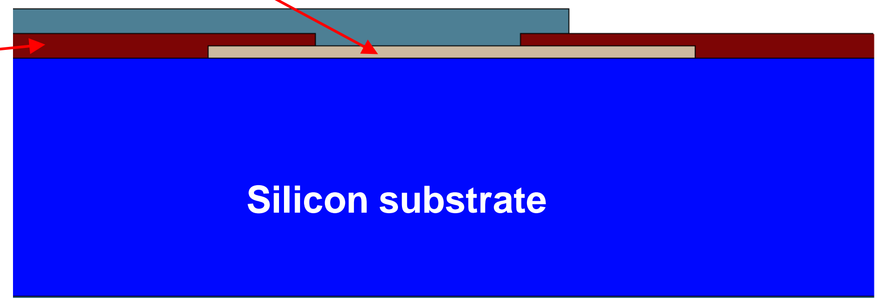




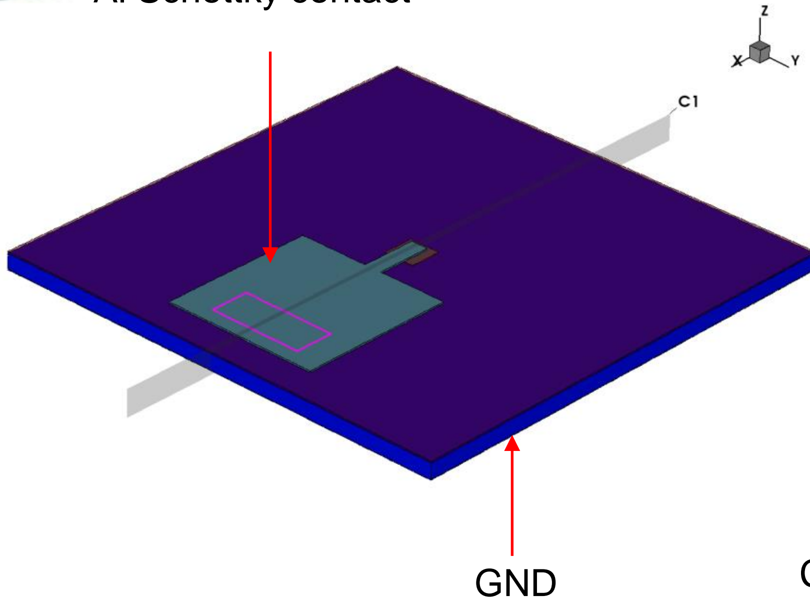
Schottky junction (Ni/Pt/…)

SiO2

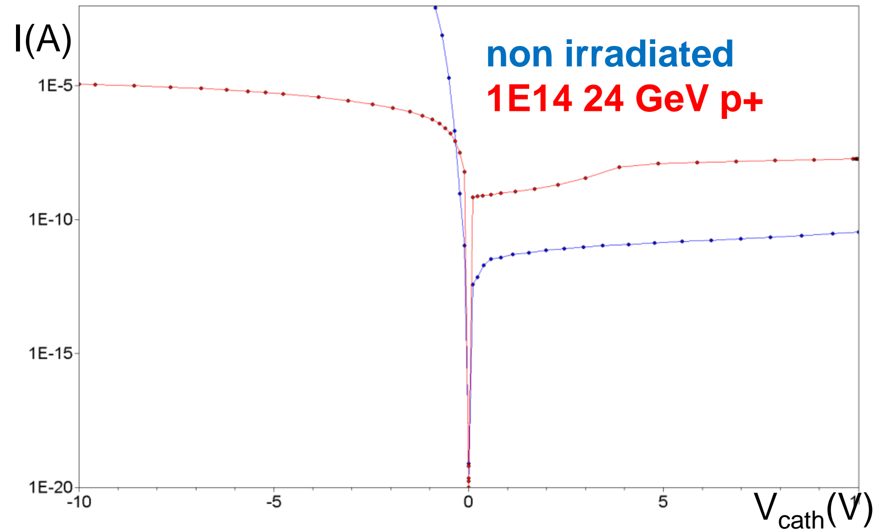


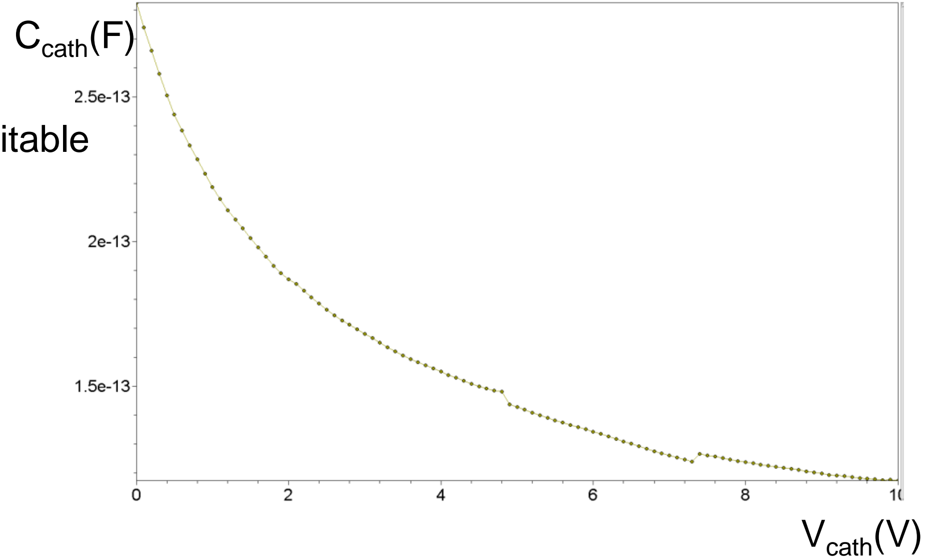
Anode Ohmic contact

Al Schottky contact



Al cathode





Metal to use to have Schottky junction suitable for DLTS studies:

Al : Φ_m =4.1eV
Ni : Φ_m =5.01eV
Pt : Φ_m =6.35eV
…?

Conclusions

- TCAD simulation of CMOS devices (OVERMOS/DECAL).Further work needed to improve modeling
- Fabrication of Schottky diodes to investigate radiation effects and develop models for CMOS simulation