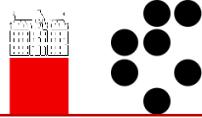


Radiation hardness of a CMOS sensor process for a novel Depleted Monolithic Active Pixel Sensor

RD50 Workshop, Krakow, 07.06.2017

Bojan Hiti (Jožef Stefan Institute, F9, Ljubljana, Slovenia) on behalf of
R. Bates, I. Berdalovic, B. Blochet, C. Buttar, R. Cardella, M. Dalla, N. Egidos, B.
Hiti, J. Willem Van Hoorn, T. Kugathasan, I. Mandic, D. Maneuski, C. Marin
Tobon, K. Moustakas, L. Musa, H. Pernegger, P. Riedler, J. Rousset, C. Riegel, C.
Sbarra, D. Schaefer, E.J. Schioppa, W. Snoeys, T. Wang, N. Wermes

HV-CMOS at HL-LHC

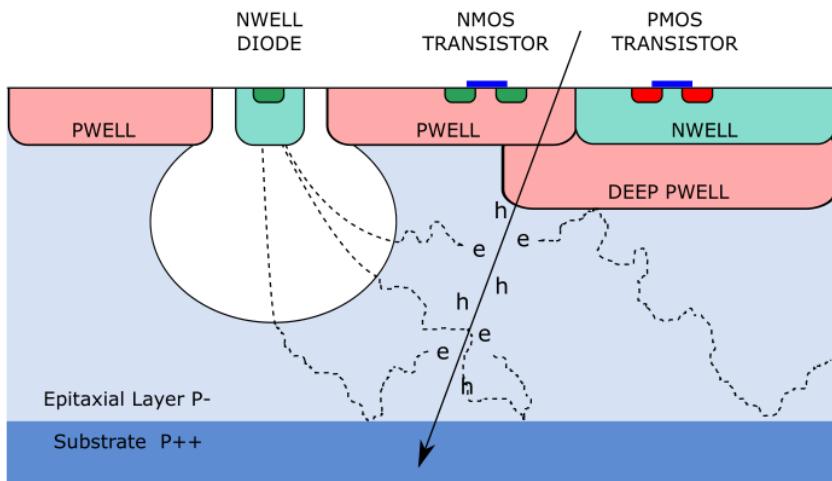
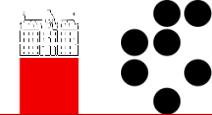


- Active sensors an interesting option for ATLAS Phase II pixel upgrade
- Challenging radiation environment

	ATLAS - LHC	ATLAS HL-LHC	
		Outer ($r > 10$ cm)	Inner ($r = 3.3$ cm)
NIEL (n_{eq} /cm 2)	2×10^{15}	10^{15}	2×10^{16}
Ionizing dose (Mrad)	80	50	> 500

- Requirements:
 - Charge collection by drift
 - Radiation hard electronics design
 - Compatibility with the rest of ATLAS ITk
- "Drop-in" CMOS detector planned for outermost ATLAS pixel layer

TowerJazz 180 nm Investigator



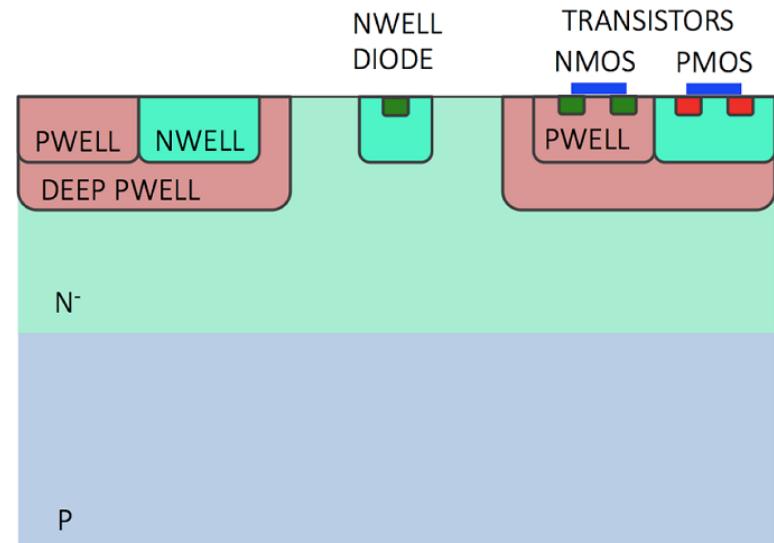
ALICE ITS Upgrade TDR

- DMAPS evolved from ALPIDE chip for ALICE ITS upgrade
- Small fill factor, low capacitance design (5 fF)
 - Higher gain, faster response, higher Q/C
 - Potentially lower power consumption
 - Important to ensure efficient charge collection, especially on pixel edges

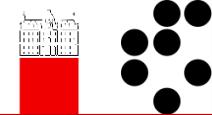
C. Gao et al., NIM A (2016) 831

<http://www.sciencedirect.com/science/article/pii/S0168900216300985>

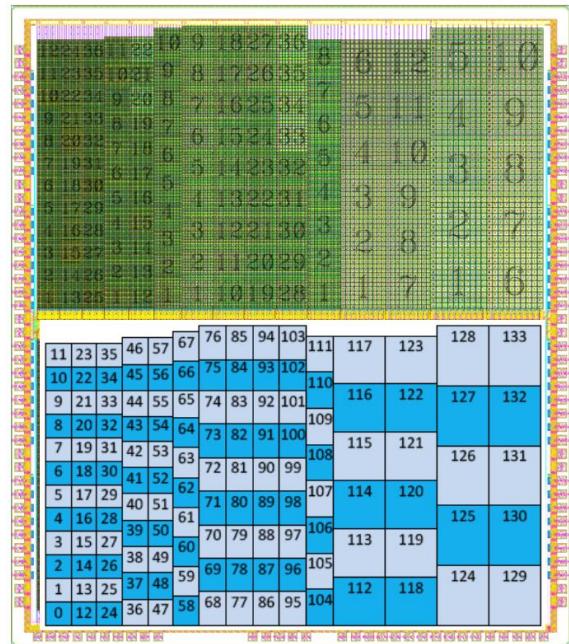
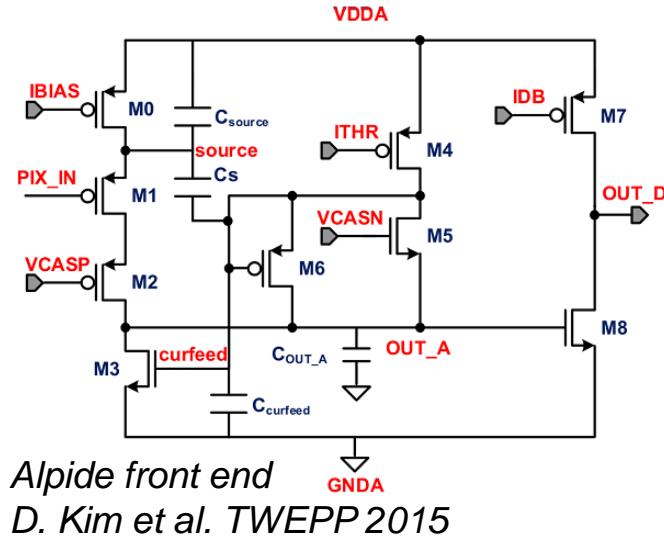
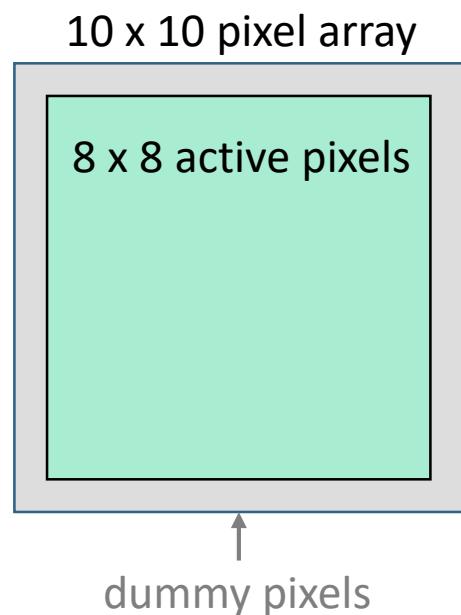
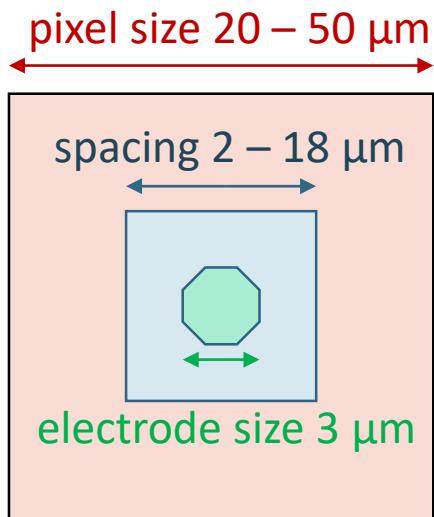
- Modified process
- Additional n-layer to generate a deep junction, maintaining low C
- Significantly improved charge collection after irradiation
- No significant circuit or layout changes required

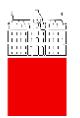


TowerJazz 180 nm Investigator



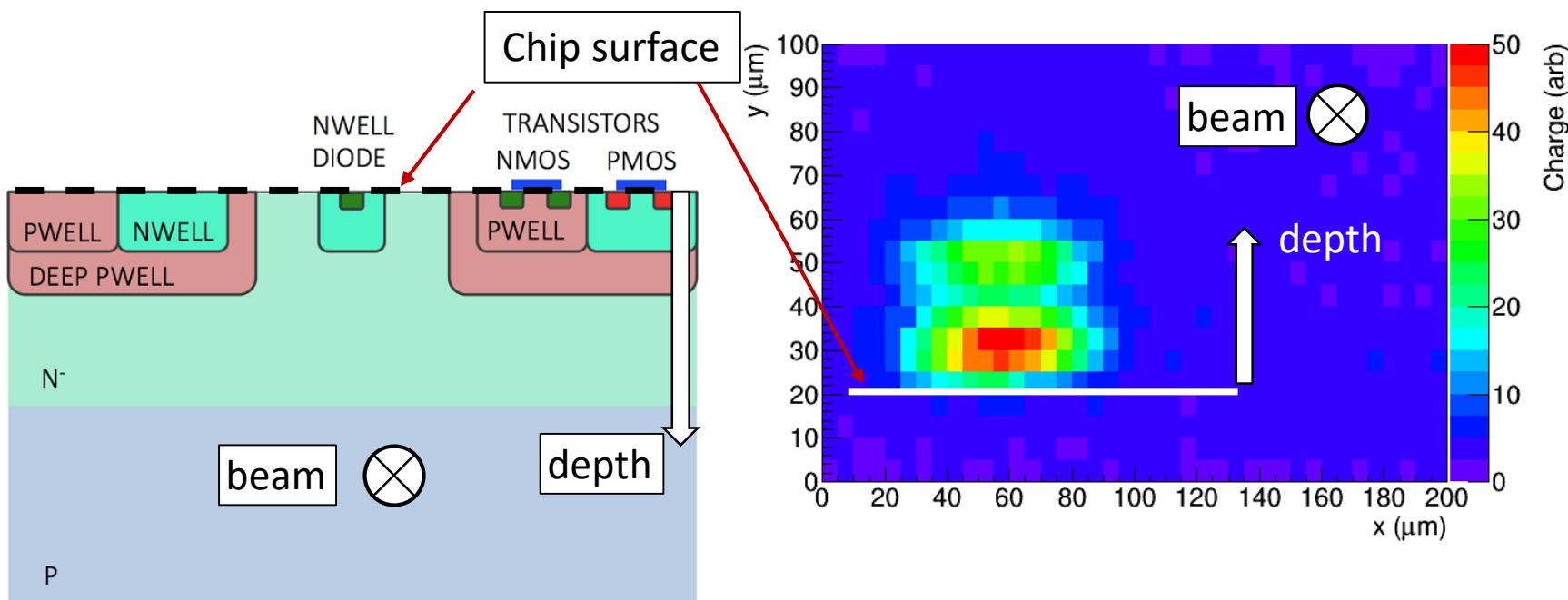
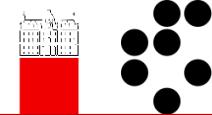
- Charge collection in a thin 25 µm epi-layer (high resistivity)
- Maximal bias voltage 6 V
- Internal charge sensitive amplifier (CSA) in pixel cells
- Investigator chip consists of > 250 test matrices with different pixel flavours
- Charge collection tests with E-TCT, source measurements and test beam





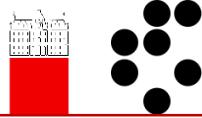
E-TCT

E-TCT principle

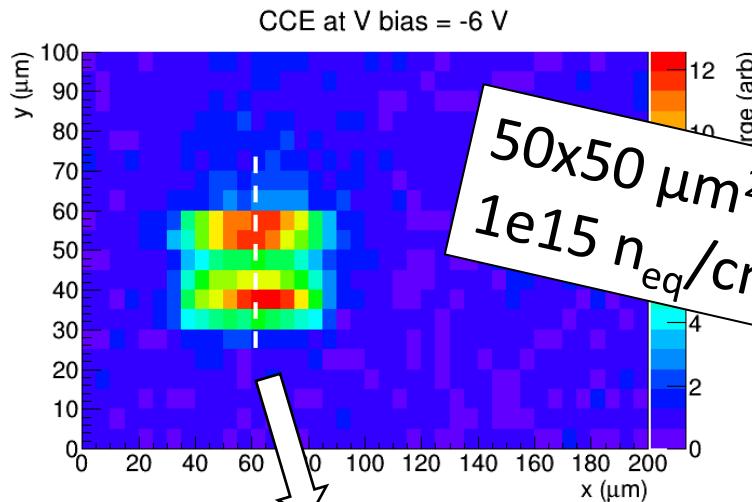


- Inject charge carriers into the sample with laser light from sample edge
- Readout individual pixels
- Can study response uniformity within the pixel
- TCT measurements made with chips from two wafers with different n-layer doping
 - W11 weakly doped, W16 strongly doped n-layer
- Neutron irradiated chips (Ljubljana):
 - $1e15, 2e15, 5e15, 1e16 n_{eq}/cm^2$

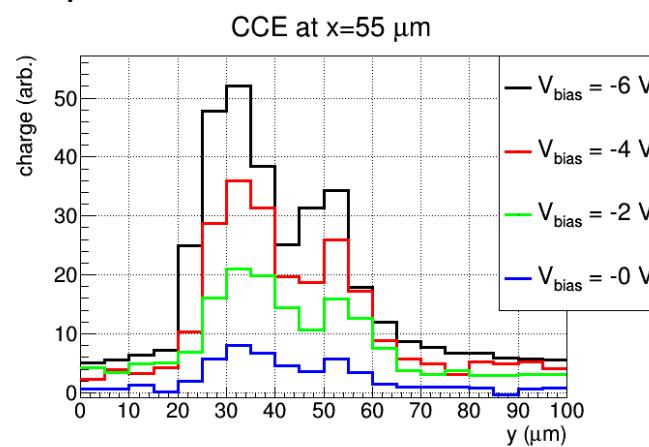
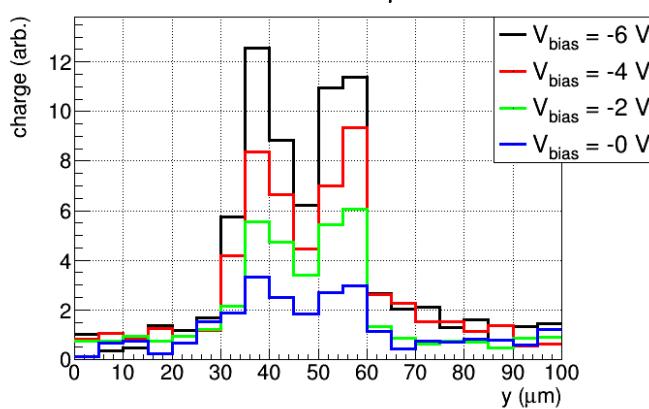
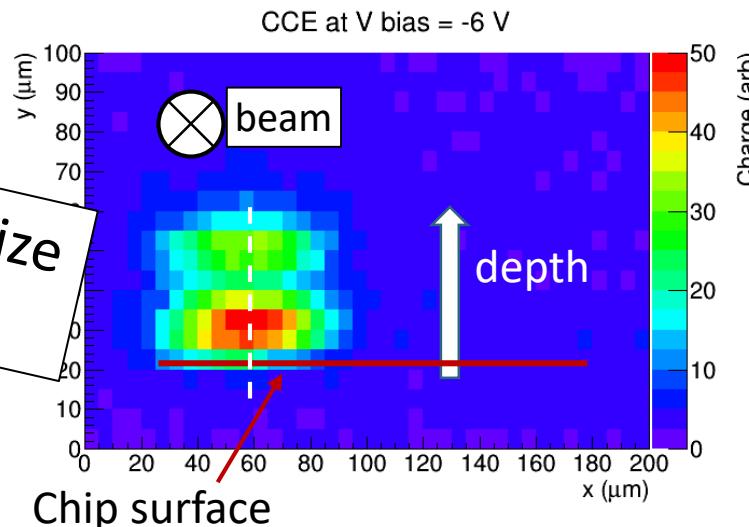
Results 1e15 – single pixel 50 x 50 μm^2



Wafer 11 (weaker n-layer doping)

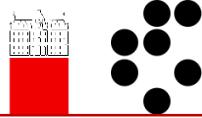


Wafer 16 (stronger n-layer doping)

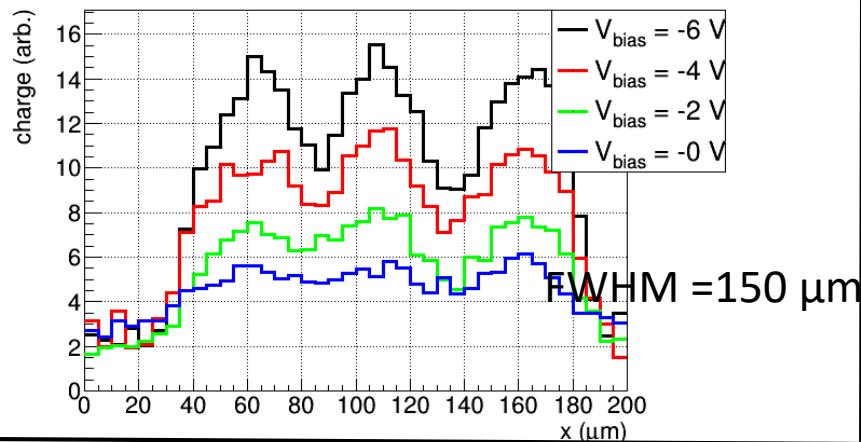
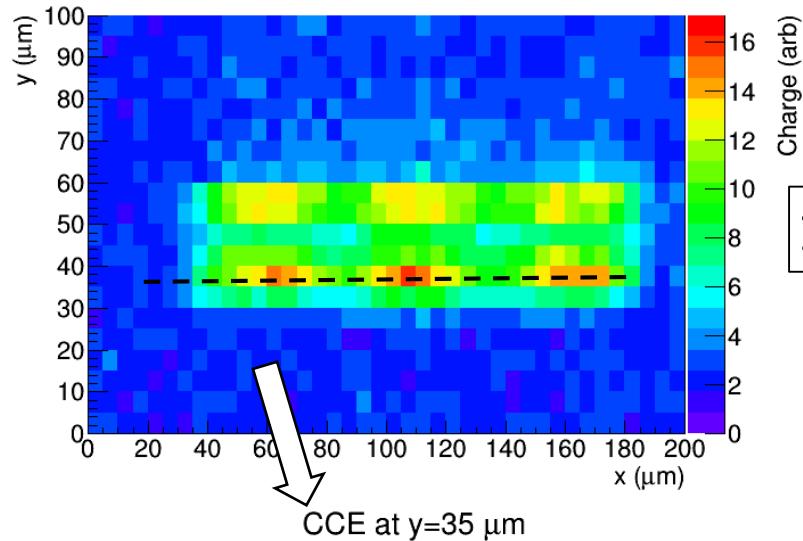


Both wafers have two peaks of charge collection along the depth (double junction)

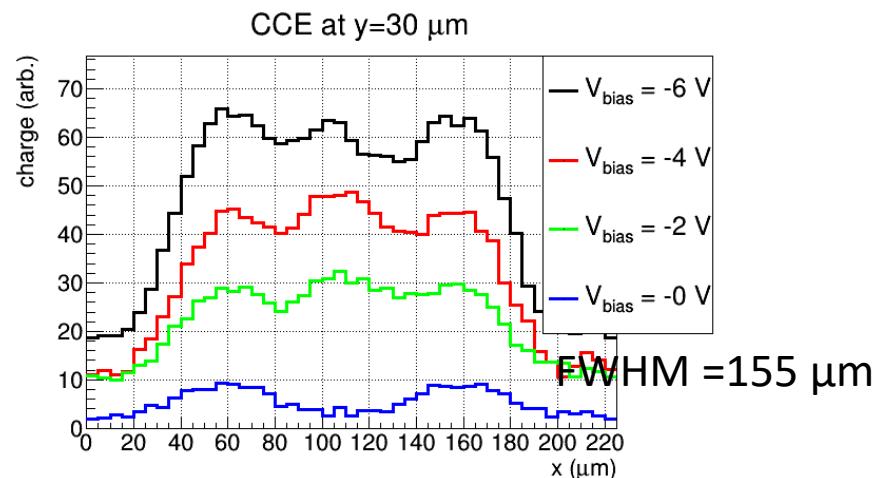
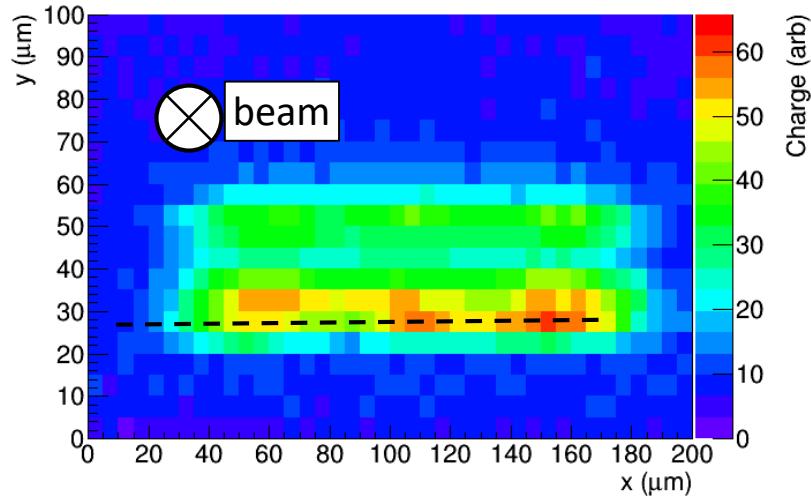
Results $1e15$ – 3 neighbours $50 \times 50 \mu\text{m}^2$



Wafer 11 (weaker n-layer doping)



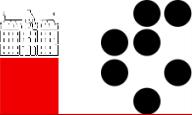
Wafer 16 (stronger n-layer doping)



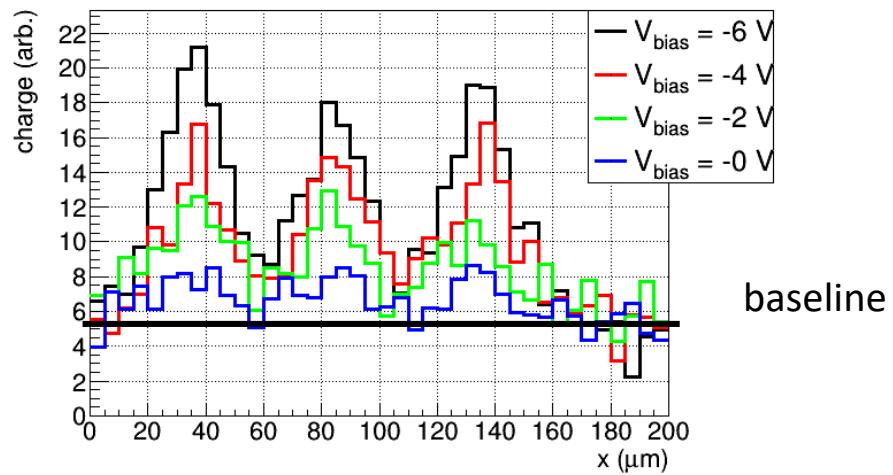
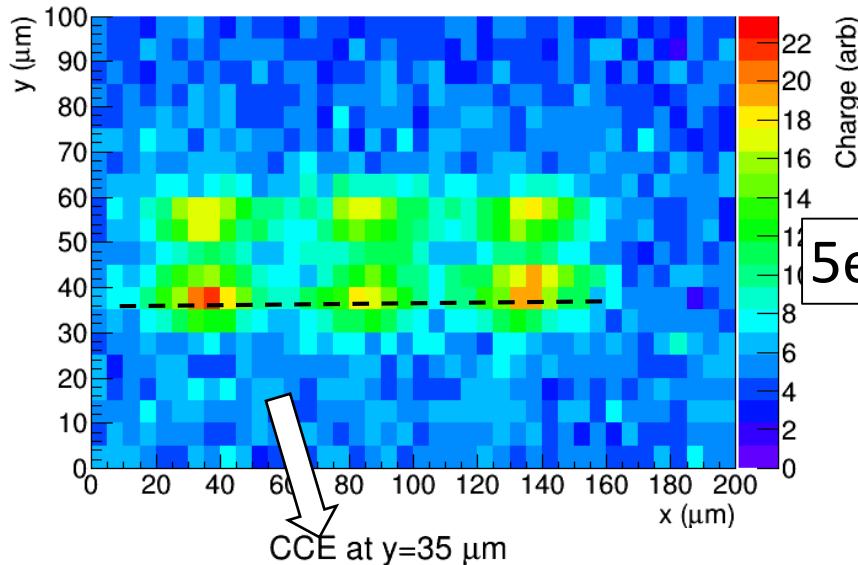
Pixels read out individually, signals summed offline

Charge uniformity between pixels is slightly better on W16

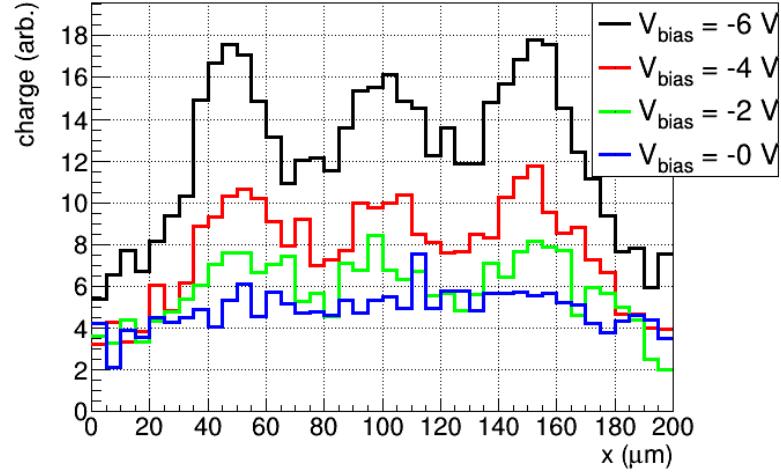
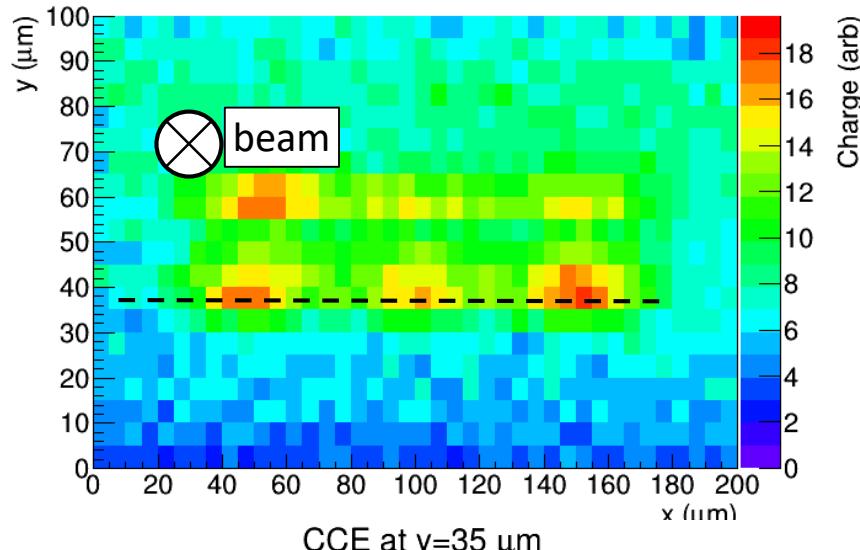
Results 5e15 – 3 neighbours $50 \times 50 \mu\text{m}^2$



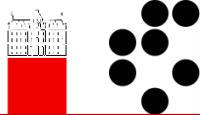
Wafer 11 (weaker n-layer doping)



Wafer 16 (stronger n-layer doping)

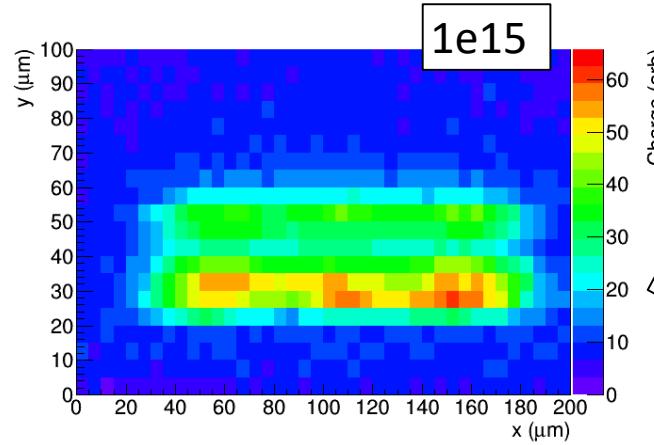
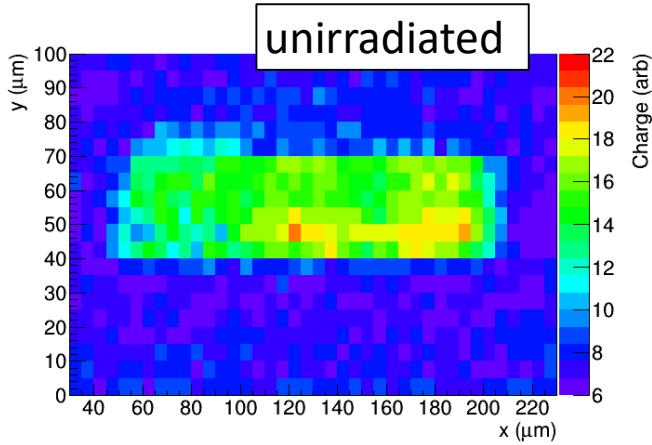


Charge uniformity between pixels is better on W16 (eff. $\approx 50\%$) than on W11 (eff. $\approx 20\%$)

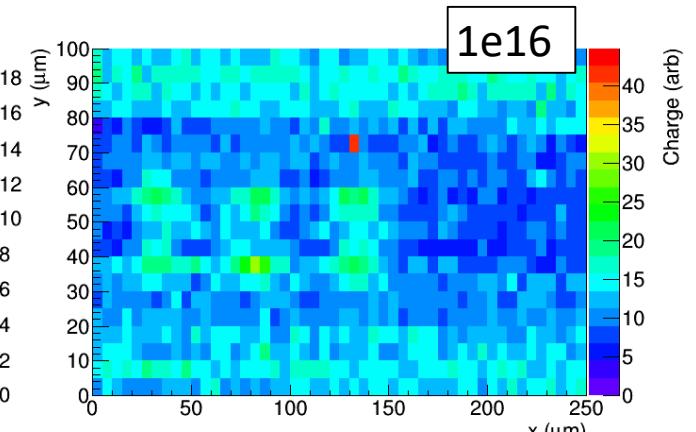
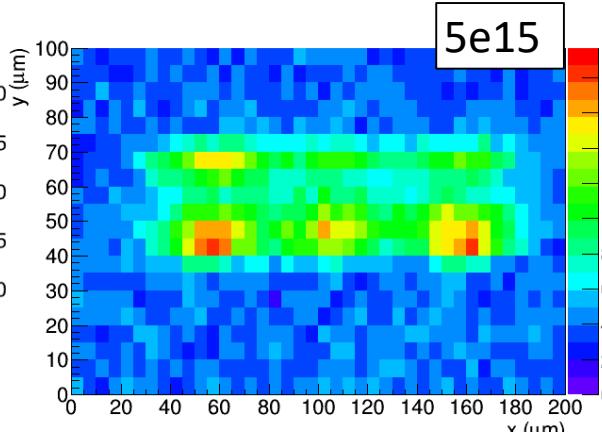
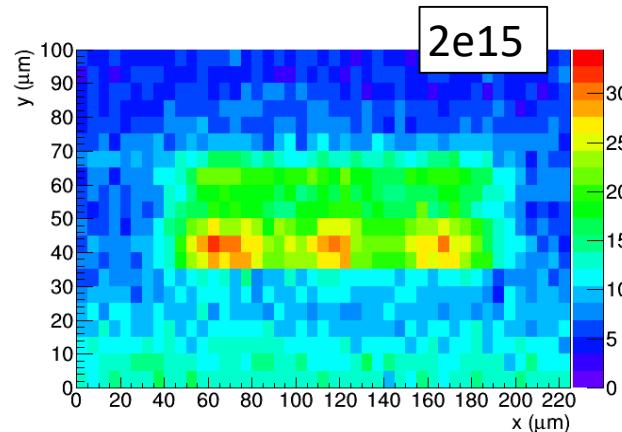


Summary for all fluences

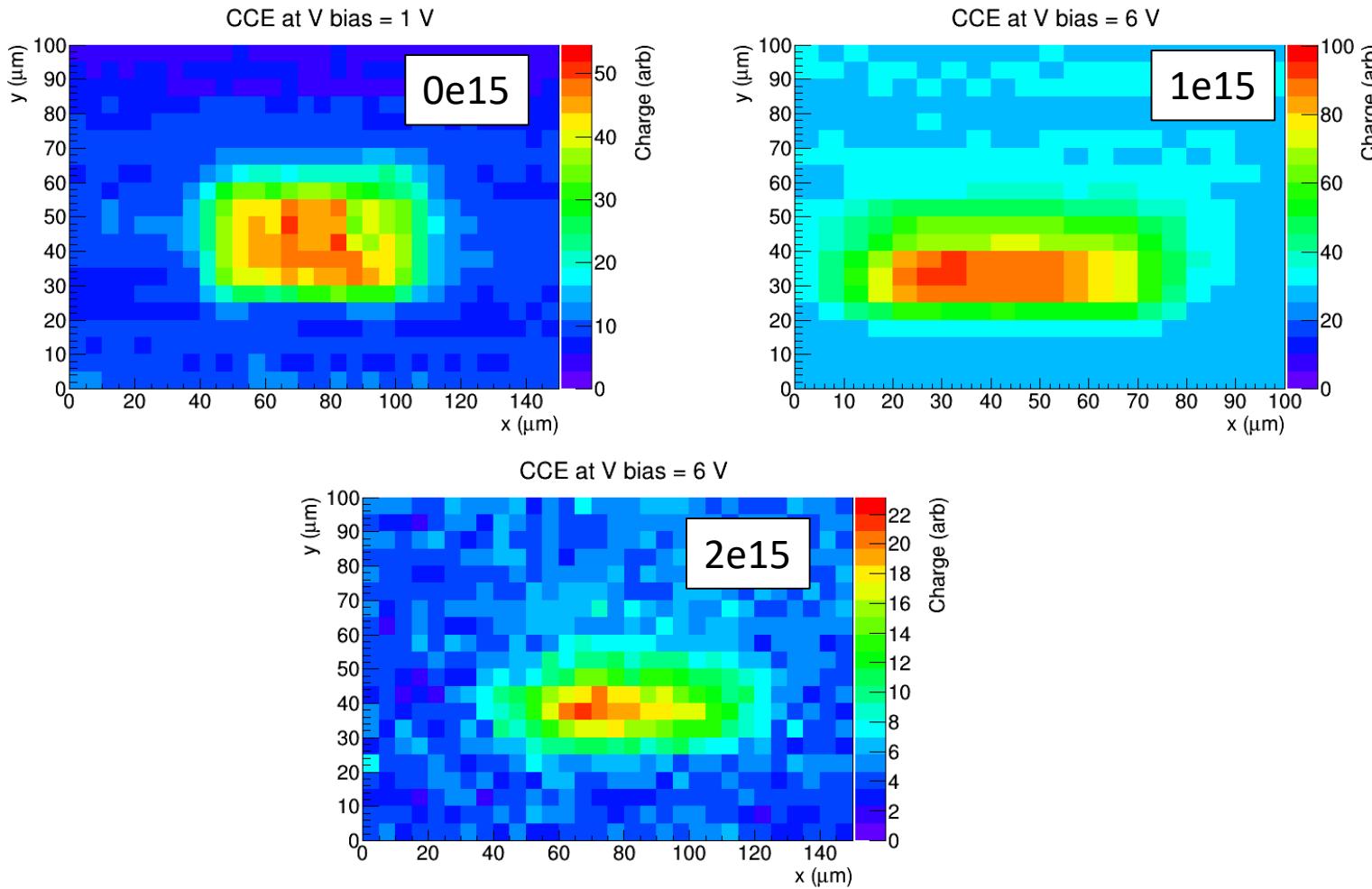
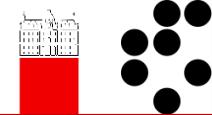
- Signals from three neighbour pixels ($50 \times 50 \mu\text{m}^2$ pixel size) summed together
- Neutron irradiated chips 0 – $1\text{e}16 \text{n}_{\text{eq}}/\text{cm}^2$
- Up to $5\text{e}15 \text{n}_{\text{eq}}/\text{cm}^2$ good response uniformity
- Higher charge collection at the front and at the back side of epi-layer seen (double peak)



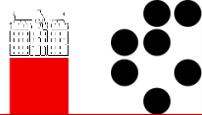
$V_{\text{bias}} = 6 \text{ V}$



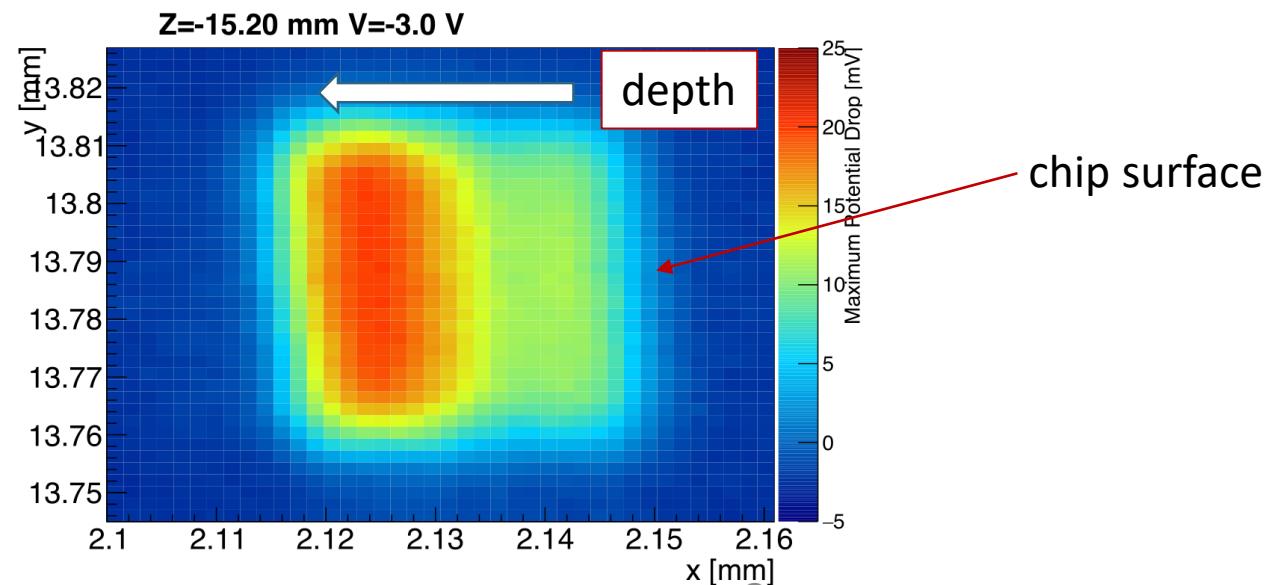
20 x 20 μm^2 pixel size, 3 neighbours



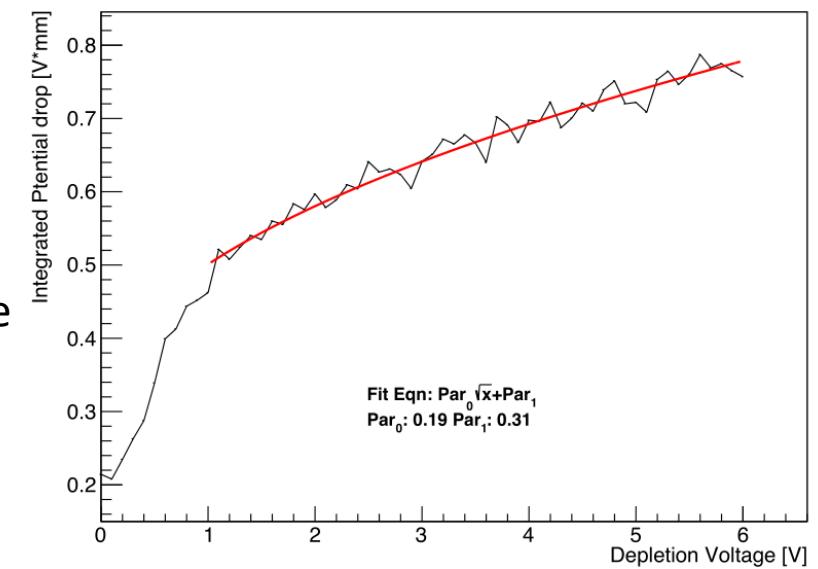
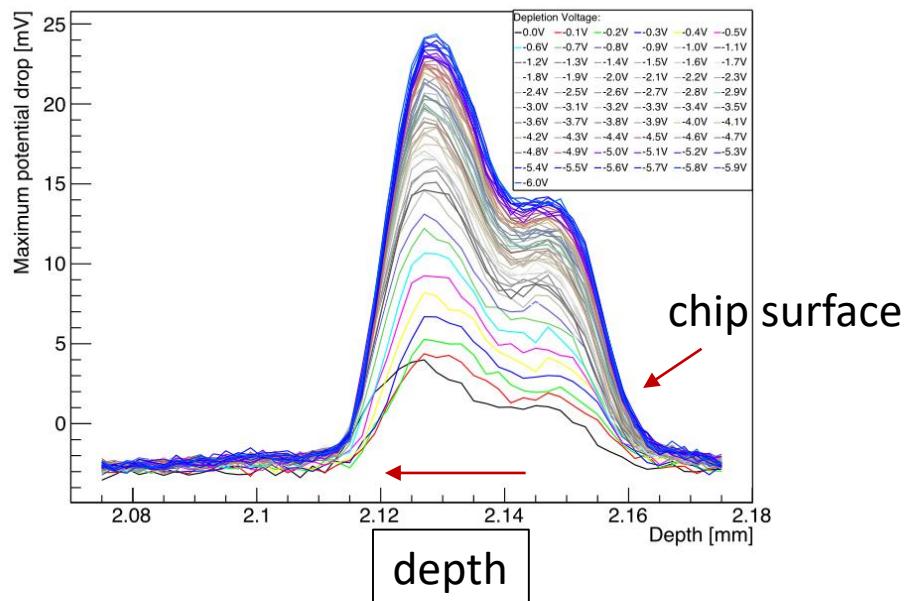
- 20 x 20 μm^2 pixels challenging to measure with E-TCT (small!)
- Measurements up to 2e15 show relatively good charge uniformity in the matrix

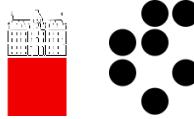


- unirradiated chip
- $50 \times 50 \mu\text{m}^2$ pixels
- double peak structure visible



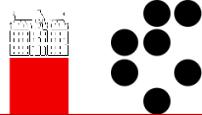
A. Sharma, C. Solans, CERN



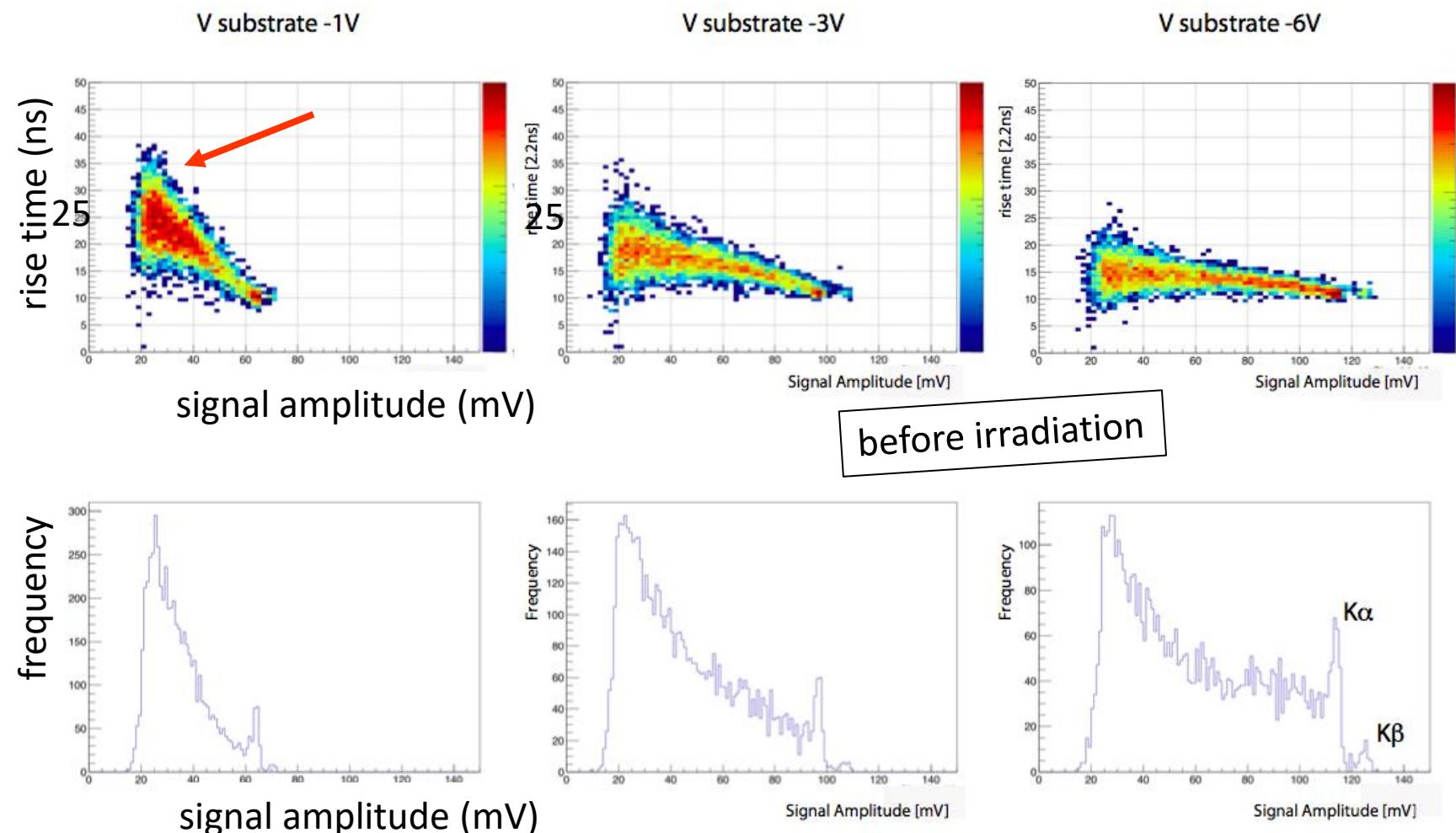


Source measurements

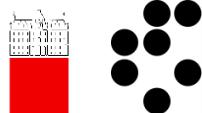
^{55}Fe standard process



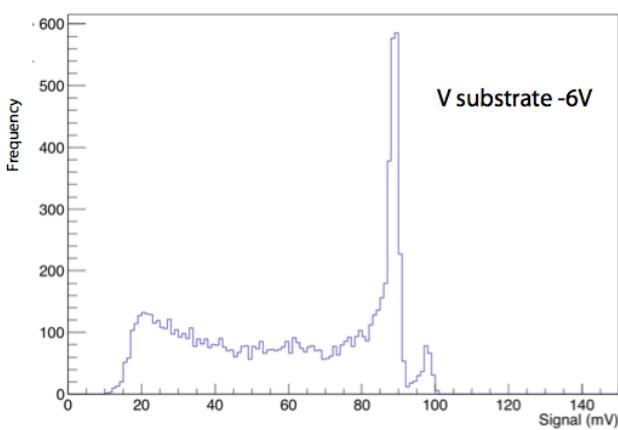
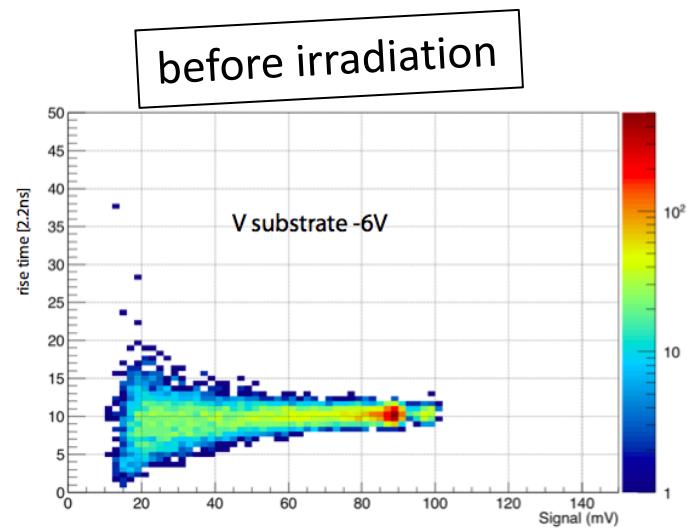
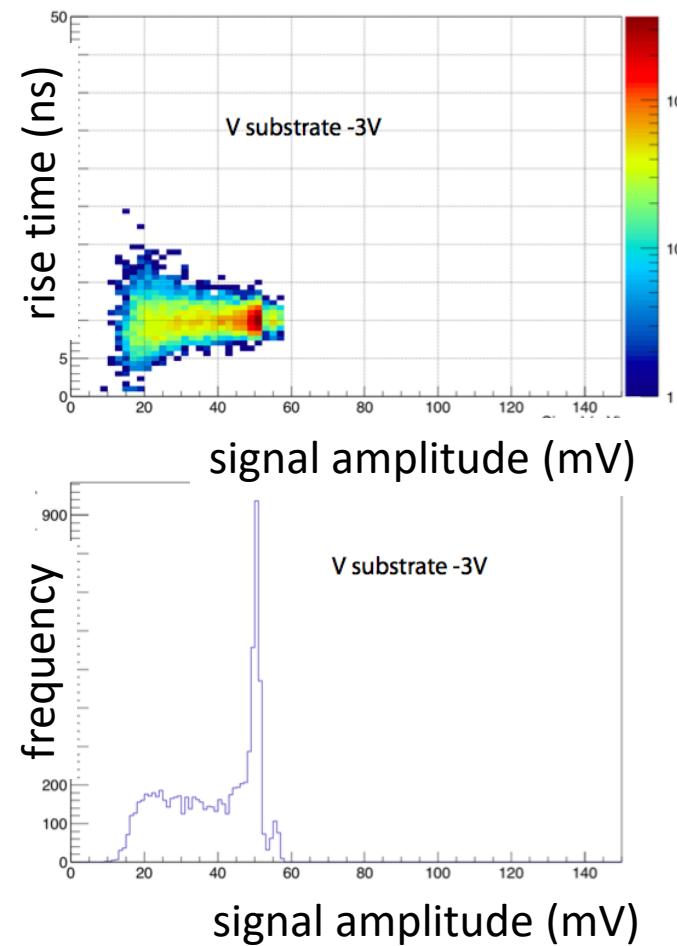
- Standard process chips, calibration with ^{55}Fe (K_α 5.9 keV)
- Rise time vs. amplitude: significant fraction of slow ("diffusion") signals
- Faster charge collection for shared hits at higher V_{bias}



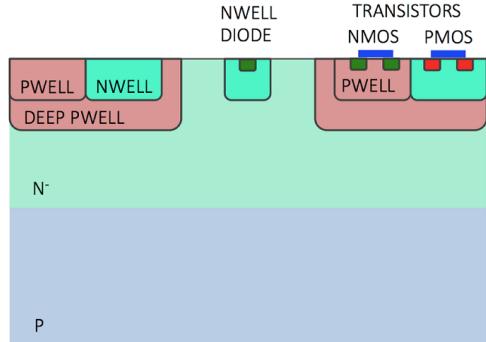
^{55}Fe modified process



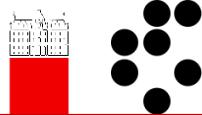
- Chips produced in modified process
- Lesser spread in charge collection time
- Better energy resolution



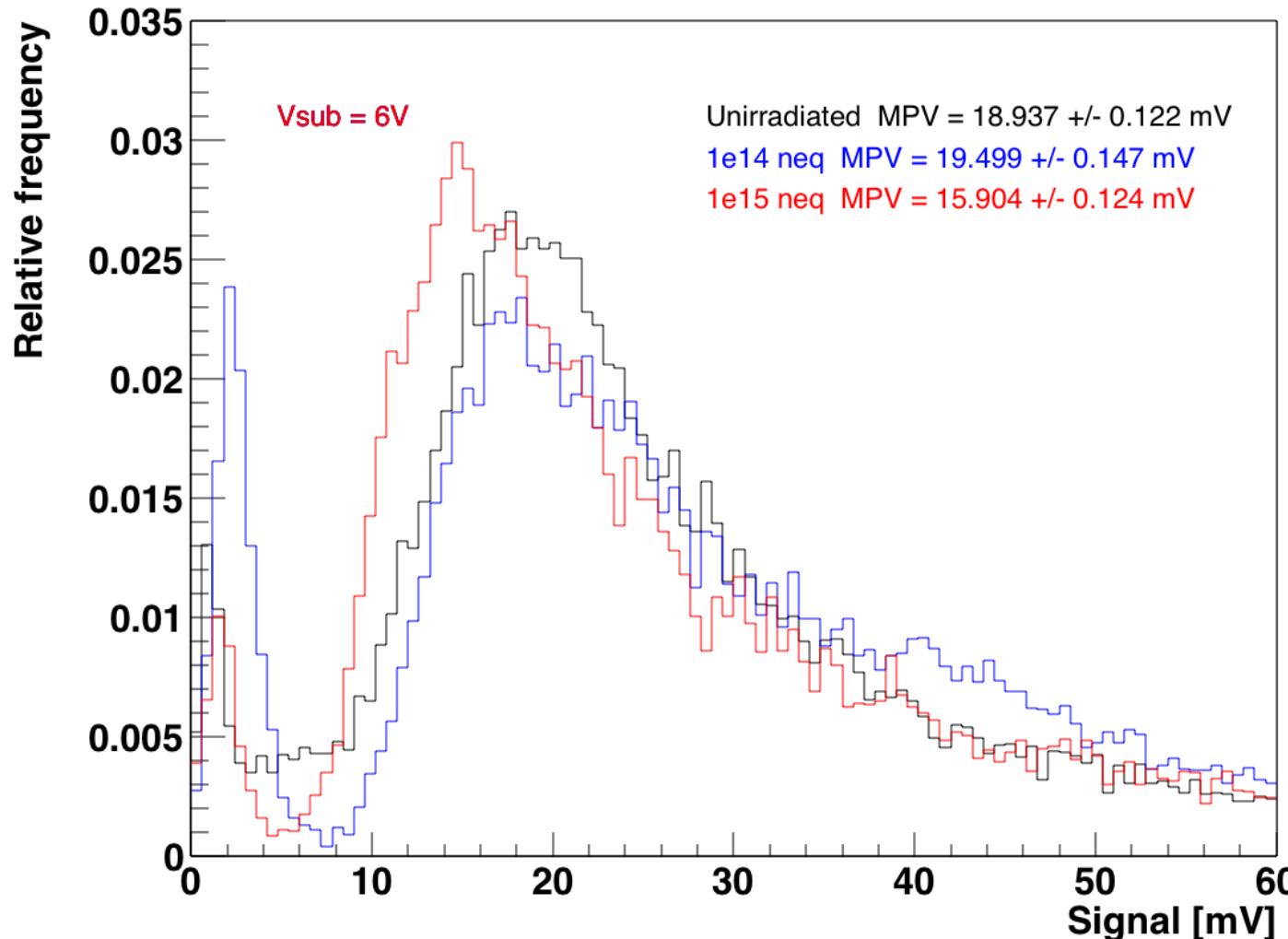
ALICE ITS / Jacobus van Hoorn IEEE NSSMIC2016



^{90}Sr spectra – modified process



Sr90 on 50x50um pixel for modified process after neutron irradiation



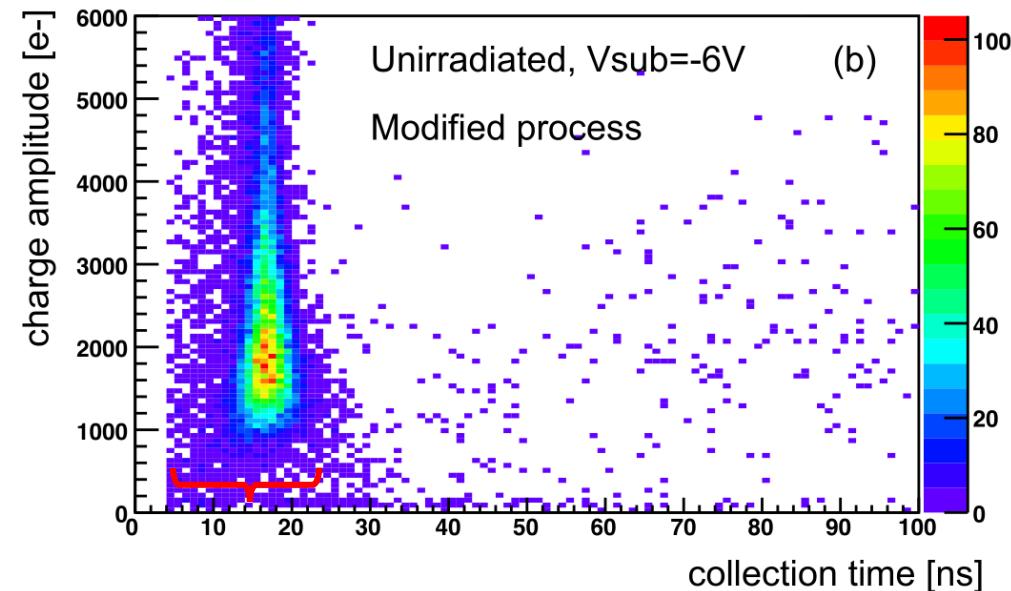
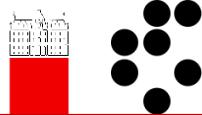
Neutron irradiation
 $1\text{e}14, 1\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$
(Ljubljana)

MPV around 2000 e⁻

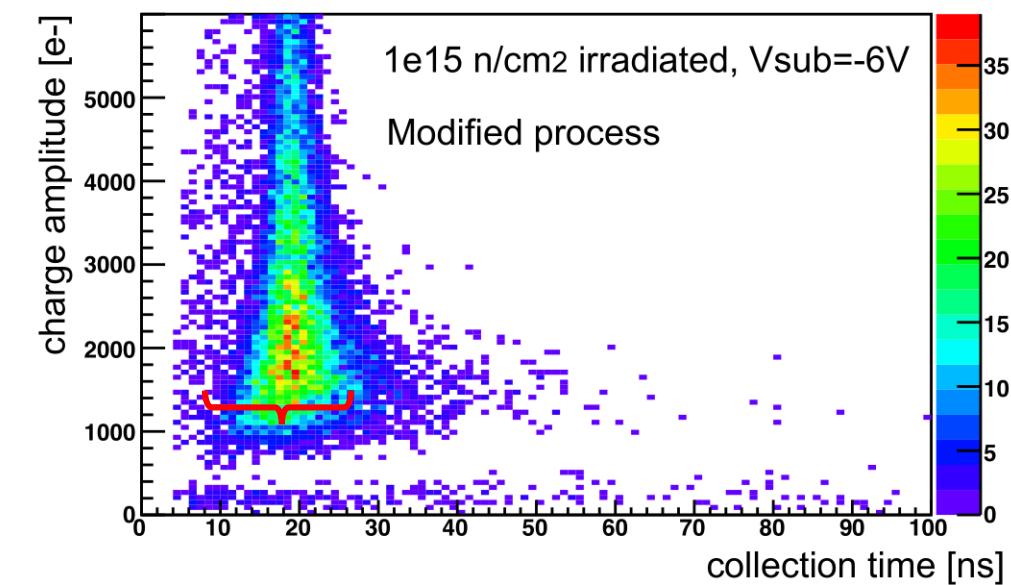
C. Riegel, CERN

Little change in signal spectrum after neutron irradiation up to $1\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$
Clear separation of signal and noise

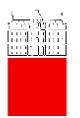
^{90}Sr - Collection time after irradiation



- Charge vs. collection time on $50 \times 50 \mu\text{m}^2$ pixels
- Little change in the signal shape after irradiation
- Charge collection times within 25 ns can be achieved
- Chips produced in standard process do not give a measurable signal after $1\text{e}15 \text{n/cm}^2$

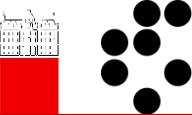


C. Riegel, CERN

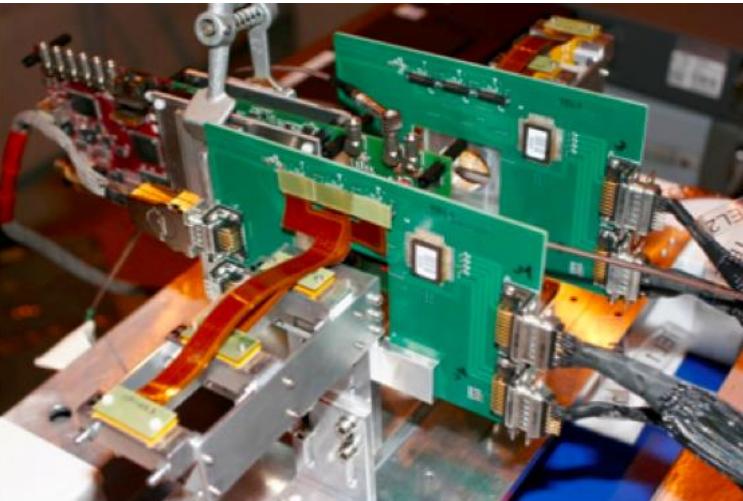


Test beam

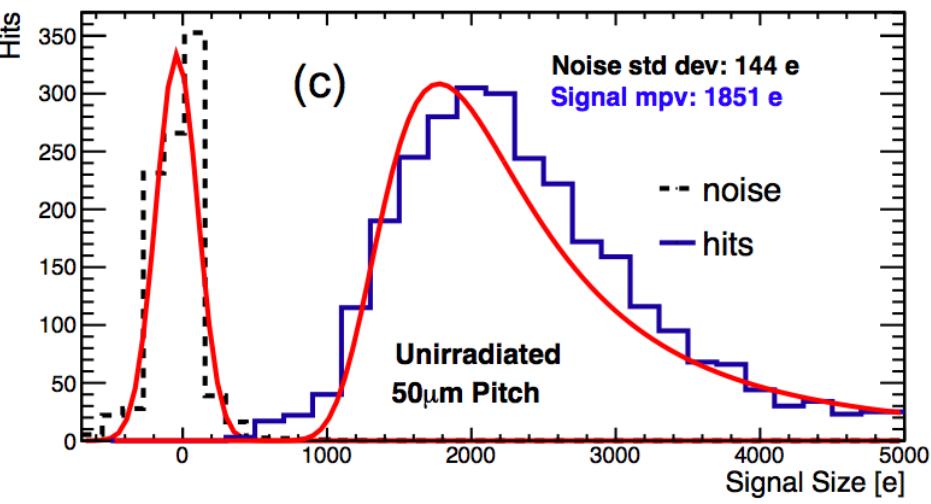
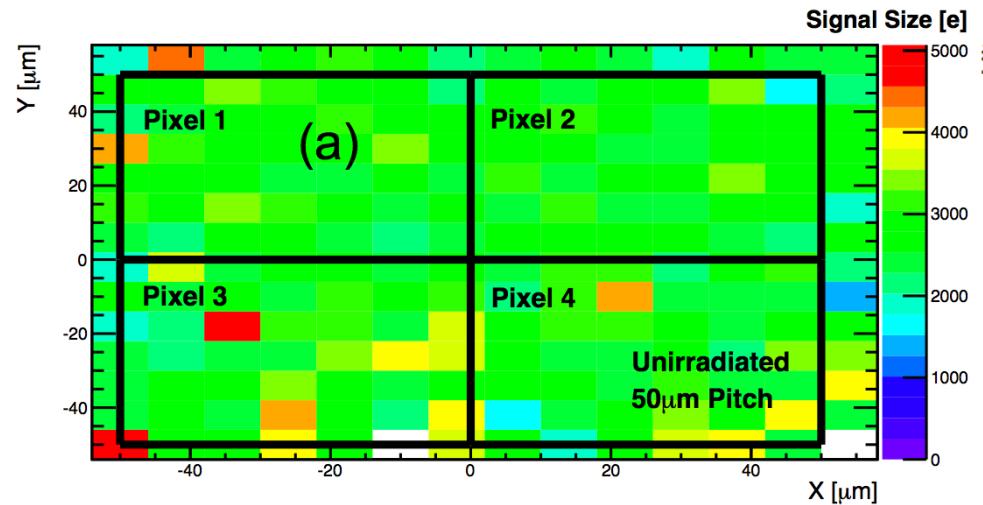
Test beam at SPS



- SPS 180 GeV pions
- Unirradiated $50 \times 50 \mu\text{m}^2$ pixel size
- $1\text{e}15 \text{n/cm}^2$ irradiated 25×25 and $30 \times 30 \mu\text{m}^2$

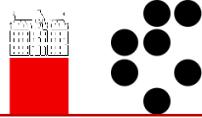


Signal size on four neighbour pixels (unirrad.)

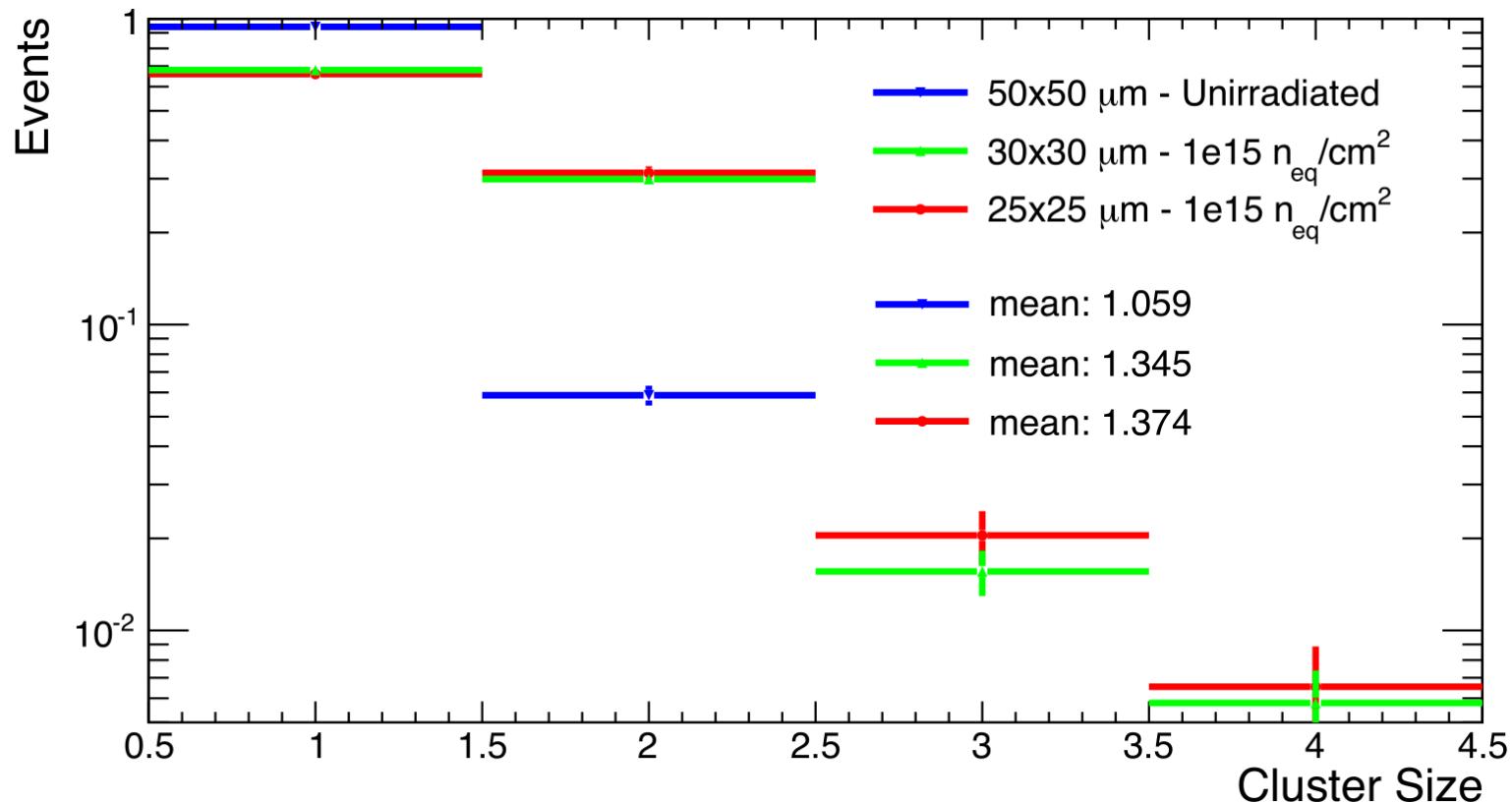
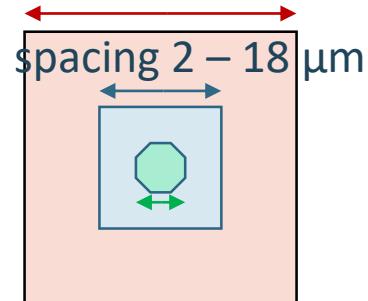


H. Pernegger, Trento 2017

Cluster size

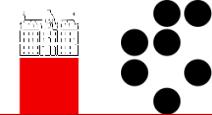


- Cluster size in dependence of pixel pitch
- Larger pixels → smaller cluster size
- Also influenced by spacing between DNW and DPW
 - **25x25** and **30x30** μm^2 pixels have 3 μm spacing
 - **50x50** μm^2 pixels have 18 μm spacing

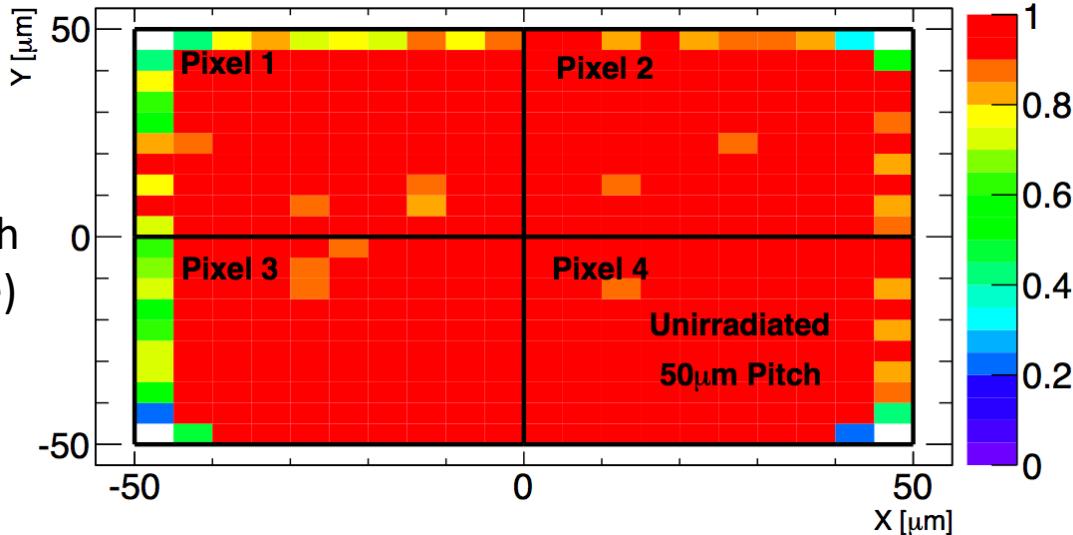


H. Pernegger, Trento 2017

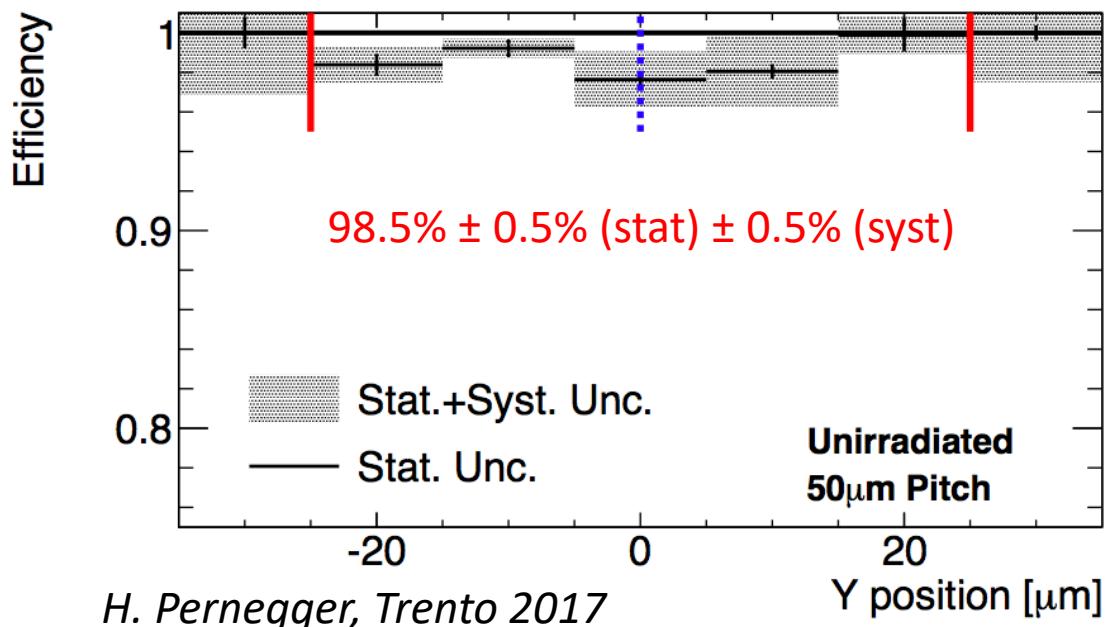
Unirradiated sample efficiency



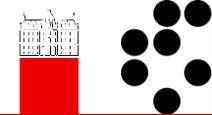
- Unirradiated sample
- Efficiency 98.5 % a bit low due to a high threshold 640 e⁻ (common mode noise)



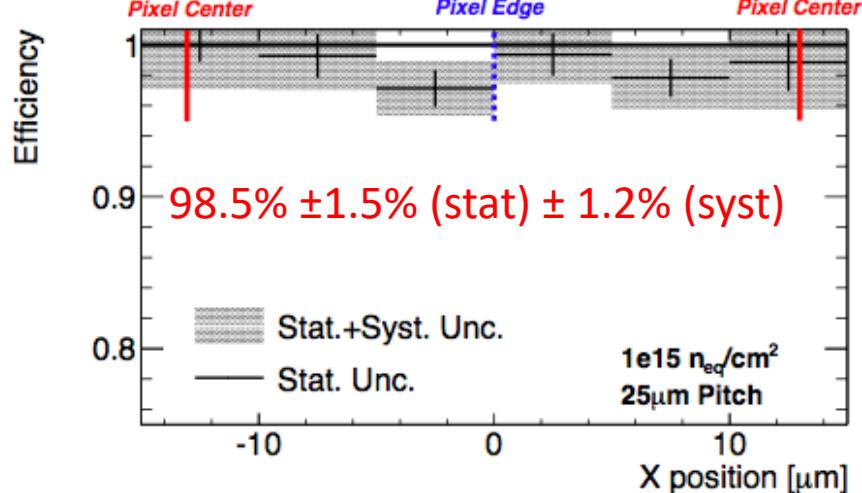
efficiency across pixel:



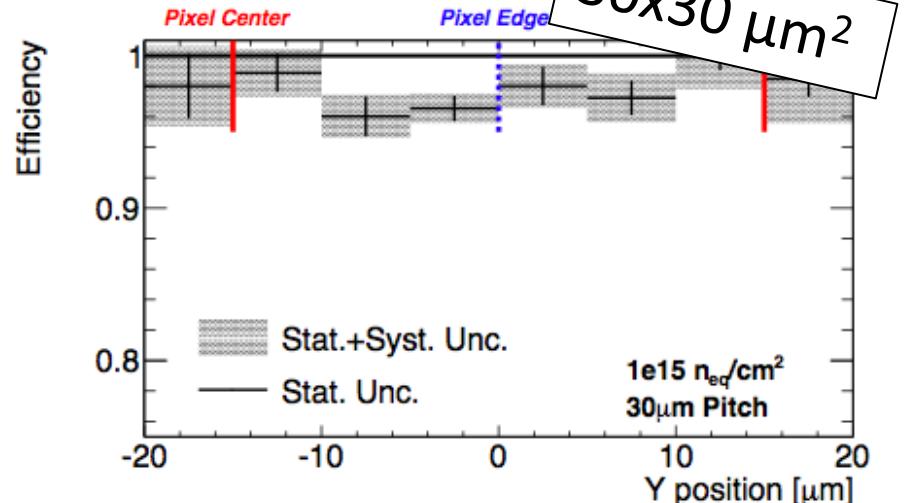
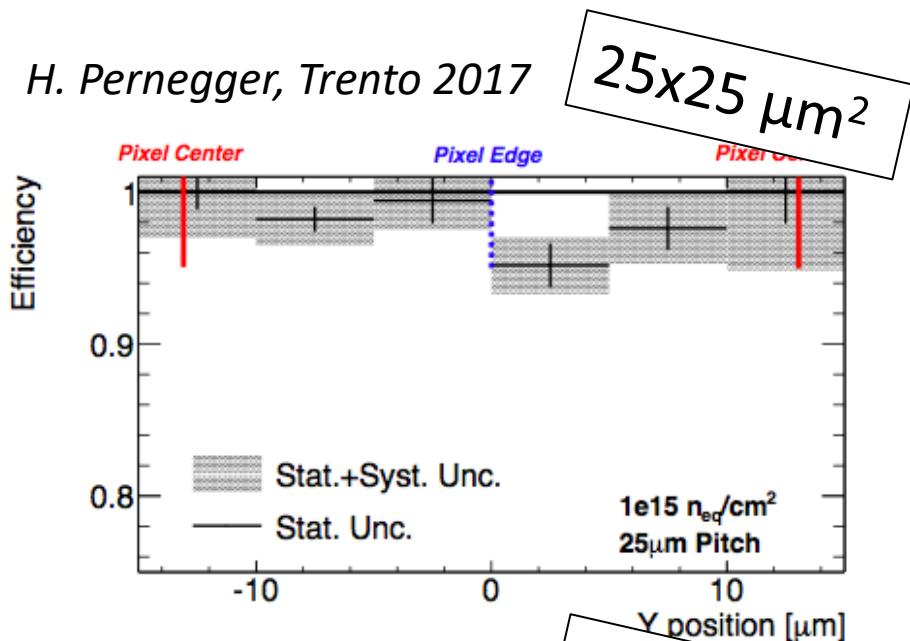
Irradiated sample efficiency

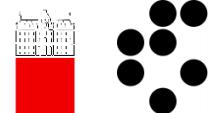


- 1e15 irradiated 25x25 and 30x30 μm^2
- Good uniformity across pixel



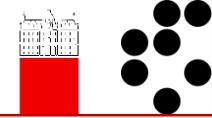
H. Pernegger, Trento 2017





- Low capacitance sensor technology promising for use in DMAPS
- Characterisation of irradiated chips with complementary methods
 - E-TCT:
 - Good charge collection efficiency and uniformity up to $5\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$
 - Response more uniform in chips with highly doped n-layer
 - Radioactive source scan:
 - Obtained good charge spectra also after irradiation to $1\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$
 - Collection time within 25 ns
 - Test beam:
 - Good efficiency > 97 % before and after irradiation to $1\text{e}15 \text{ n}_{\text{eq}}/\text{cm}^2$
- Sensors can be made radiation hard – sufficient for ATLAS outer pixel layers

Outlook



- New submission of an FEI4 sized demonstrator chip (2 designs):
 - TJ MALTA
 - Full matrix = 512x512 pixels
 - Design/CERN
 - Active area $18 \times 18 \text{ mm}^2$
 - Hit memory in active matrix
 - All hits are asynchronously transmitted over high-speed bus to EoC logic
 - No clock distribution over active matrix to minimize power and digital-analog cross-talk
 - TJ MonoPix
 - 512x256 pixels ($36.4 \times 36.4 \mu\text{m}^2$ pixel size)
 - Design/Bonn
 - Active area $18 \times 10 \text{ mm}^2$
 - Hit memory in active matrix (2 flip-flop per pixel)
 - Synchronous column drain architecture
 - Hit address asserted to bus with 40 MHz token
 - 6 bit ToT coding at end of column

Design Team: W. Snoeys, T. Kugathasan, C. Marin Tobon, I. Berdalovic, R. Cardella, N. Egidos (CERN) J. Rousset, B. Blochet (MIND), K. Moustakas, T. Wang (Bonn)

- Characterisation of proton irradiated samples
- TID measurements
- Design of a quad module for implementation in ATLAS