Depleted CMOS chip design and test beam of the H35Demo chip

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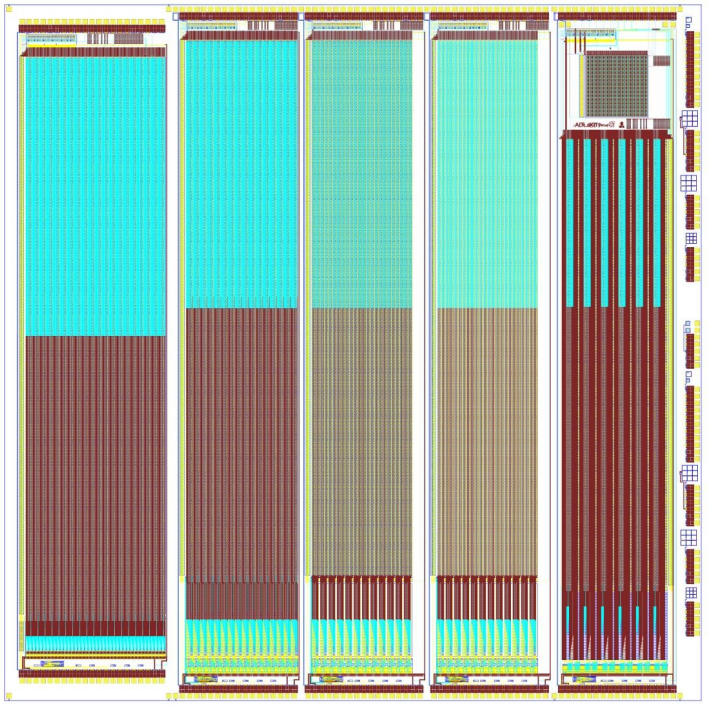
Outline

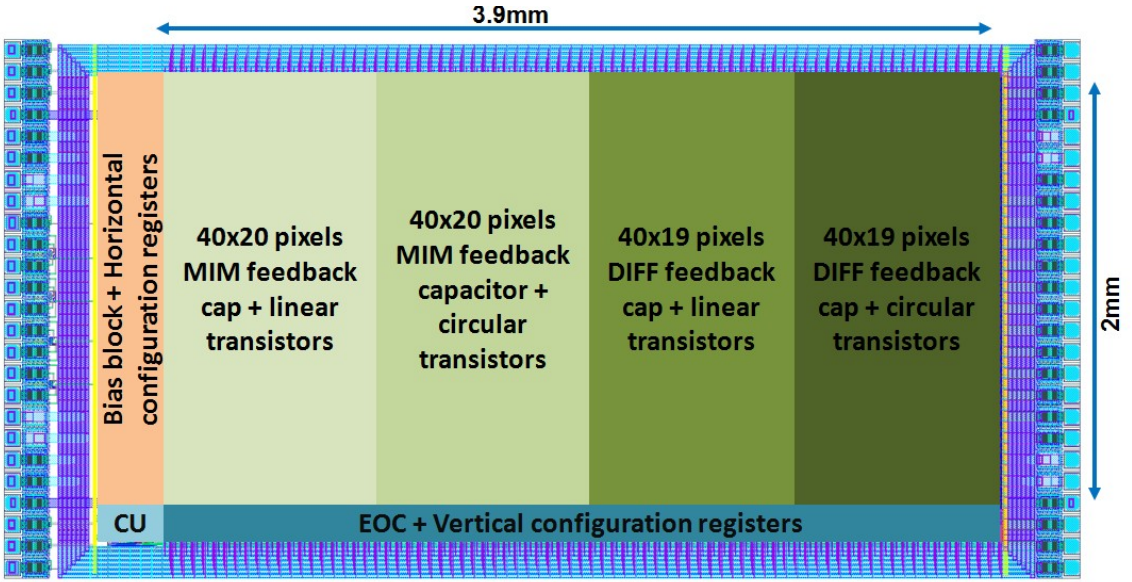
- Chip design
  - LF ATLAS Pix
  - LF2
  - RD50 Chip
  - H35Demo
- H35Demo Chip test beam
  - Monolithic matrix readout
  - Test beam measurements
  - Results
  - Conclusions

LF ATLAS Pix



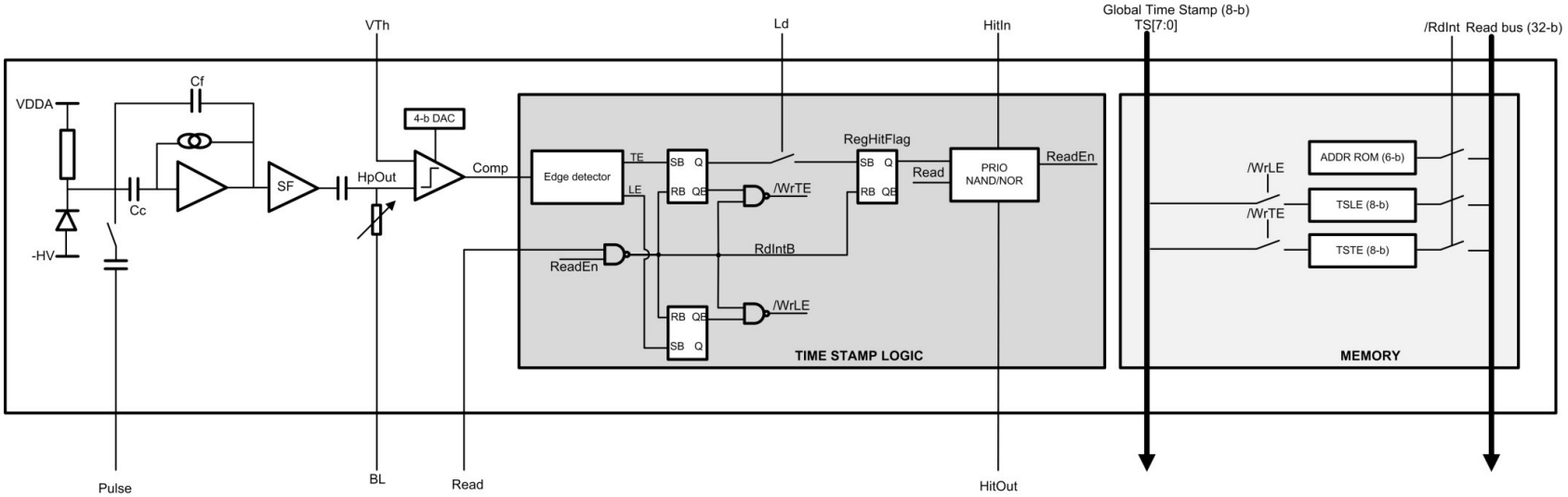
- Technology: LFoundry 150nm HV-CMOS
- Resistivities: 100 Ωcm, 500 Ωcm,
  1.1 kΩcm, 1.9 kΩcm and 3.8 kΩcm
- Designed by KIT, IFAE and University of Liverpool
- IFAE main contribution on the digital block
- Status: Received in February 2017
  - Tests ongoing in KIT

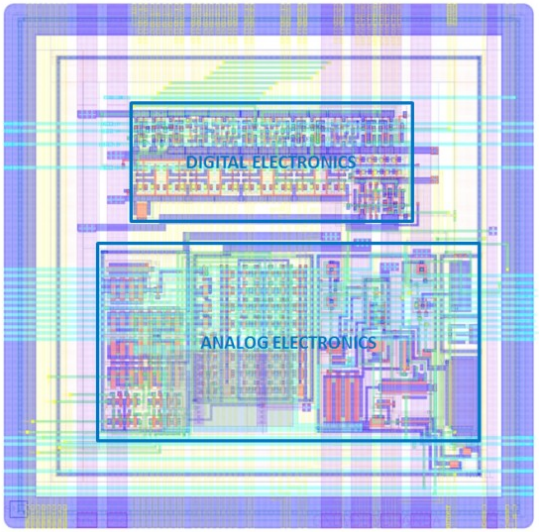
LF2



- FEI3 like pixel matrix in 50x50 μm^2 pixel
- Technology: LFoundry 150nm HV-CMOS
- Resistivities: 500 Ωcm and 1.9 kΩcm
- Designed by IFAE in collaboration with University of Liverpool
- Contributions from University of Geneve and KIT
- Status: Received in May 2017
  - First tests ongoing

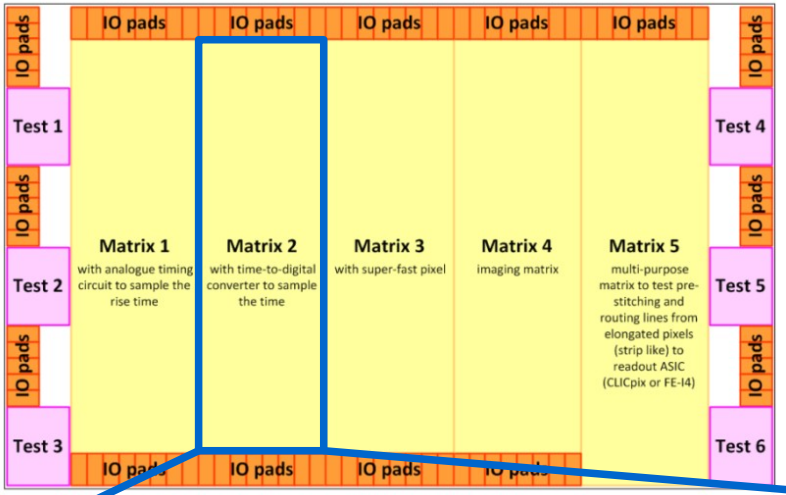
LF2 Readout *a la FEI3*



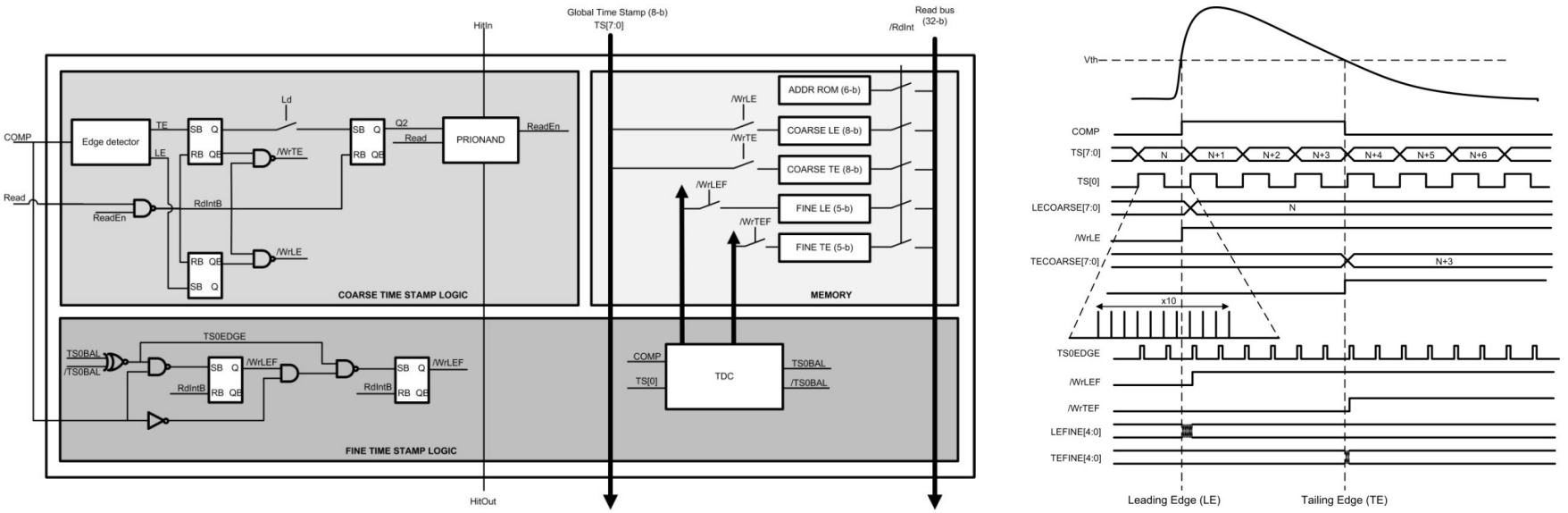


- Column-drain architecture
- Global 8-bit gray encoded time stamp (40MHz)
- For each hit:
  - Leading Edge (LE): 8-bit DRAM memory
  - Trailing Edge (TE): 8-bit DRAM memory
  - Address: 6-bit ROM memory
- TOT = LE – TE (off-chip)

RD50 Chip



- LFoundry 150nm HV-CMOS
- Designed by: U. Liverpool, U. Barcelona, IFAE, FBK (...)
- IFAE main contribution on the matrix with on-pixel TDC (Time-to-Digital Converter):
  - Global Time Stamp: coarse time measurement
  - TDC: fine time measurement
- Status: Design phase

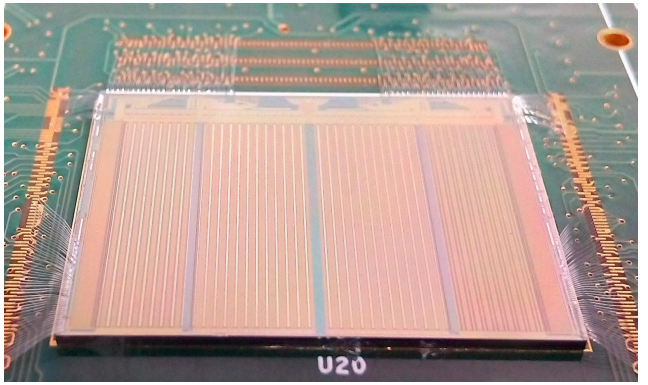


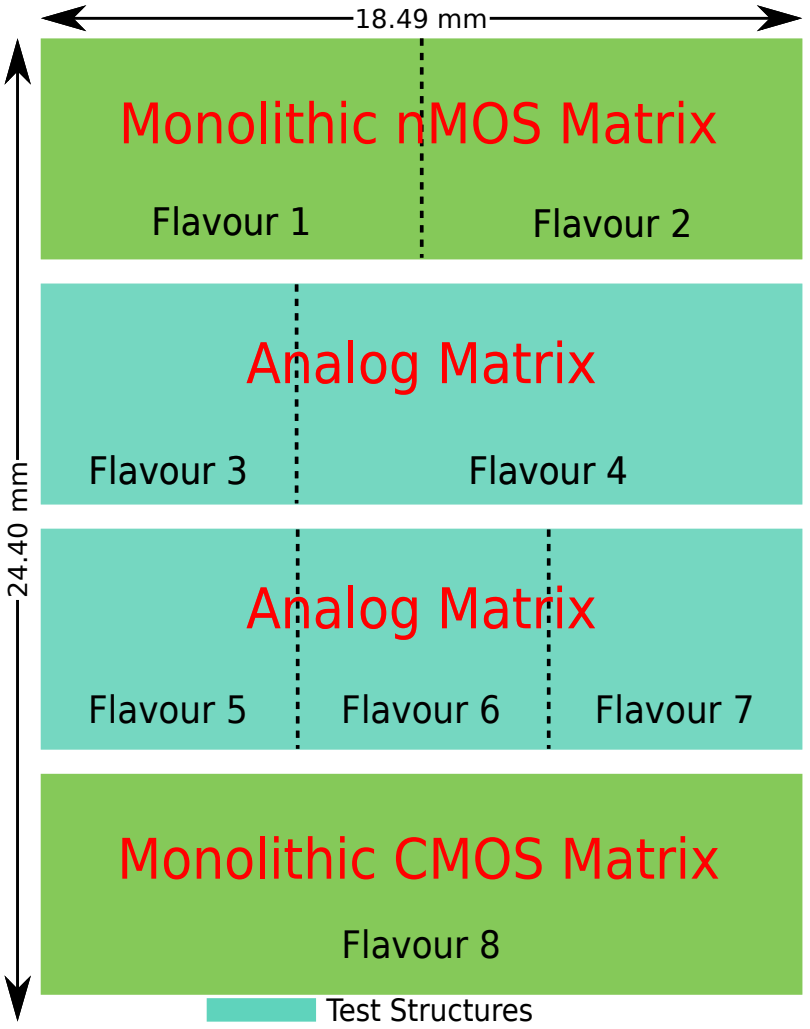
More details about the RD50 Chip in E. Vilella talk

H35Demo Chip

A large area demonstrator chip in the AMS 0.35µm HV-CMOS technology produced on wafers of different resistivity:
20 Ωcm (standard), 80 Ωcm, 200 Ωcm, 1 kΩcm

Designed by KIT, IFAE and University of Liverpool



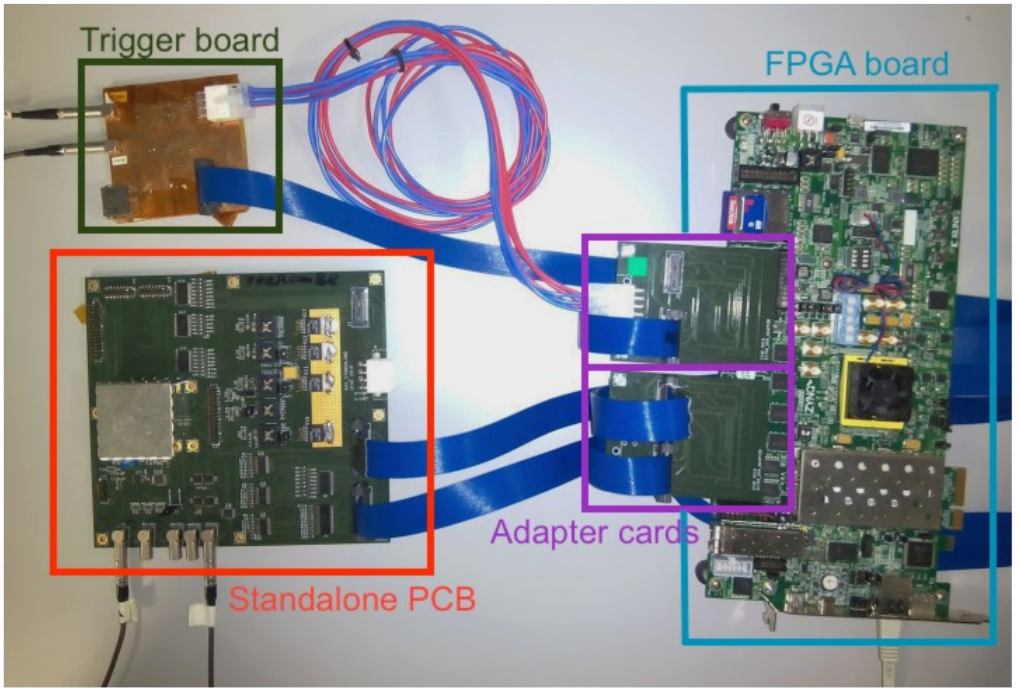


Eight different pixel matrix flavors:

- Monolithic **nMOS** matrix
  - Digital pixels with in pixel nMOS comparator
  - Two flavors: w/ Time Walk compensation and w/o Time Walk compensation
- **Analog** matrix (2 arrays)
  - Different flavors in terms of gain and speed
  - To be capacitative coupled to FE-I4 readout chips
- Monolithic **CMOS** matrix
  - Analog pixels with off pixel CMOS comparator
    In the readout cells:
    - 1 discriminator for the left half
    - 2 discriminators for the right half

Monolithic matrix readout

Readout of the monolithic matrices developed at IFAE: hardware, firmware and software



FPGA board:

- Xilinx ZC706

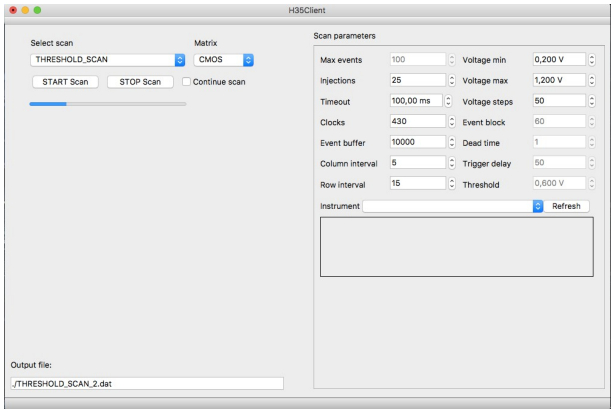
H35Demo PCB:

- Low voltage regulators
- Sensor bias
- Test pulse input
- Analog signal output
- Able to program all matrices and read both CMOS and nMOS

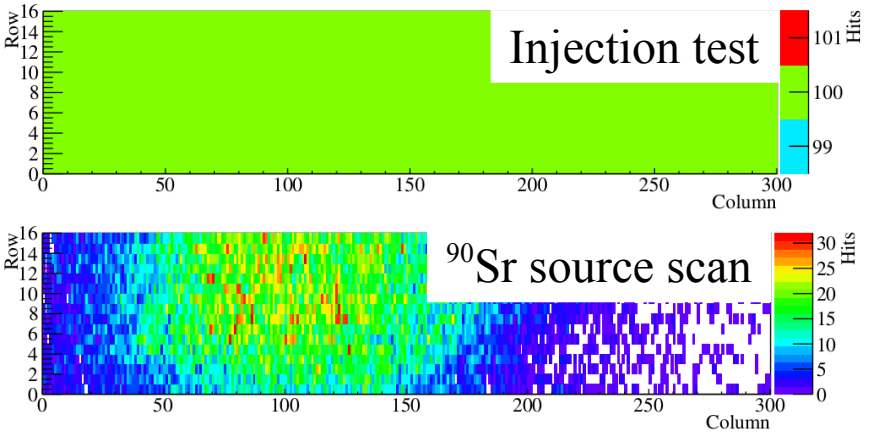
Trigger board:

- Trigger in
- Busy out

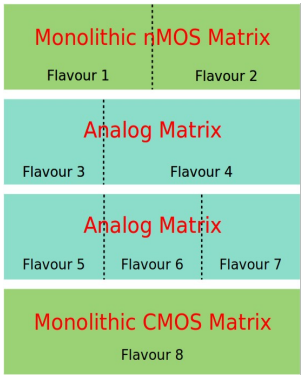
Steering software



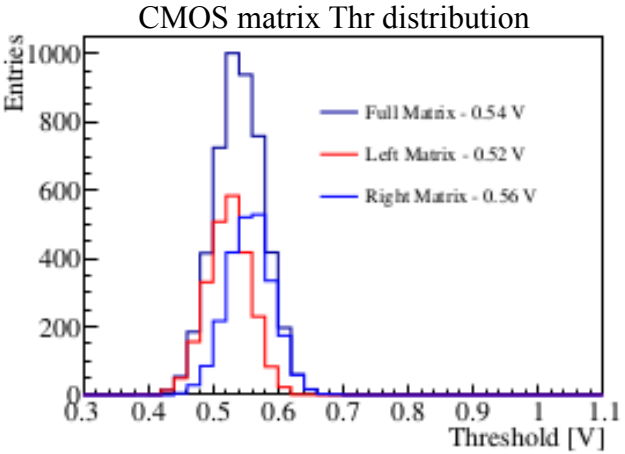
Preparatory lab test



Threshold tuning



There is a large threshold dispersion if the chip is not tuned, the left and right parts of the matrix have two different distributions

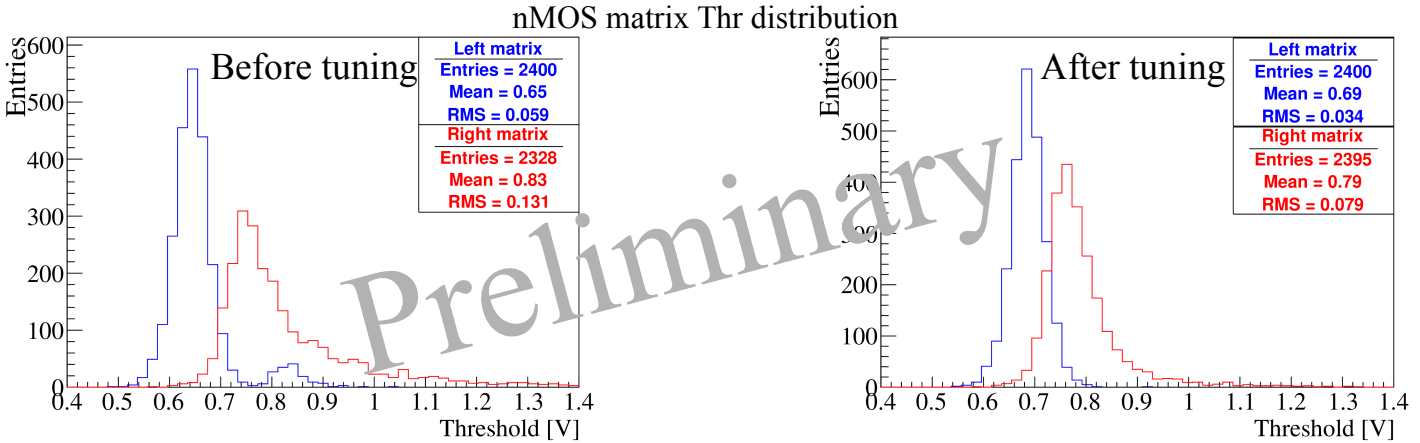


On the CMOS matrix a 4-bit DAC per each pixel is available in the periphery (TDAC)

- The left part of the matrix stops responding after the TDAC is changed
- When assigning different values to each pixel the outcome is not the expected one

On the nMOS matrix an in-pixel 2-bit DAC is available

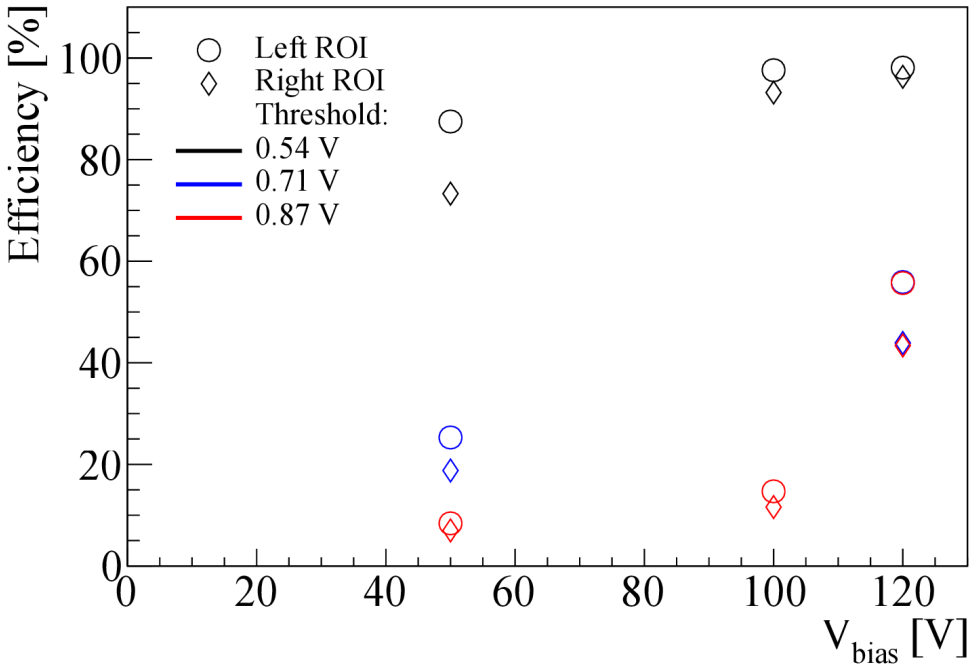
- It allows to recover the pixels out of the central distribution for the left matrix
- Time-Walk discriminator need to be adjusted to recover the right matrix



Test beam in collaboration with UniGe

First Test Beam (TB) w/ UniGe FEI4 telescope in November 2016 @ CERN SPS

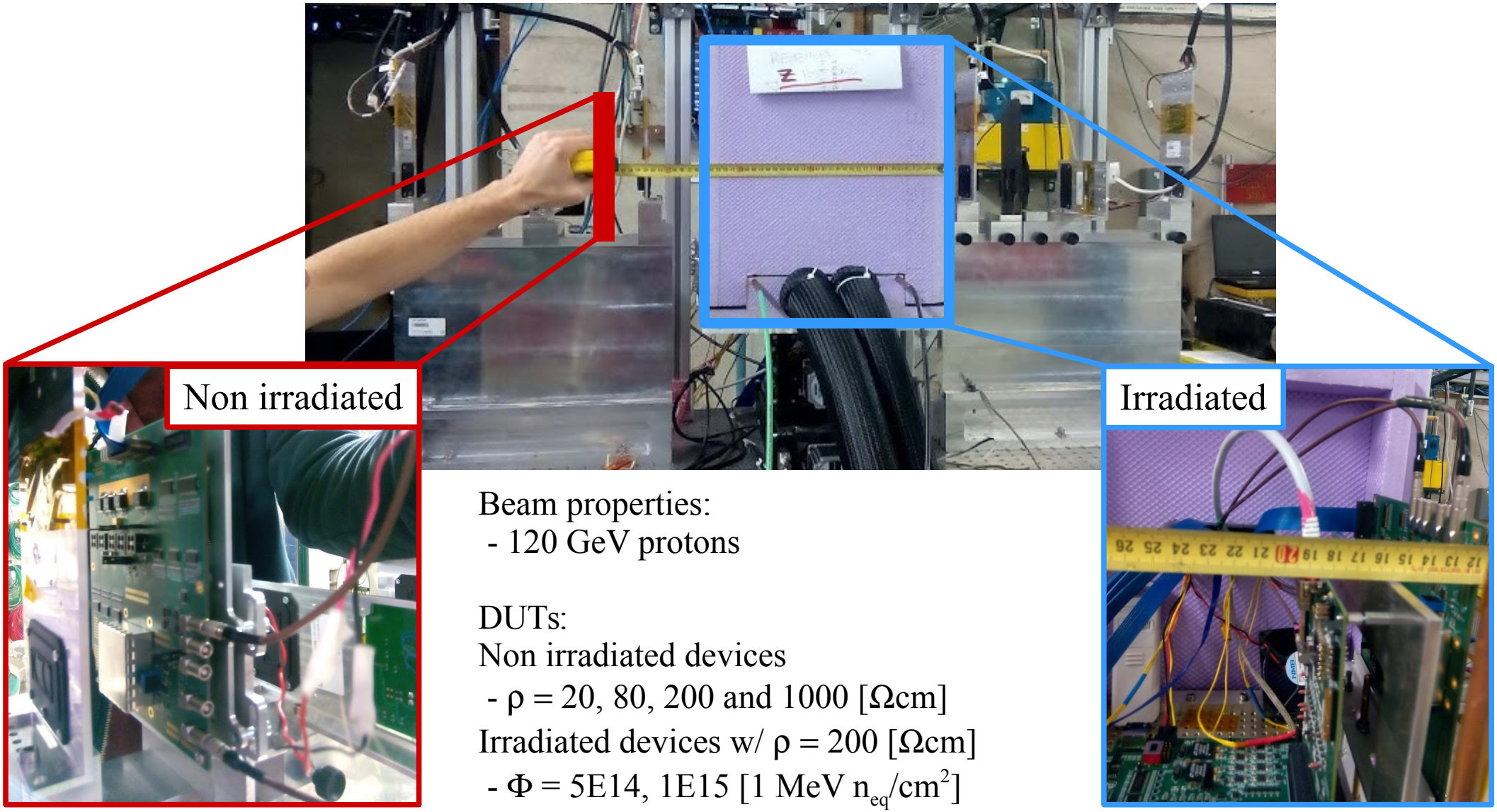
- CMOS matrix of a non irradiated 200 Ωcm chip tested
- Maximum efficiency of 98% (97%) on the left (right) half of the CMOS matrix
- Threshold value too large to have larger efficiency at lower voltage
- Left/Right asymmetry can be explained by the different threshold distribution
- Results presented at Instrumentation for Colliding Beam Physics (INSTR17) by S. Terzo
  → arxiv.org/abs/1705.05146



Thanks to the UniGe ATLAS group:
M. Benoit, F. Di Bello, M. Kiehn, B. Ristic and M.V. Barrero Pinto

Test beam in collaboration with UniGe

Second TB w/ UniGe FEI4 telescope in April 2015 @ Fermilab, first time with irradiated chips



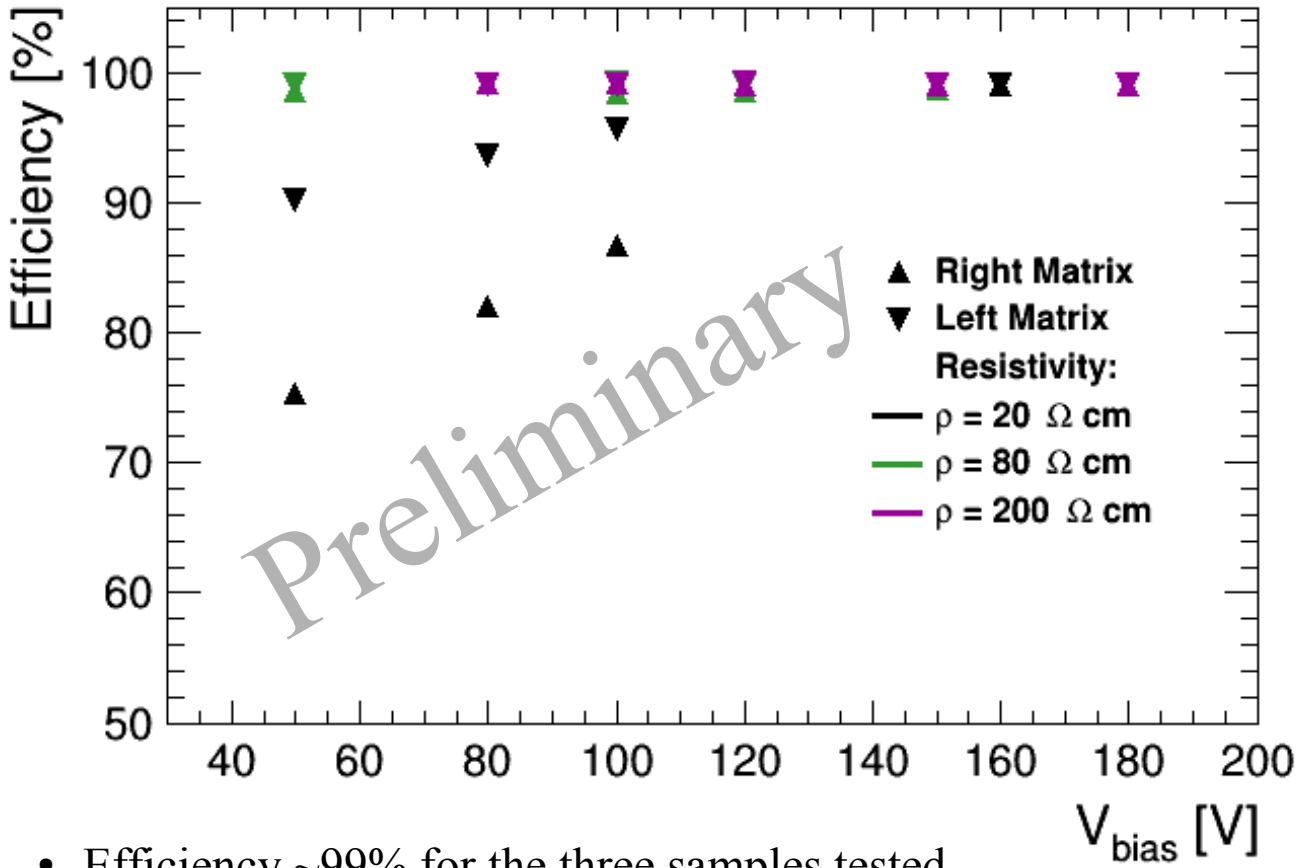
Beam properties:
- 120 GeV protons

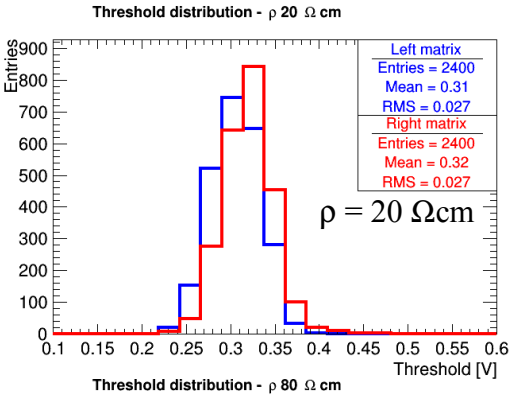
DUTs:
Non irradiated devices
- ρ = 20, 80, 200 and 1000 [Ωcm]

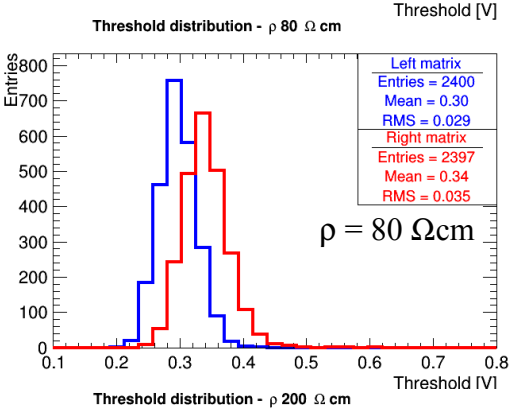
Irradiated devices w/ ρ = 200 [Ωcm]
- Φ = 5E14, 1E15 [1 MeV n_{eq}/cm^2]

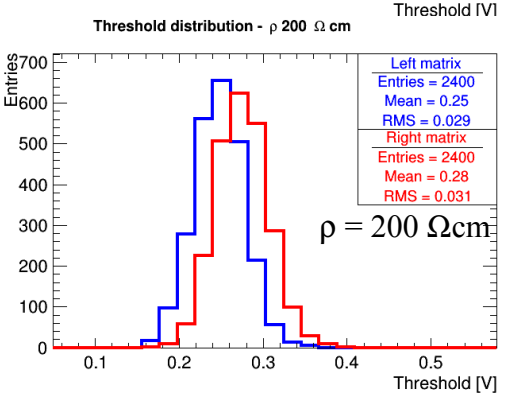
Irradiated w/ neutron at JSI

Non irradiated DUTs



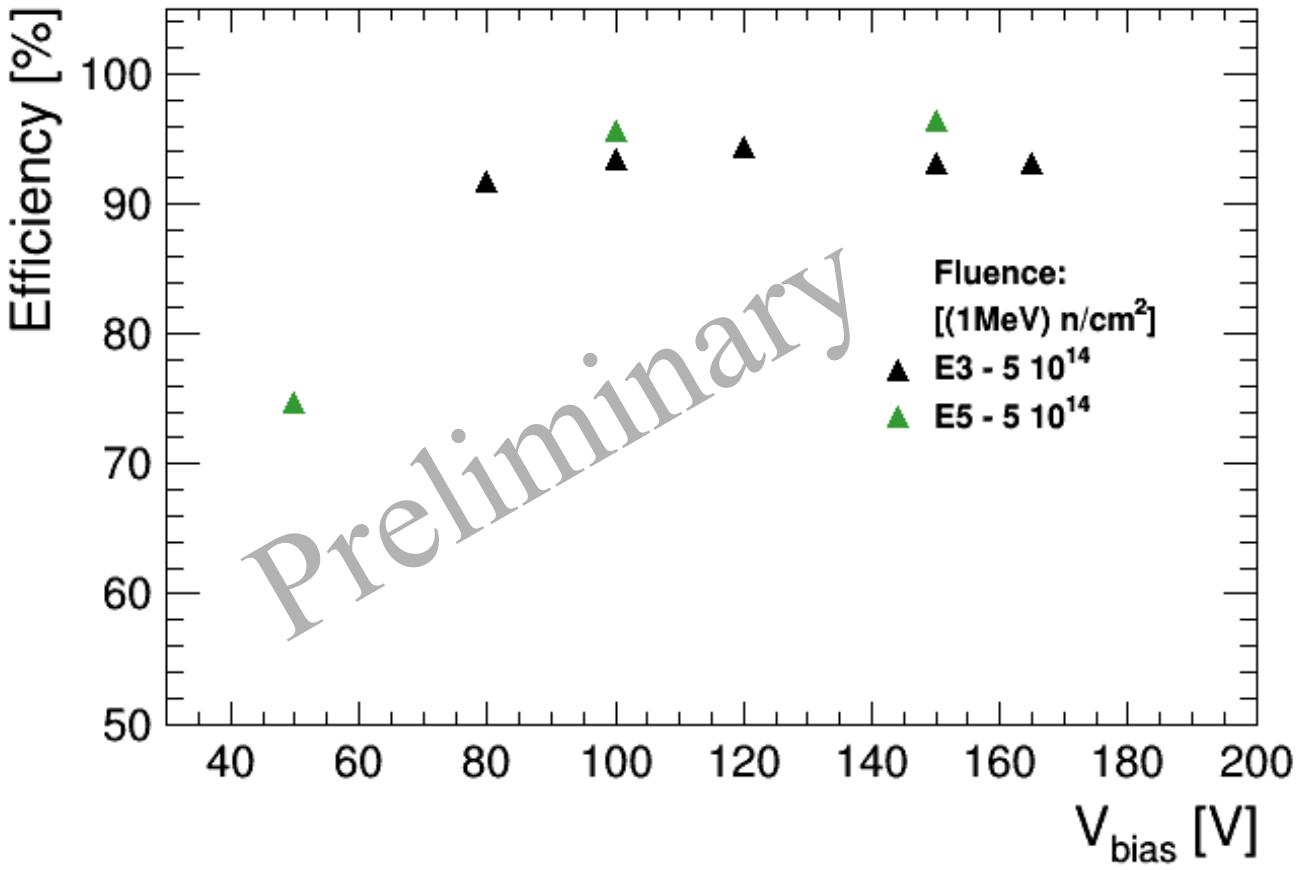


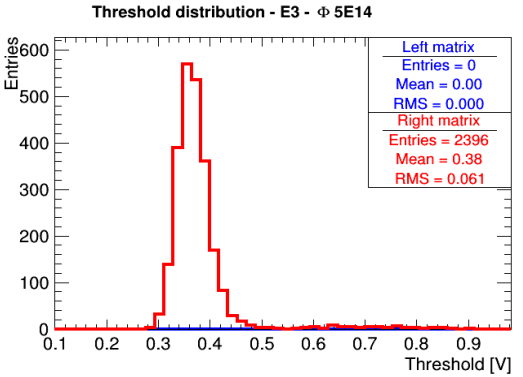


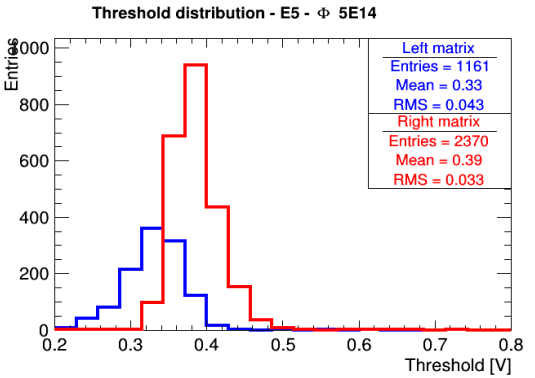


- Efficiency ~99% for the three samples tested
- Left/Right asymmetry significant only for the 20 Ωcm sample does not seem related to the different threshold
- 1 kΩcm sample trips with the spill
  low V_{bd}, probably from a bad wafer
- The 200 Ωcm sample has larger efficiency than in previous TB where it was tested with a larger threshold

Irradiated DUTs







- The telescope and H35Demo data streams run out of synchronization
  - Current analysis on lower statistics
  - Issue more serious on sample w/ higher irradiation dose (analysis ongoing)
- The two samples irradiated at 5E14 n/cm2 have reach an efficiency larger than 90% @ V > 80 V

Thanks to the JSI people for the irradiation effort:
G Kramberger, I Mandic, V Cindro

Conclusions

- IFAE is involved both in designing and testing HV-CMOS chips for high energy physics experiments
- The first TB of a monolithic matrix of the H35Demo chip after irradiation has been performed
- Non irradiated H35Demo chip of different resistivities tested
  → Efficiency ~ 99%
  → Compatible w/ previous results from the CERN SPS TB
- Synchronization issue for the irradiated samples
  → Efficiency > 90% on the 5E14 samples
  → Preliminary analysis, not full statistics
- Proton irradiated H35Demo chips just received from KIT

Thanks

Backup

Motivation

Depleted CMOS for the ATLAS upgrade

LHC upgrade to High Luminosity LHC scheduled for beginning 2024
Plan to increase the luminosity by an order of magnitude up to 10^{35} $cm^{-2}s^{-1}$

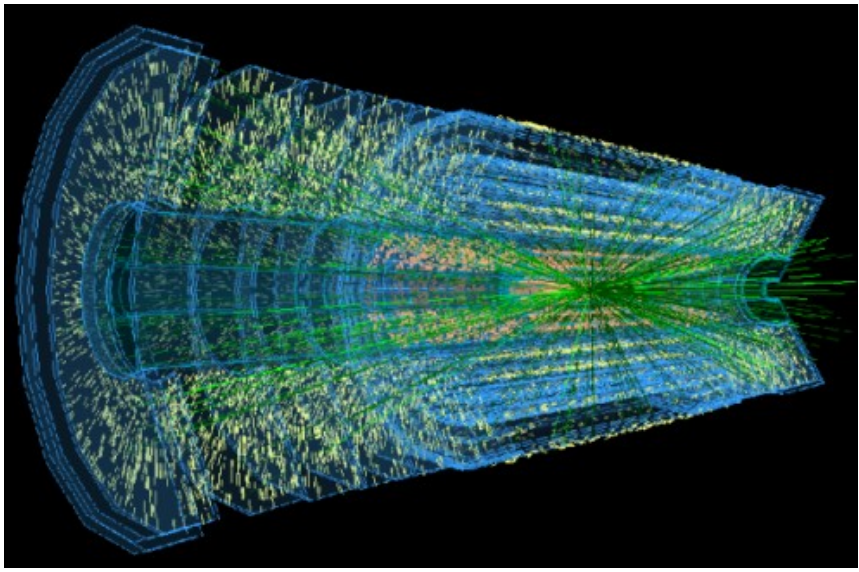
Detector challenges:
particle multiplicity - pileup rejection
radiation hardness

ATLAS ITk - tracker upgrade for HL-LHC

- 5 layers Pixel detector
- 4 layers Strip detector

A total area of **~10 m^2 of pixel detectors** will be installed

The **innermost pixel layer** will be required
to stand up to a fluence of **$2 \cdot 10^{16}$ n_{eq}/cm^2**
the **outermost layer ~ 10^{15} n_{eq}/cm^2**



Sketch of an event in ATLAS at HL-LHC

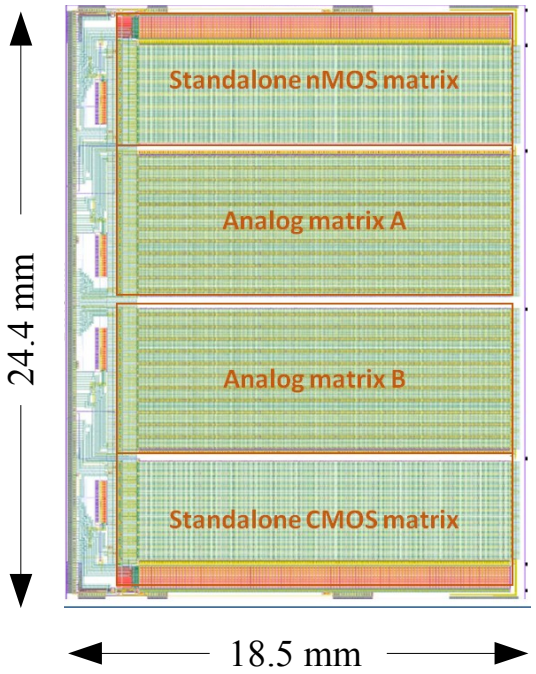
Depleted CMOS technologies being investigated in ATLAS as an option for the HL-LHC upgrade

ATLAS groups are investigating the performances of:

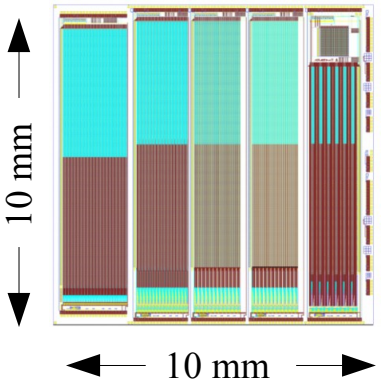
- Devices from different foundries
- Different approaches:
  CC coupled – monolithic

Chip Design

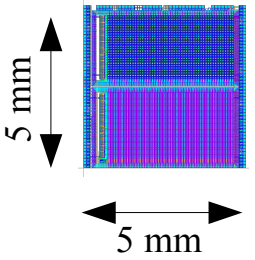
H35Demo



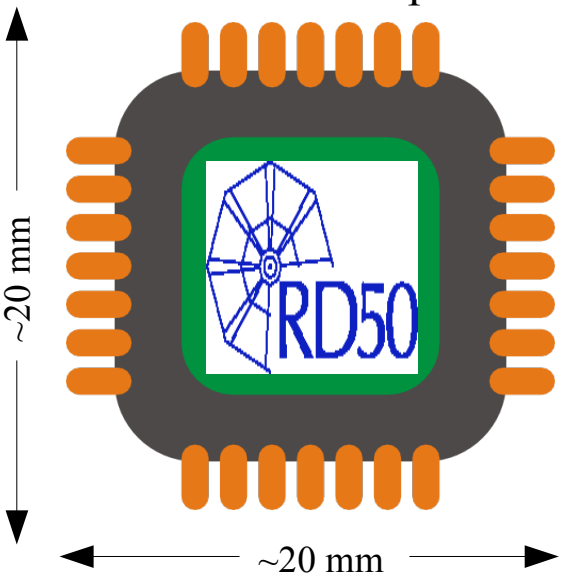
LF ATLAS Pix



LF2



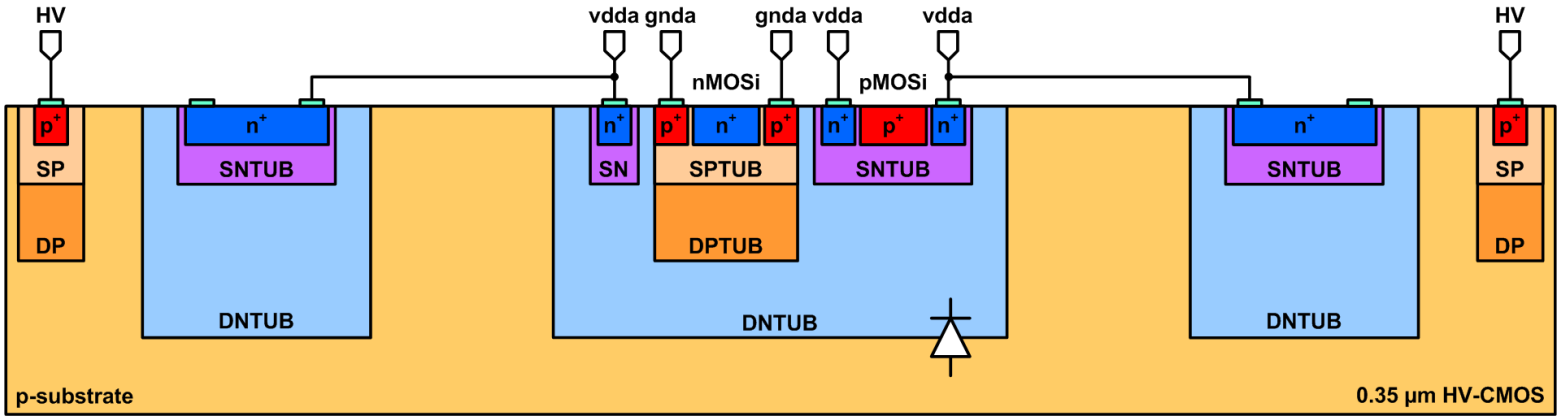
RD50 Chip

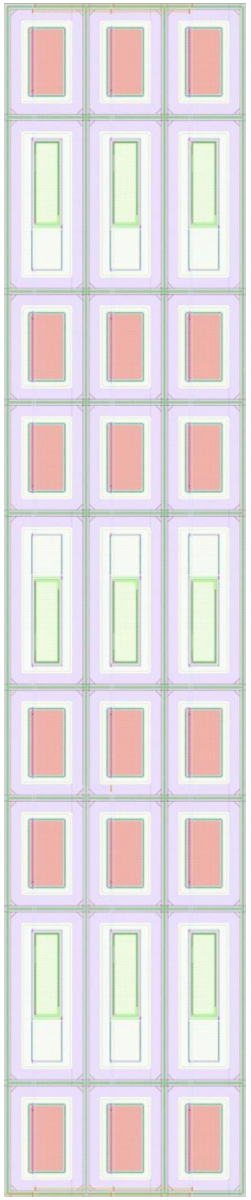


H35Demo test structure

The tested structure is a matrix of 3x3 pixels of 50·250 μm^2 each

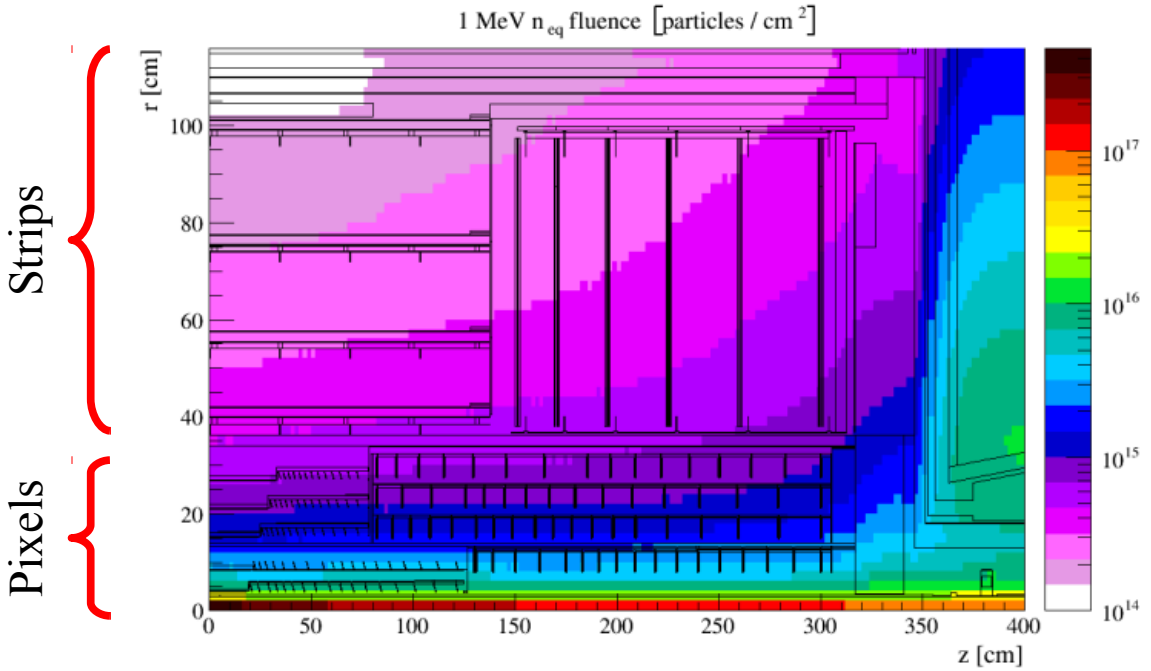
- 3 deep N wells in each pixel
  - central 50·110 μm^2
  - external 50·70 μm^2
- no electronics inside the pixels
- deep P well inside the deep N well of the central N well
- deep N wells covered by a layer of polysilicon in the external N wells
- central pixel (marked in red in the figure) is read out individually
- signals of the 8 external pixels are shorted together



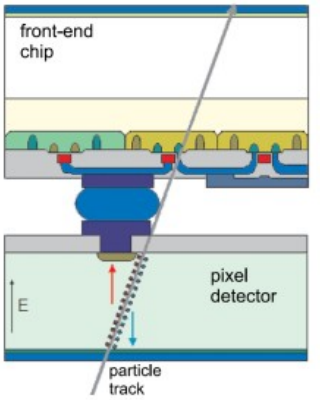


Backup

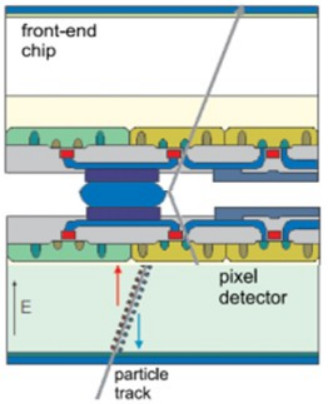
Requirements for inner and outer layers of the ATLAS ITK differ by orders of magnitude in terms of radiation tolerance, occupancy, ...



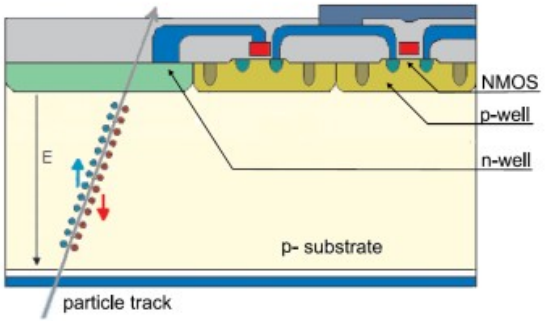
Different options:



Hybrid



Capacitive coupled (CCPD)



Monolithic

Possible solution:

Hybrid solution for the **inner layers**

CMOS monolithic or CCPD for the **outer layers**

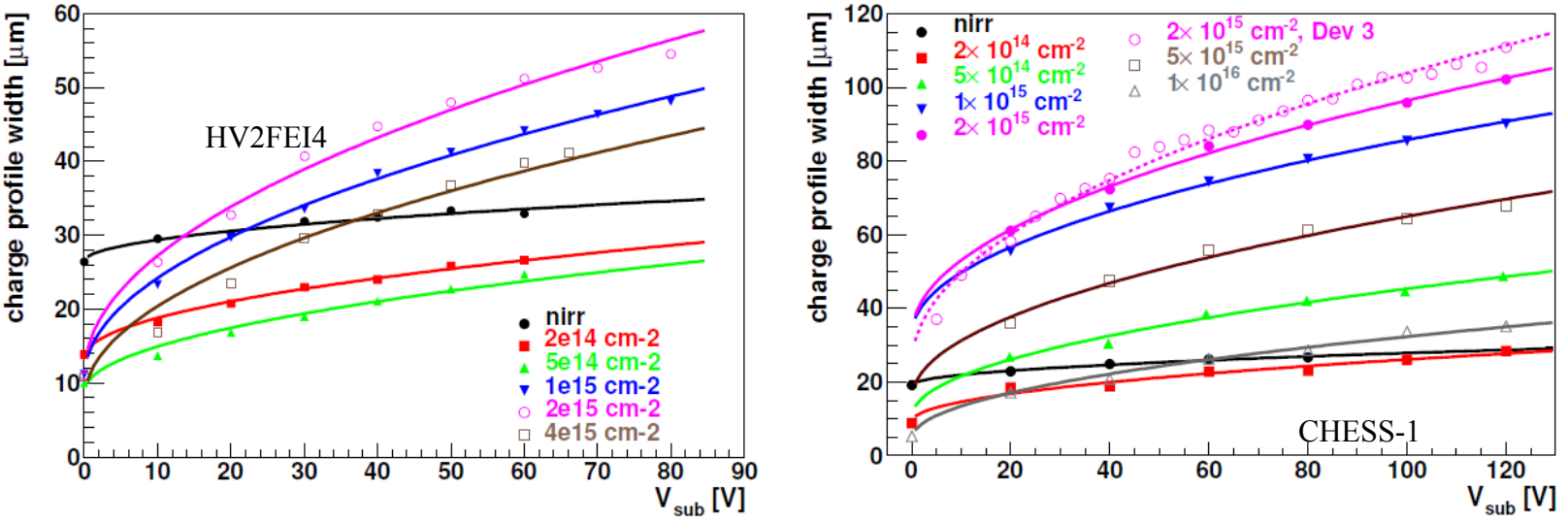
CCPD and monolithic could be more cost effective and meet radiation hardness requirements for the outer layers

HV-CMOS for HEP

Several productions from different foundries have been made
Each with its production technology and wafer resistivity:

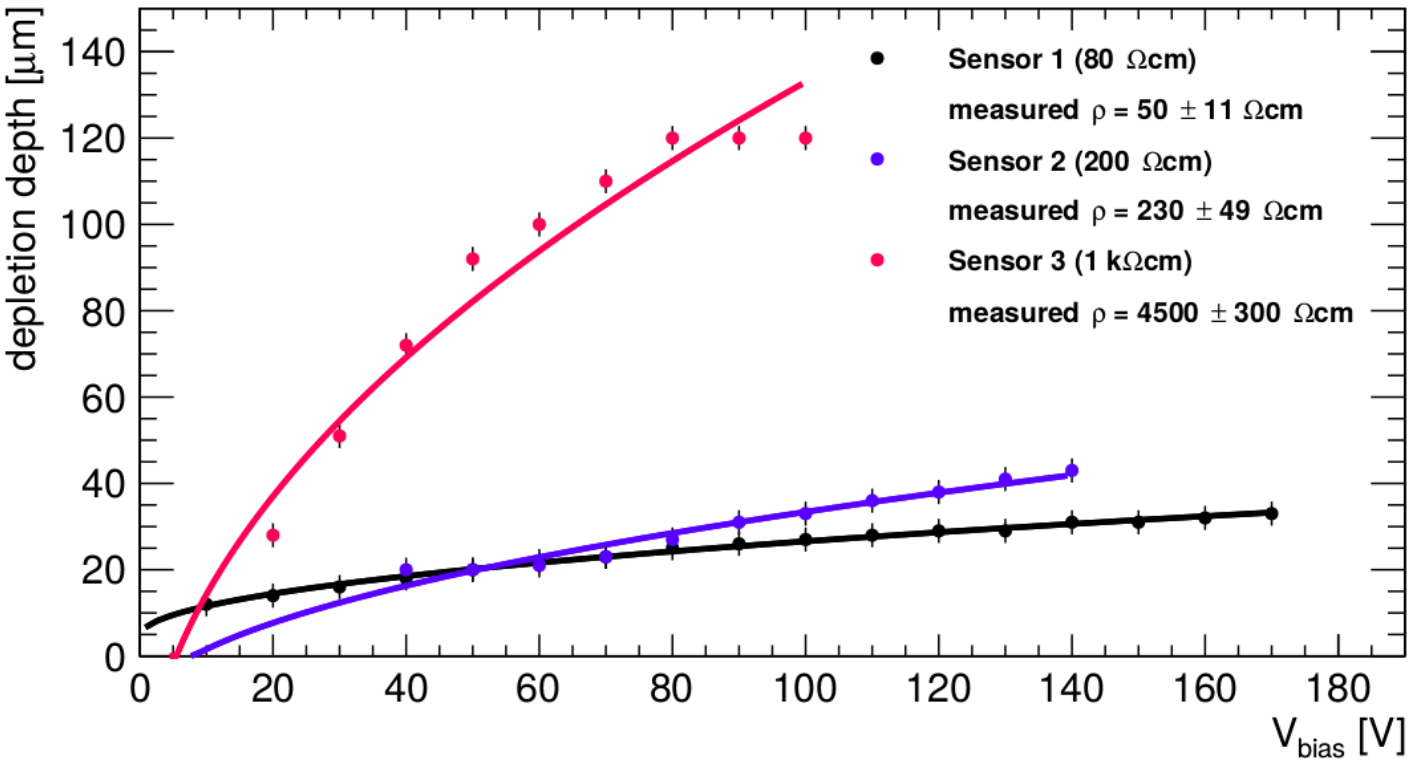
- AMS 350nm, ρ = 20Ω·cm (CHESS-1)
- AMS 180nm, ρ = 10Ω·cm (HV2FEI4)
- LFoundry 150nm, ρ = 2kΩ·cm
- X-FAB 180 nm, ρ = 100Ω·cm

Interesting results have been obtained but it is hard to compare devices from different foundries because of different technologies, substrate doping and well properties



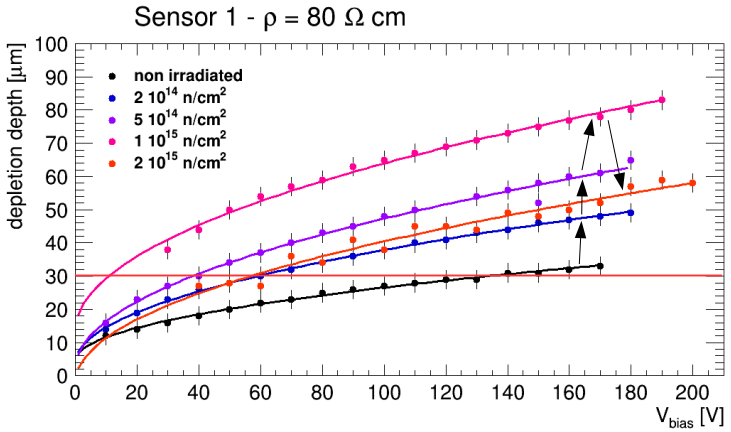
G Kramberger, 27th RD50 Workshop

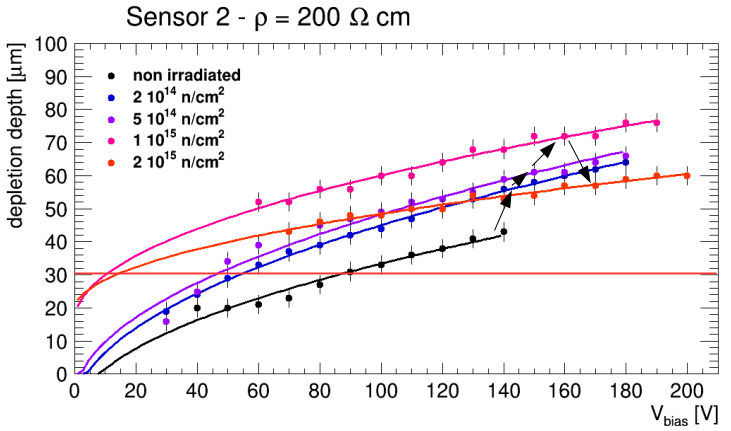
Depletion depth

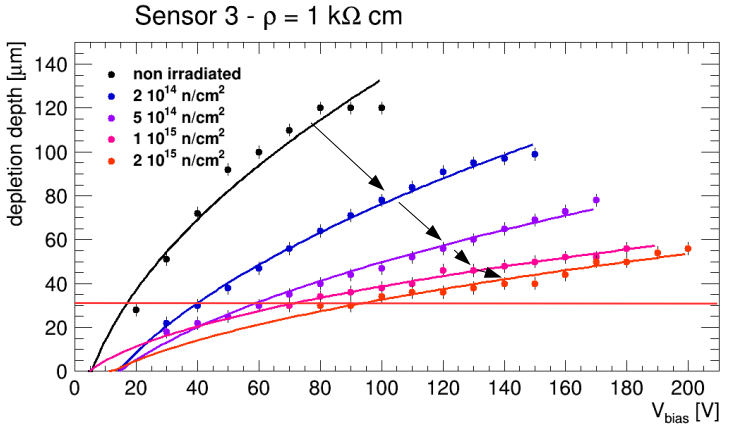


Depletion depth measured with edge-TCT on a scanning TCT set-up

Depletion depth - irradiated







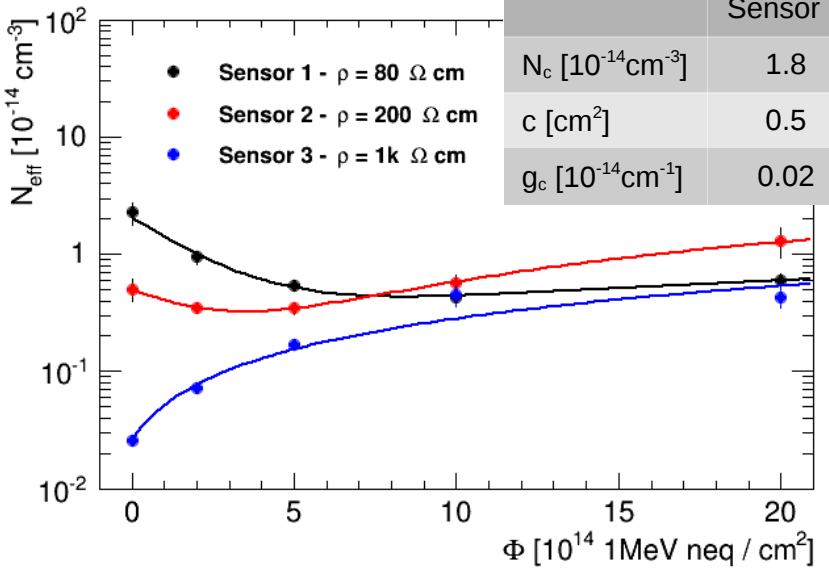
Writing the depletion depth as a function of N_{eff}

$$d(V) = d_0 + \alpha\sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V}$$

A change of the slope means a change in N_{eff}

$$N_{eff} = \underline{N_{eff0}} - \underline{N_c \cdot (1 - exp(-c \cdot \Phi_{eq}))} + \underline{g_c \cdot \Phi_{eq}}$$

Initial doping — Acceptor removal — Radiation induced acceptor introduction



	Sensor 1	Sensor 2	Sensor 3
N_c [10^{-14}cm^{-3}]	1.8	0.4	--
c [cm^2]	0.5	0.3	--
g_c [10^{-14}cm^{-1}]	0.02	0.07	0.03

After irradiation to ~10^{15} 1MeV n_{eq}/cm^2 Neff tends to roughly the same value for all resistivities

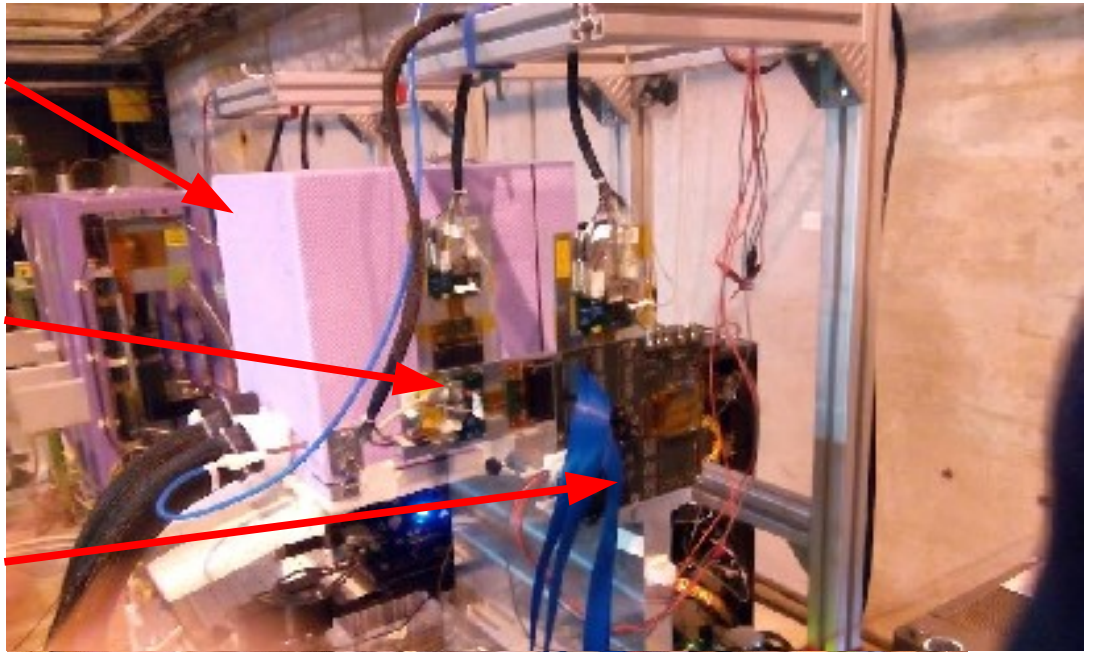
TB set-up

UniGe FEI4 Telescope and IFAE DAQ system for monolithic H35Demo chip

UniGe Cooling box
- Irradiated samples

UniGe Telescope
- 6 x FEI4 planes
- 2 planes rotated 90º
- RCE readout

IFAE H35Demo PCB
- CMOS matrix aligned to the beam

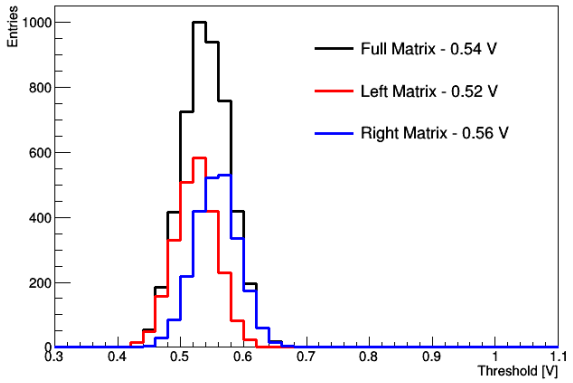


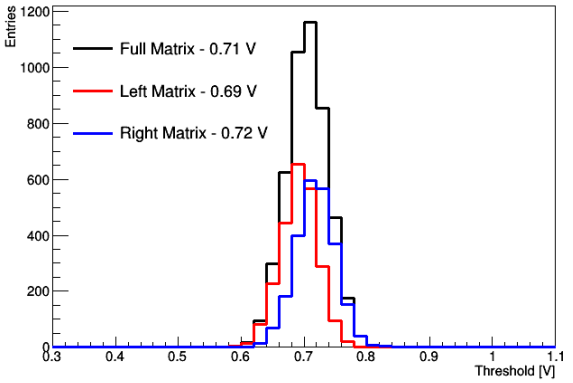
Integration with the Geneva FEI4 telescope (Trigger – busy scheme)

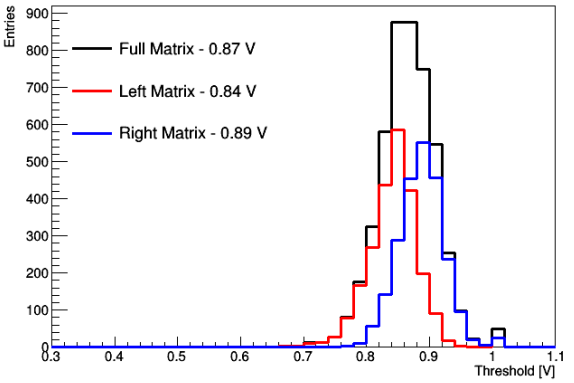
- Triggers from the telescope reach the Xilinx FPGA board
- Busy signal from the FPGA is risen to stop the DAQ until H35 is ready again
- Events are written separately and sequentially by each DAQ system
- System running at 25 ns with ~2 kHz trigger rate

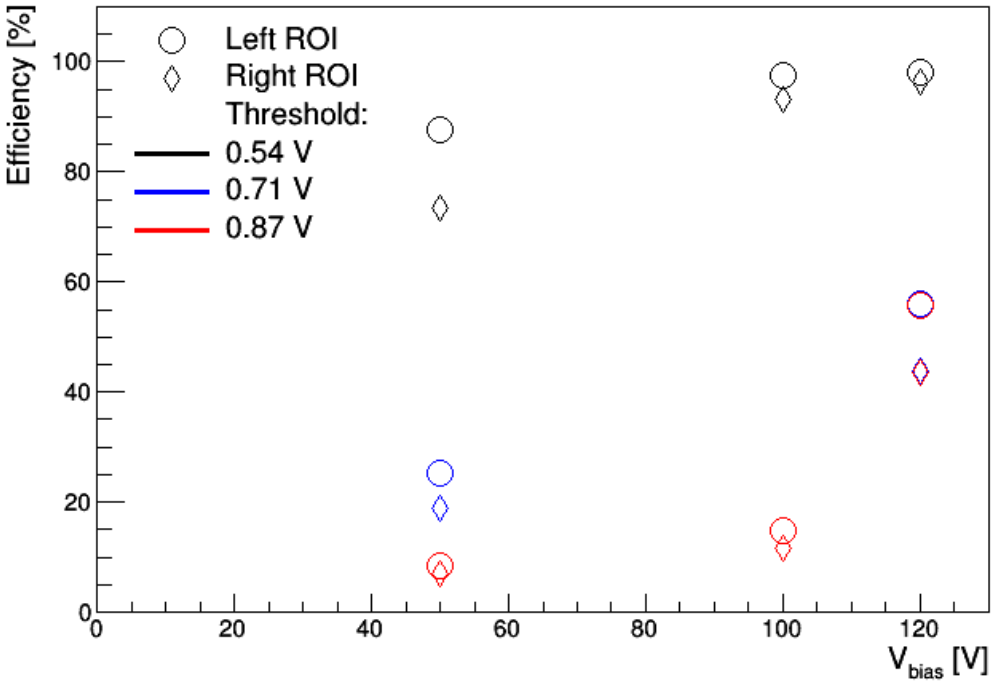
November 2016 TB resumee

Threshold distribution has Left/Right asymmetry, tuning not implemented









Efficiency larger than 96% at 120V and Thr = 0.54V

→ 98% for the Left matrix where threshold is lower

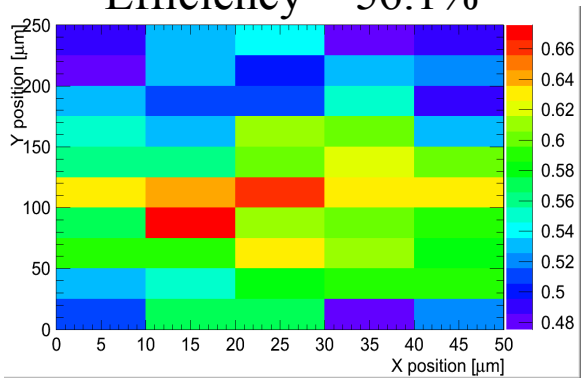
In-pixel efficiency

Threshold dependence

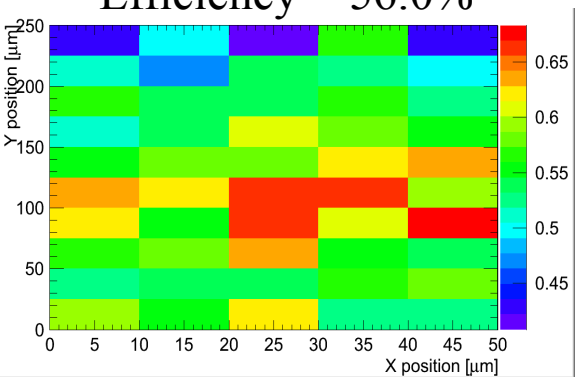
Threshold = 0.87 V | **Threshold = 0.71 V** | **Threshold = 0.54 V**

Left

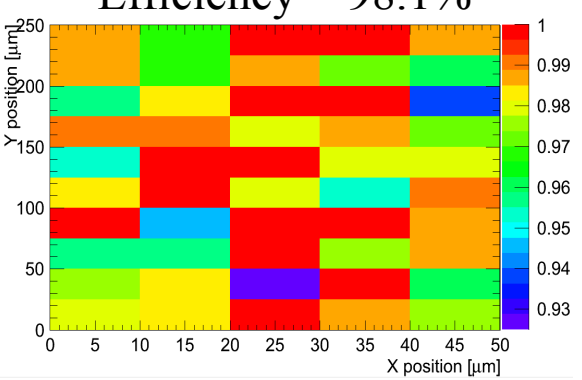
Efficiency = 56.1%



Efficiency = 56.0%

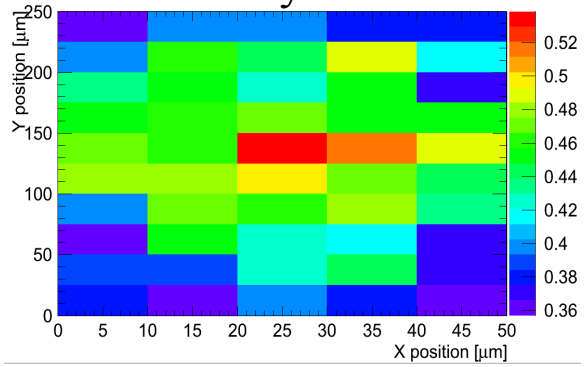


Efficiency = 98.1%

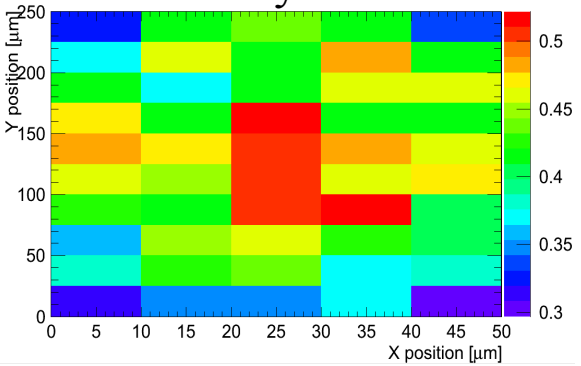


Right

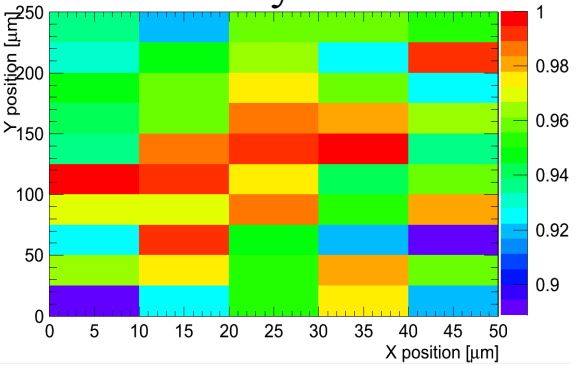
Efficiency = 42.9%



Efficiency = 42.3%



Efficiency = 96.3%



V_{bias} = -120 V

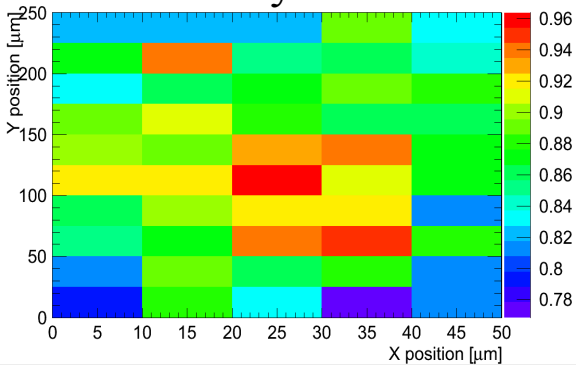
In-pixel efficiency

Bias voltage dependence

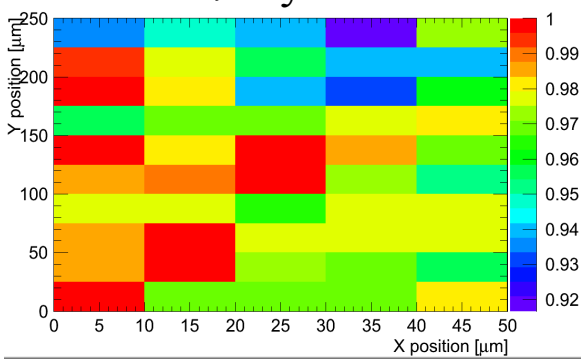
V_{bias} = 50 V **V_{bias} = 100 V** **V_{bias} = 120 V**

Left

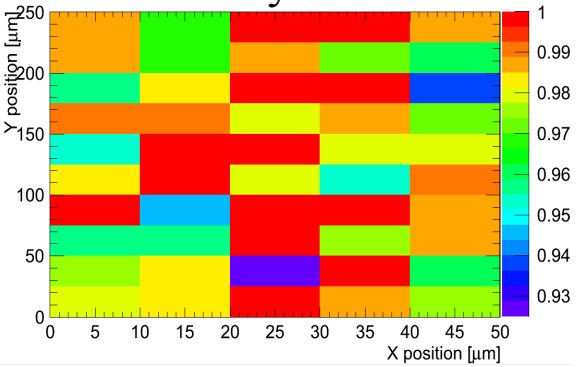
Efficiency = 87.1%



Efficiency = 97.2%

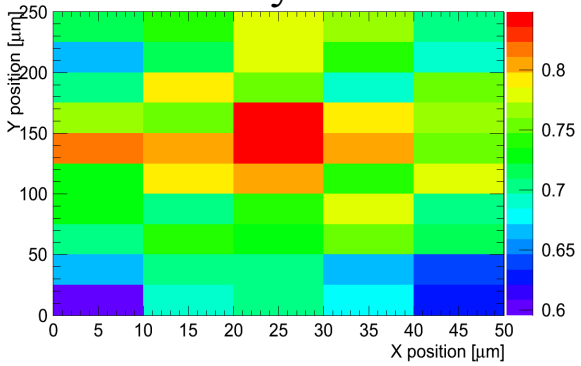


Efficiency = 98.1%

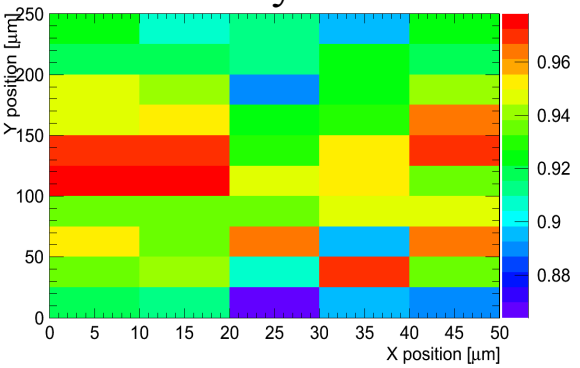


Right

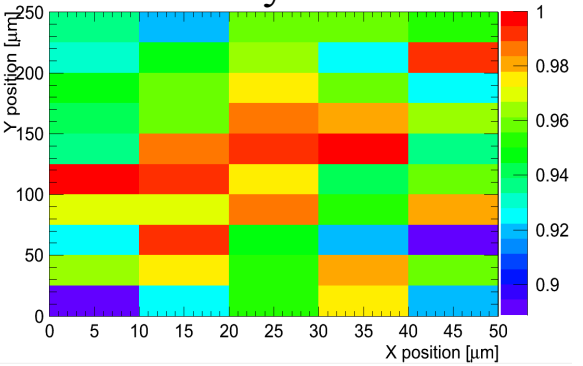
Efficiency = 73.5%



Efficiency = 93.4%



Efficiency = 96.3%



Threshold = 0.54 V