Contribution ID: **24** Type: **not specified**

HV-CMOS testing and design

Wednesday 7 June 2017 11:10 (20 minutes)

The ATLAS collaboration is studying the possibility to install HV-CMOS devices in the outermost layer of the upgraded pixel detector of the ATLAS ITk for HL-HLC.
For this purpose different technologies are being investigated and different prototypes have already been produced and tested.
IFAE is participating both in design and testing of HV-CMOS devices.
Beam test results of the monolithic matrices of irradiated and non irradiated H35Demo devices will be presented. Moreover the IFAE contribution to the design of different HV-CMOS chip productions will be shown.

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Session Classification: CMOS