Recent progress of the RD50 collaboration towards an R&D HV-CMOS submission in the 150 nm node from LFoundry

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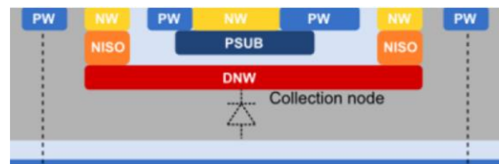
Outline

1. Technical features of available foundries
2. Our experience with LFoundry
3. Short term plans
4. Longer term plans
5. Summary

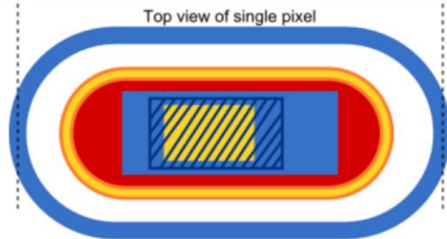
Technical features

Foundry	Feature node [nm]	HV [V]	HR [Ω·cm]	Depletion region [μm]	P-N wells	Metal layers	Backside biasing	Stitching	TSV
ams	350 180	<150	20 – 1k 10 – 1k	140	Triple	4 6	No	No	Yes
LFoundry	150	<120	10 – 4k	170	Quadruple	6	Yes	Yes	No
TowerJazz	180	<6	1k – 8k	18 – 40	Quadruple	6	Yes	No	No
XFAB	180	<200	100	–	BOX layer	7	No	No	No
ESPROS	150	<20	2k	50	Quadruple	6	Yes	No	No

Sensor cross-section:



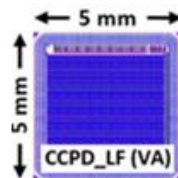
C_{PSUB_DNWELL} non-negligible

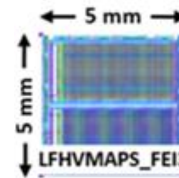


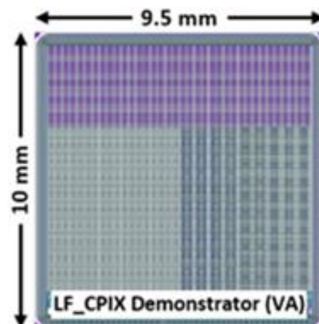
P. Rymaszewski, JINST 11 C02045, 2016

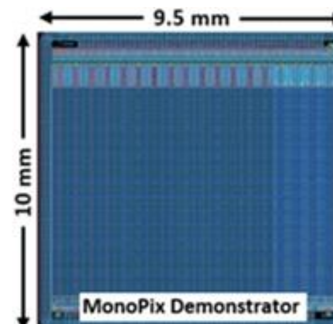
- Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode).
- Full CMOS electronics are possible in the sensor area.

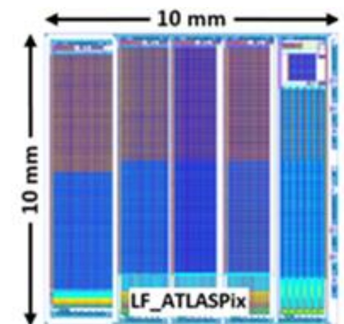
Prototypes:











Our experience – LF design

5 mm

5 mm

1)

2)

3)

LFHVMAPS_FEI3 (LF2). Areas from top to bottom:

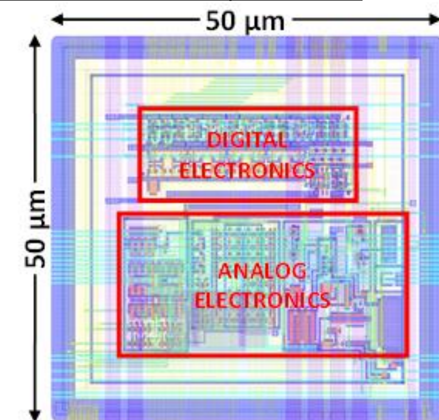
1) Test structures

- TCT/e-TCT
- sensor capacitance measurement
- very fast measurements

2) Non-HEP matrix

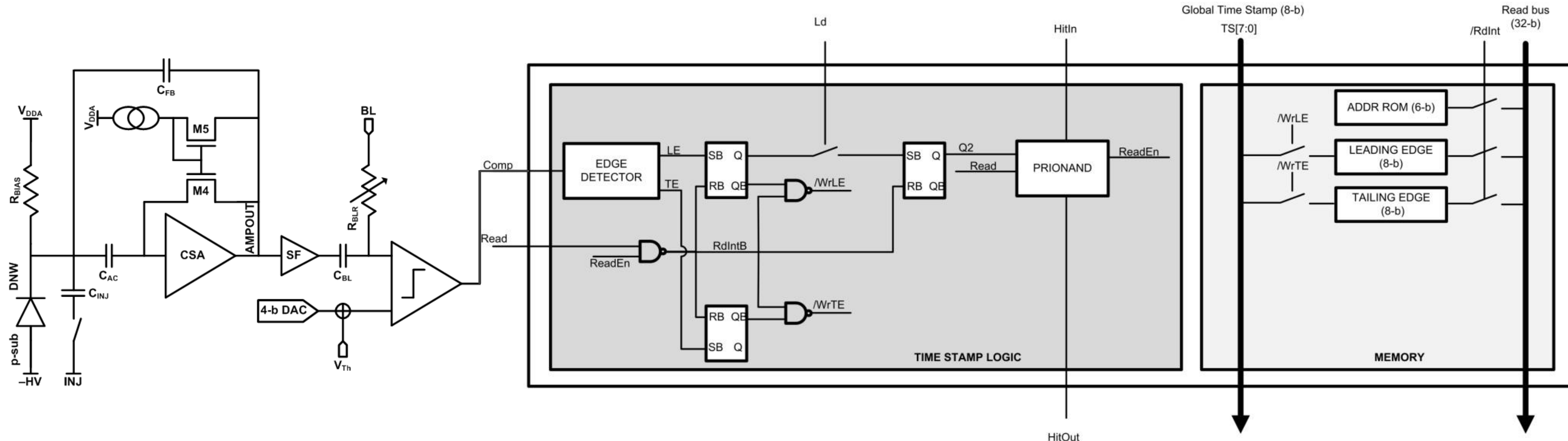
3) Matrix of HV-MAPS pixels with FE-I3 style readout

- 40 rows x 78 columns of pixels
- pixel area is 50 µm x 50 µm
- analog and digital readout electronics are embedded inside the pixel area



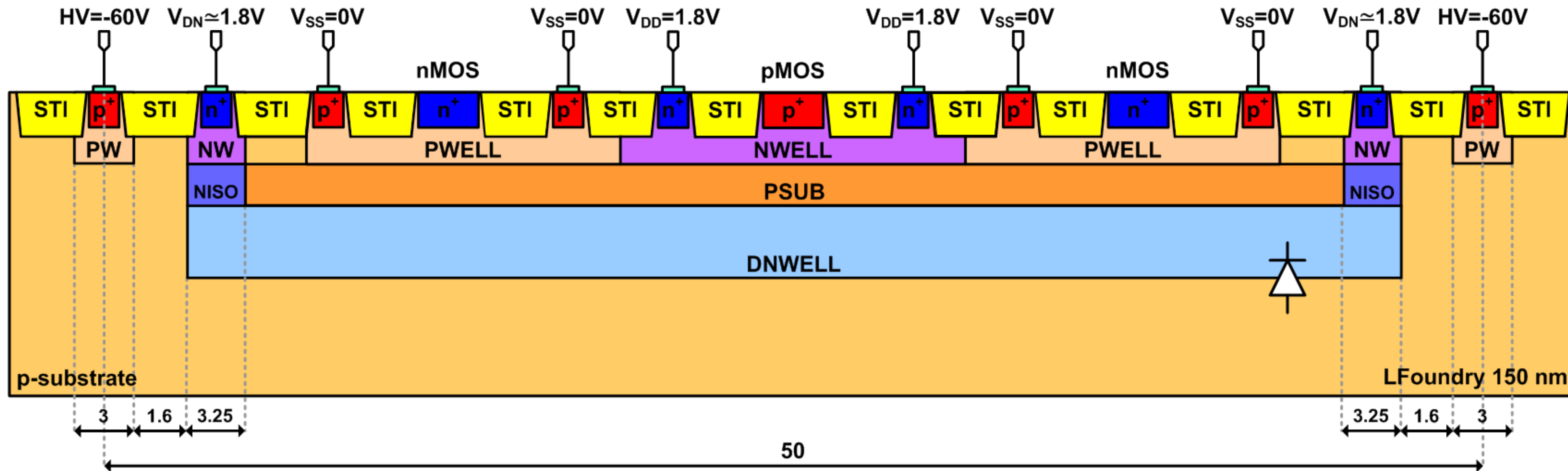
- Fabricated resistivities are 500 Ω·cm and 1.9k Ω·cm
- Detector thickness is 280 µm
- No backside biasing option

Our experience – LF design



- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
- The **digital readout** is based on FE-I3 style:
  - **Two 8-bit DRAM memories** that continuously store two time stamps (Leading Edge, Trailing Edge)
  - ToT = TE – LE (off-chip)
  - **One 8-bit ROM memory** to store the pixel address
  - **Electronics (edge detector)** to process the output of the discriminator and tell when the LE and TE have to be stored
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz
- Total power consumption per pixel is ~27 µW (pre-amplifier current is <10 µA)

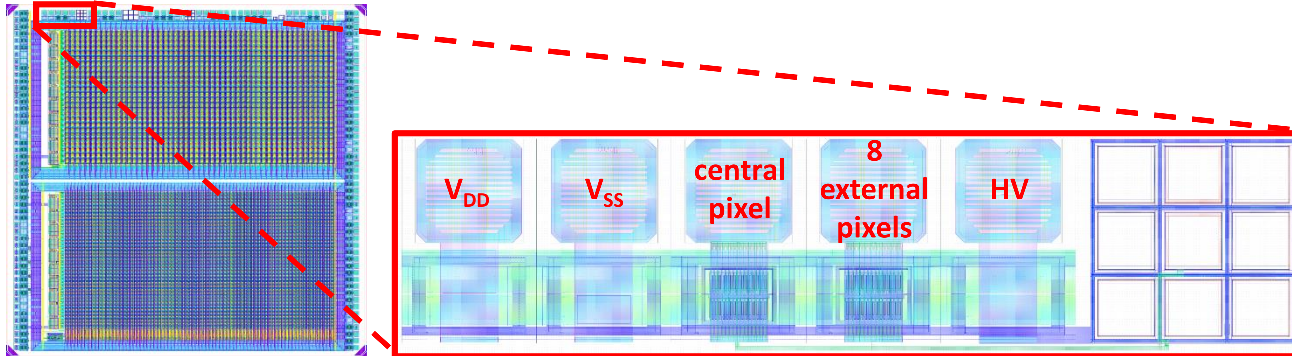
Our experience – LF design



- The sensing diode is a DNWELL/p-substrate junction
- The DNWELL can be isolated from PWELLs/NWELLs thanks to the PSUB layer
- **Therefore, it is possible to have fully CMOS electronics inside the pixel area**
- In our case, we have multiple PWELLs and NWELLs:
  - 1 PWELL/NWELL for the CSA and the shaper
  - 1 PWELL/NWELL for the CMOS discriminator
  - 1 PWELL/NWELL for the digital readout
  - 1 NWELL for the pMOS transistors of the sensor bias circuit (this NWELL is connected to the DNWELL)
- The DNWELL is biased through an n^+/NWELL/NISO structure

Our experience – LF measurements

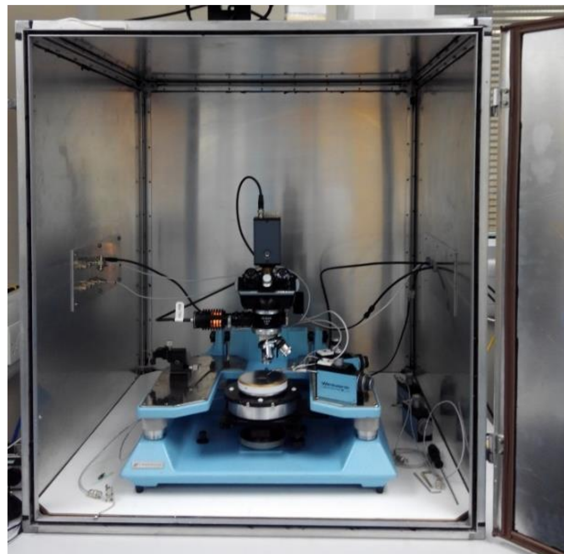
Circuit:

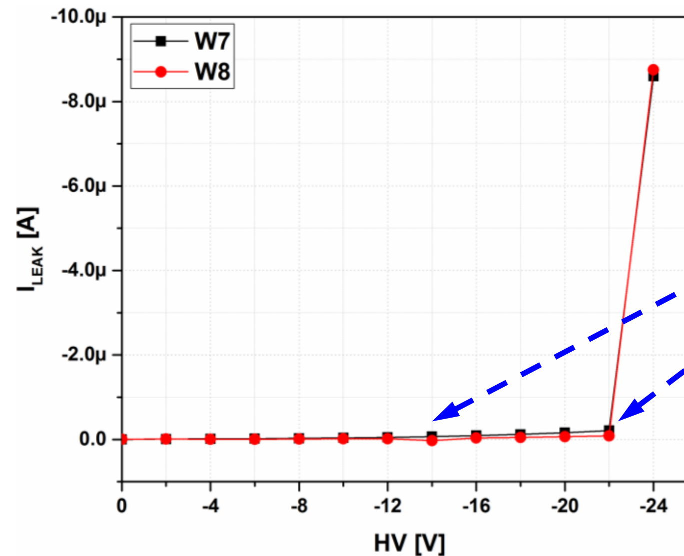


Test structure for eTCT:

- 3 x 3 matrix of HV-CMOS pixels
- pixel size is 50 µm x 50 µm
- no readout electronics

I-V measurements with probe station:





Matrix of pixels with FE-I3 style readout:

- currently testing the readout electronics, just started
- we'll know more soon

Too high leakage current

Too low breakdown voltage

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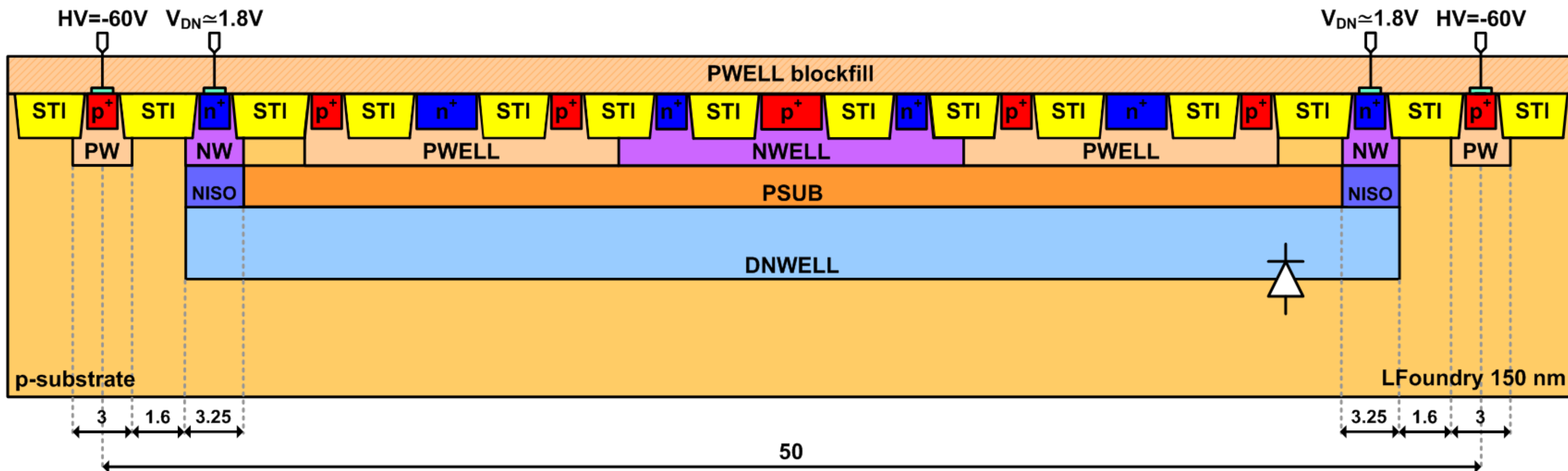
What did go wrong?

- LFoundry informed us that the V_{BD} of a PWELL/NWELL junction is ≃24 V
- LFoundry is a technology with *Design-For-Manufacturing post-processing* that includes:
  - Autogeneration of PWELL → Can be avoided drawing PWELL blockfill in the design (we did)



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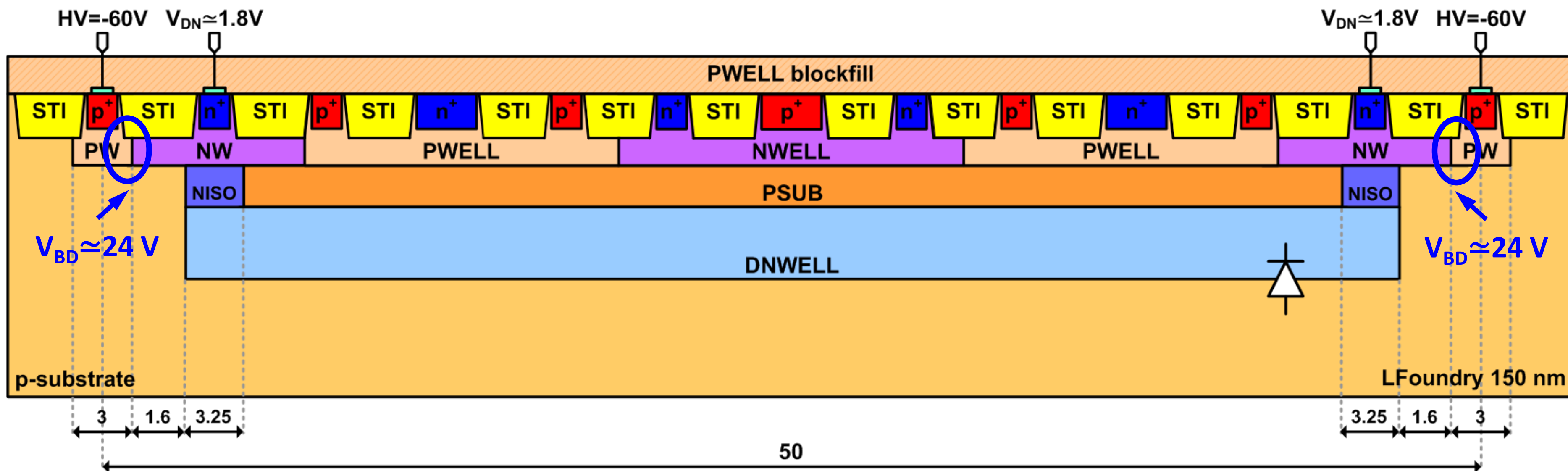
  - Autogeneration of NWELL → Can be avoided drawing NWELL blockfill in the design (we didn't do)
  - As a result of that, the V_{BD} we see is between the PWELL/NWELL junction and not between the p-substrate/DNWELL junction



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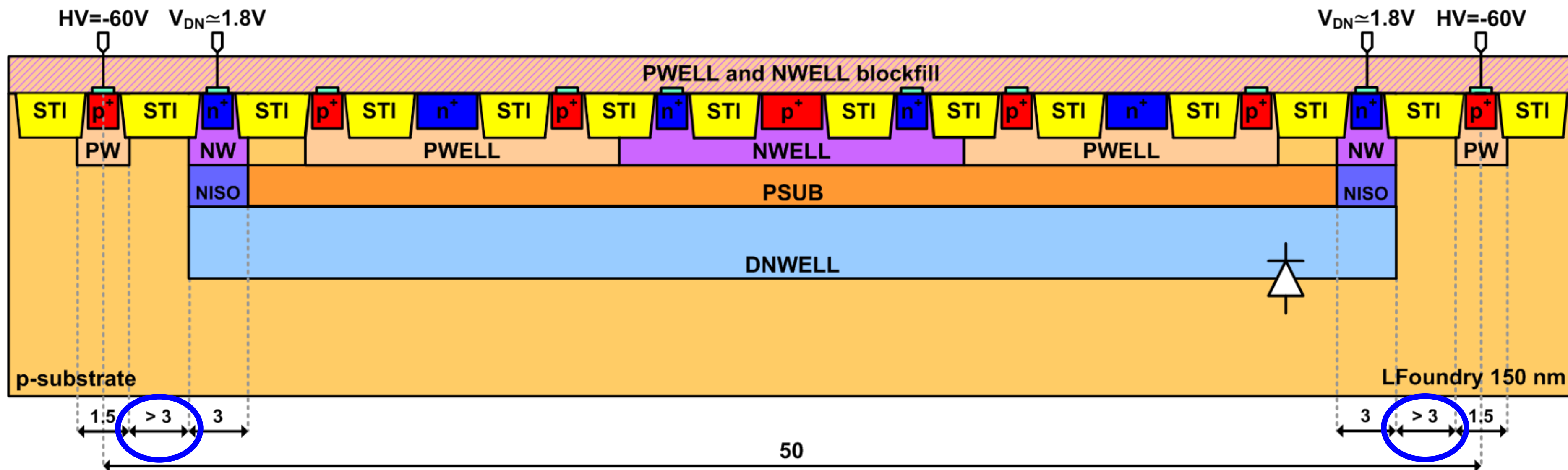
  - As a result of that, the V_{BD} we see is between the PWELL/NWELL junction and not between the p-substrate/DNWELL junction
- In addition to that, if we want high V_{BD} (> 60 V), we need to increase the PWELL/NWELL separation to > 3 µm (with 3 µm, V_{BD}≃75 V with standard resistivity substrate) → This forces us to re-design the pixel



- We now know how to fix this

Sensor parasitic capacitance

- **TCAD simulations** → Done by Lingxin Meng (Uni. Liverpool) and Jens Dopke (RAL) using TCAD_15 A files set provided by LFoundry

- For a 50 μm x 50 μm pixel with PSUB full coverage of the NISO enclosed area:
  - The total value is → 520 fF
  - PSUB/DNWELL junction → ≃400 fF (times 2?)
  - DNWELL/p-substrate junction → ≃30 fF (times 2?)
  - Corner and edge effects → ≃90 fF
- It is mandatory to minimize PSUB

- LFoundry has given us permission to make PSUB smaller than the NISO enclosed area
- Final PSUB/DNWELL capacitance will depend on the size and number of pMOS transistors
- Need to leave 1 μm overlap between PWELL and PSUB to avoid punch-through between the NWELL and DNWELL

Short term plans

- We think it is mandatory to **fabricate a small free-of-errors design** and prove that sensors + readout electronics work well before submitting a large very expensive MLM/engineering run
- We are currently working towards the **design of a small MPW**
  - **What will this design include? →** - Re-designed matrix with 50 µm x 50 µm "à la FEI3" FEI3 pixels
    - It's "only" a re-design (less time needed)
    - We think this is very interesting for the community

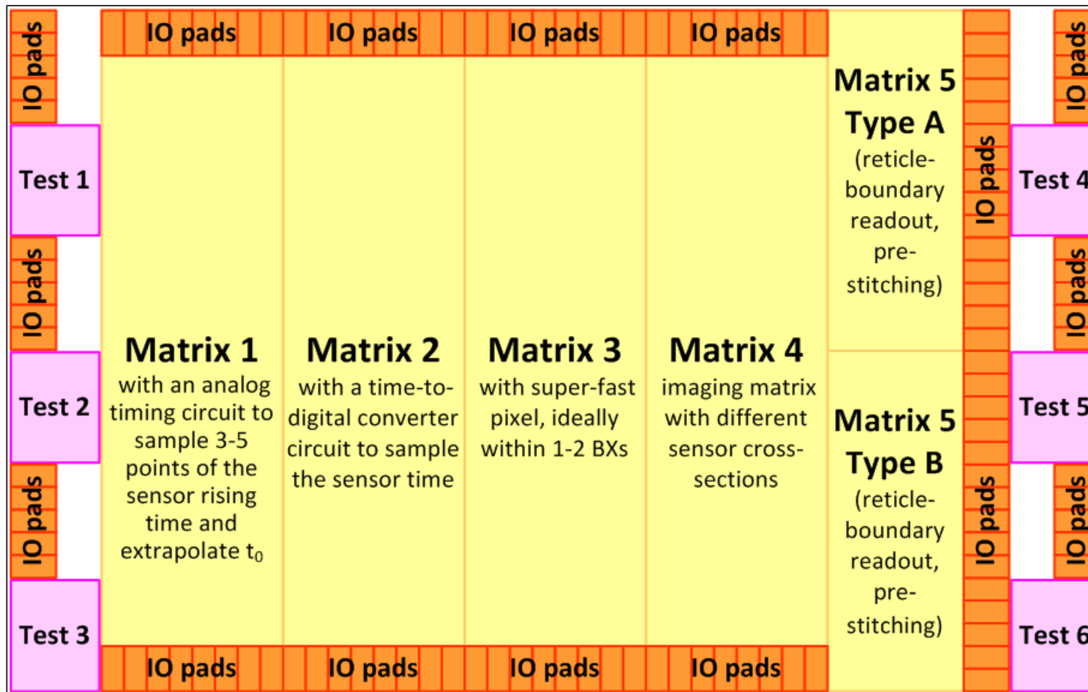
    - If time allows, also a small version of matrix 1 with analog sampling circuits (please, see slides 15-16)

    - Test structures for TCT/e-TCT

    - Re-designed I/O pads with DNWELL (instead of NISO) as the deepest layer for additional isolation from the substrate
  - **PDK version →** V1.1.0 (with improvements with respect to previous versions)
  - **Submission date →** Next possible MPW is 14-August-2017
  - **Area →** Minimum possible area allowed by LFoundry for MPW production (6 mm^2)
  - **Price →** 900 €/mm^2 + VAT

    For 6 mm^2, the price is 5400 € + VAT (1 wafer with standard resistivity and 40 chips)
  - We are looking for funding options

Longer term plans – MLM/Engineering run



CERN/RD50 collaboration:

- International project to develop radiation hard semiconductor devices for very high luminosity colliders

Target of this submission:

- Improve the timing resolution of HV-CMOS sensors with different solutions implemented at the readout circuit level
- Study new sensor cross-sections
- Study pre-stitching options (increase the device area beyond the reticle size limitation)

Technology:

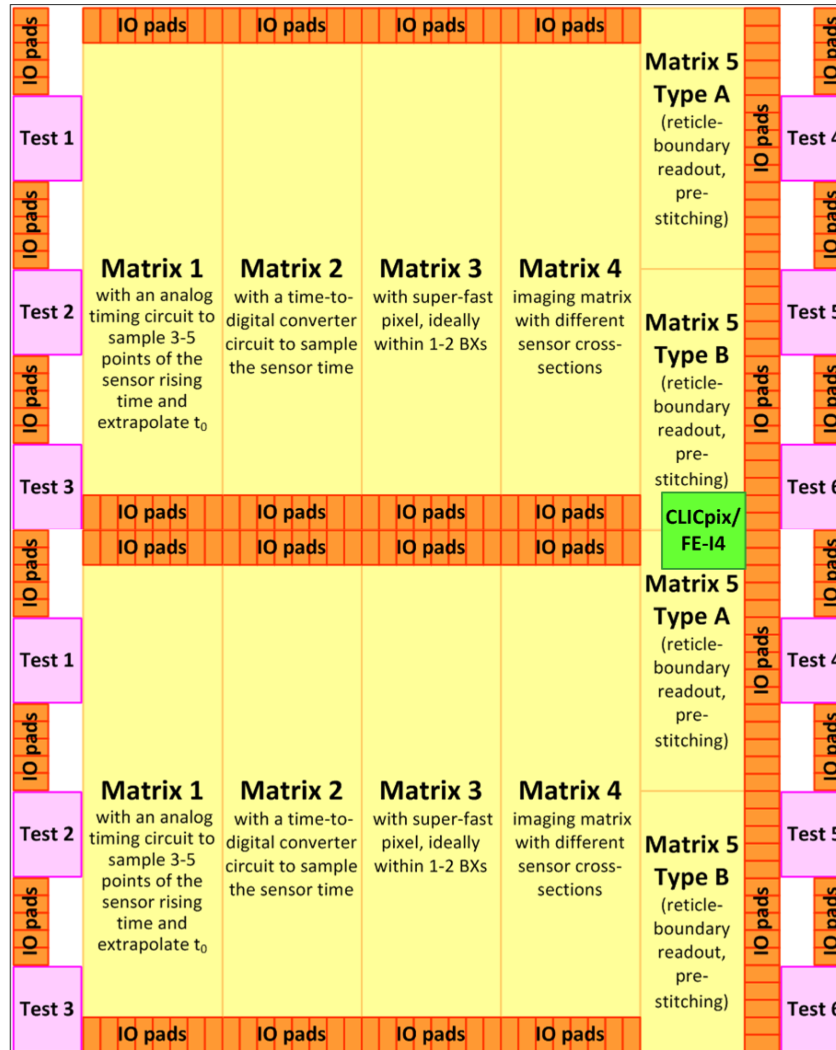
- 150 nm HV-CMOS from LFoundry

Design effort:

- IFAE (R. Casanova)
- Uni. Barcelona (O. Alonso)
- Uni. Liverpool (S. Powell, E. Vilella and C. Zhang)
- FBK (N. Massari and M. Perenzoni)

Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

Longer term plans – MLM/Engineering run



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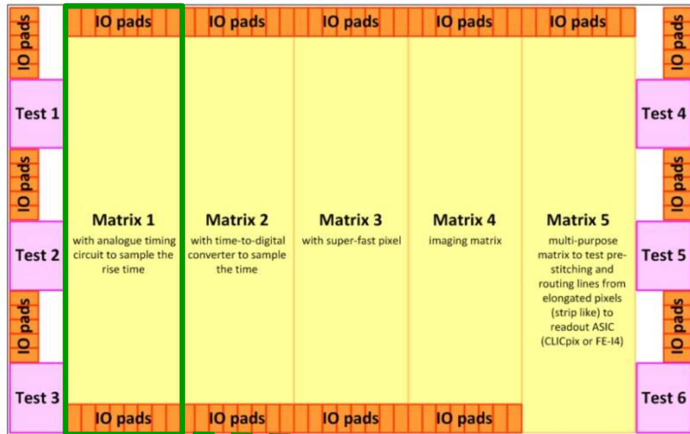
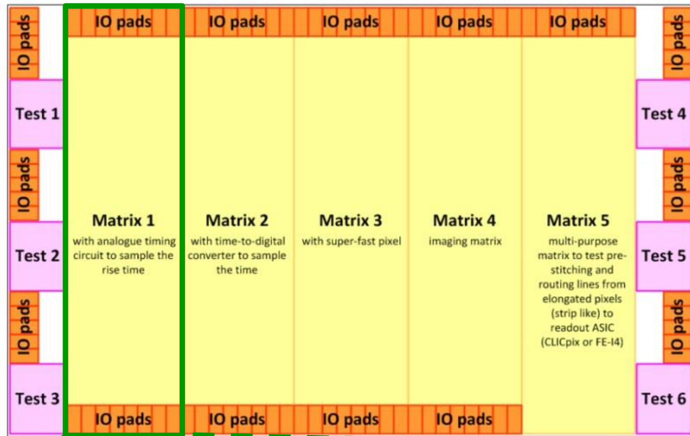
MLM/Engineering run – Matrix 1



Matrix with analog sampling circuit:

- Chain of delay elements to generate WR_0, WR_1, …, WR_n (signals to enable writing the sensor analog value, i.e. the voltage) when there is an event
- First value is the baseline voltage
- Time-stamp of first value + programmable delay
- Analog memories based on metal-insulator-metal capacitances (< 5 per pixel)
- Analog serializers to send the data off-chip + off-chip ADCs
- Off-chip processing to determine t_0 (time of event)

MLM/Engineering run – Matrix 1



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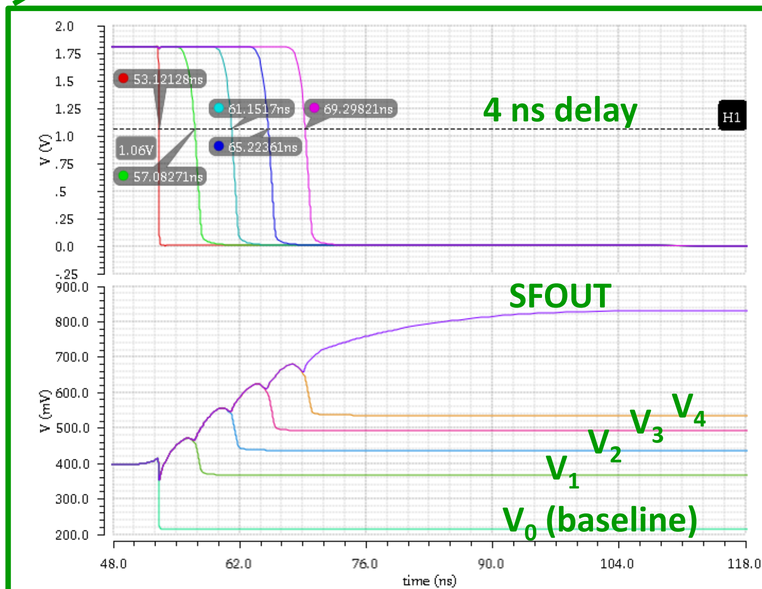
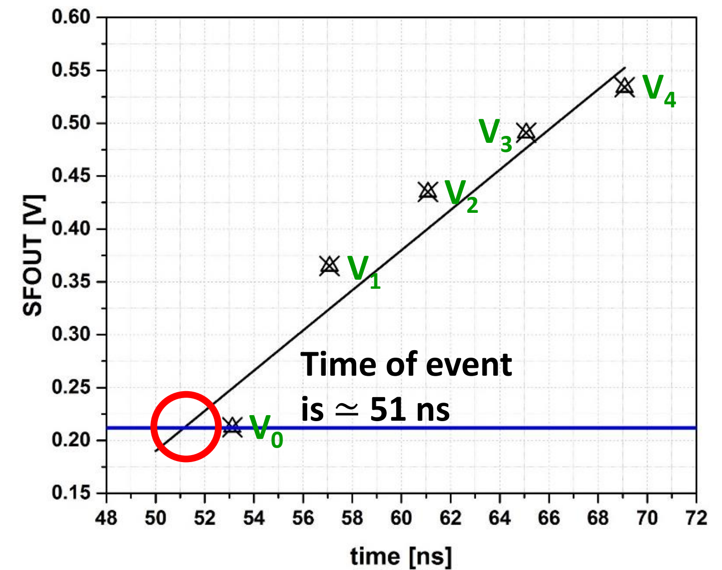
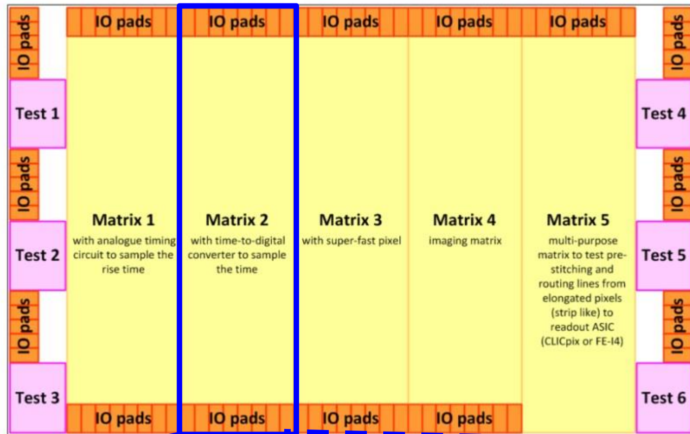


Off-chip processing →



MLM/Engineering run – Matrix 2



Matrix with in-pixel Time-to-Digital Converter (TDC):

- Leading Edge and Trailing Edge time stamp capture
- TS measured with 2.5 ns accuracy:
  - Coarse time measurement (25 ns accuracy) → global time stamp
  - Fine time measurement (2.5 ns accuracy) → TDC

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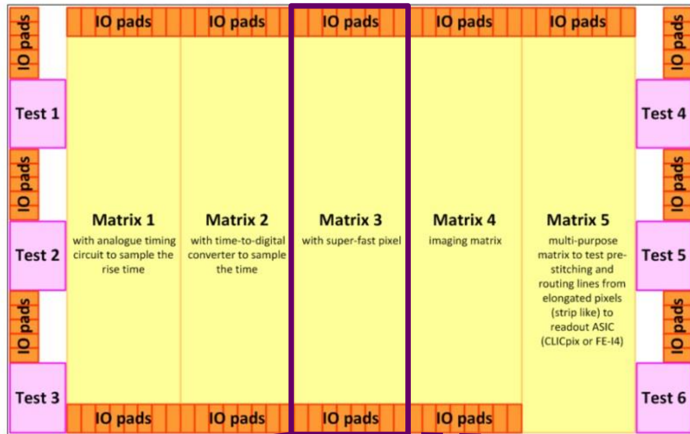
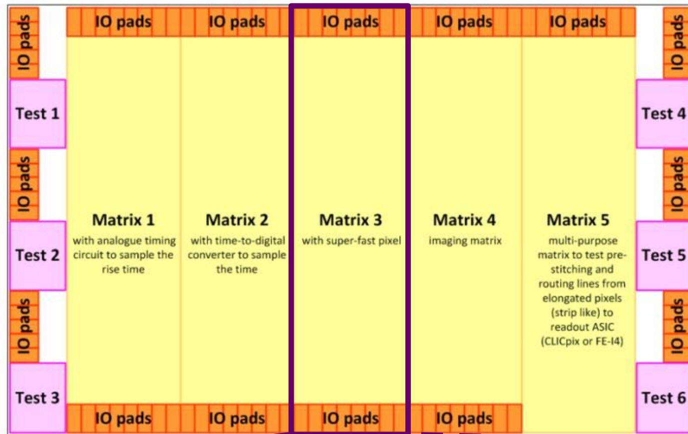
MLM/Engineering run – Matrix 3



Matrix with very fast amplifier:

- The target is to recover BL voltage after an event in < 2 BXs
- **Option 1** → Amplifier with continuous slow reset + switched fast reset
- The output of the comparator is used to enable the fast reset when there is an event
- The current consumption is slightly higher only when there is an event (total power consumption per pixel is ≃ 30 μW)
- Total recovery time < 50 ns (independent of input energy)
- No ToT info is possible

MLM/Engineering run – Matrix 3



Matrix with very fast amplifier:

- The target is to recover BL voltage after an event in < 2 BXs
- **Option 2** → Fast amplifier with continuous reset
- Optimized transistor sizing and biasing
- Total recovery time is ≃ 50 ns (dependent on input energy)
- ToT info is possible

Summary

- The **150 nm HV-CMOS technology from LFoundry** is attractive for HEP applications as
  - it is a HV/HR technology
  - CMOS electronics inside the pixel area are possible
  - there is a high number of metal layers for routing
  - backside biasing is possible
  - stitching is also possible
  - it offers cost-efficient prototyping
- Our current experience with LFoundry relies on an MPW where the sensors need to be improved
- We need **more studies on the sensor parasitic capacitance**
- We need to **re-design the pixels and submit this as a second MPW** before submitting a large very expensive MLM/engineering run
- We are **currently working for this second MPW**, which will contain
  - re-designed matrix with 50 µm x 50 µm "à la FEI3" FEI3 pixels
  - a small version of matrix 1 with analog sampling circuits (if time allows)
  - test structures for TCT/e-TCT
- Our longer term plans, include the **submission of an MLM/engineering run** with
  - 3 matrices of pixels with solutions implemented at the readout circuit level to improve the sensor timing resolution
  - 1 matrix of pixels with new sensor cross-sections
  - 1 matrix of pixels to study pre-stitching options
  - several test structures

Many thanks for your attention!