

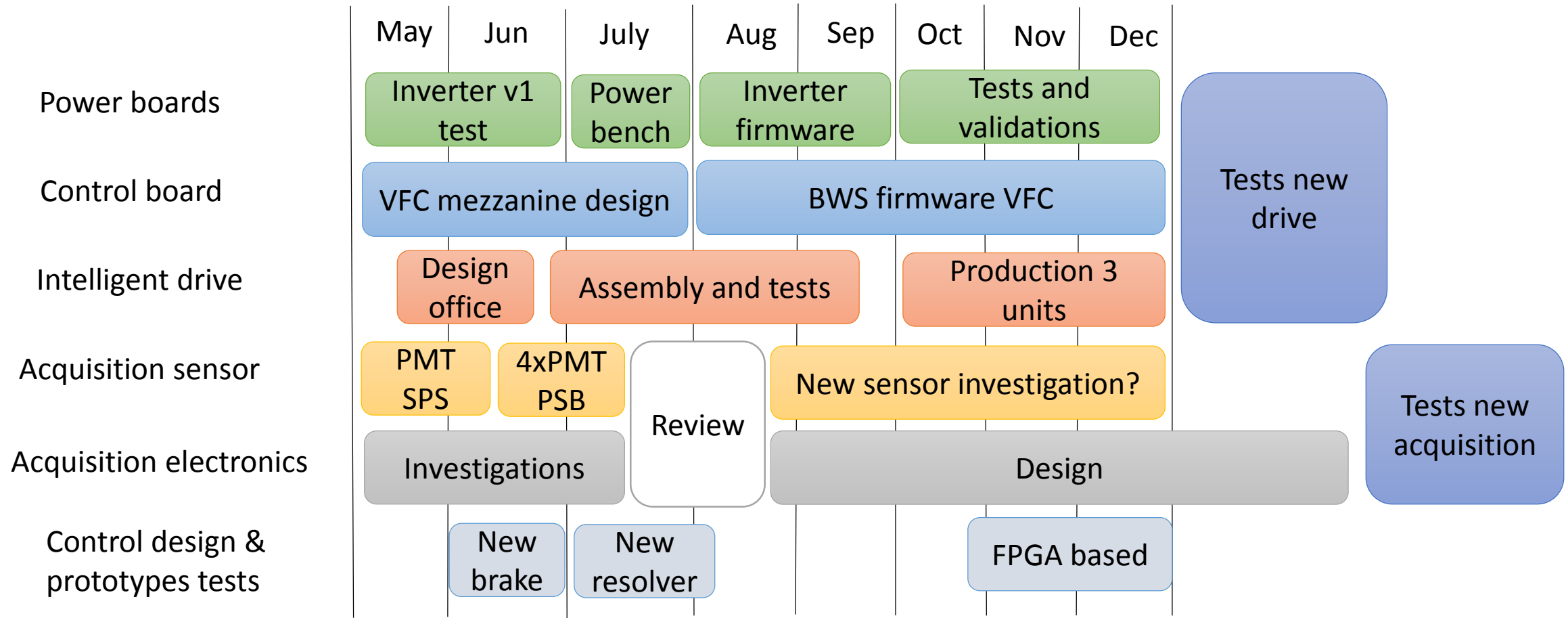


Working plan for 2017 Acquisition and Control Electronics

J. Emery for the wire-scanner
Inputs from Federico, Patrik & Jose



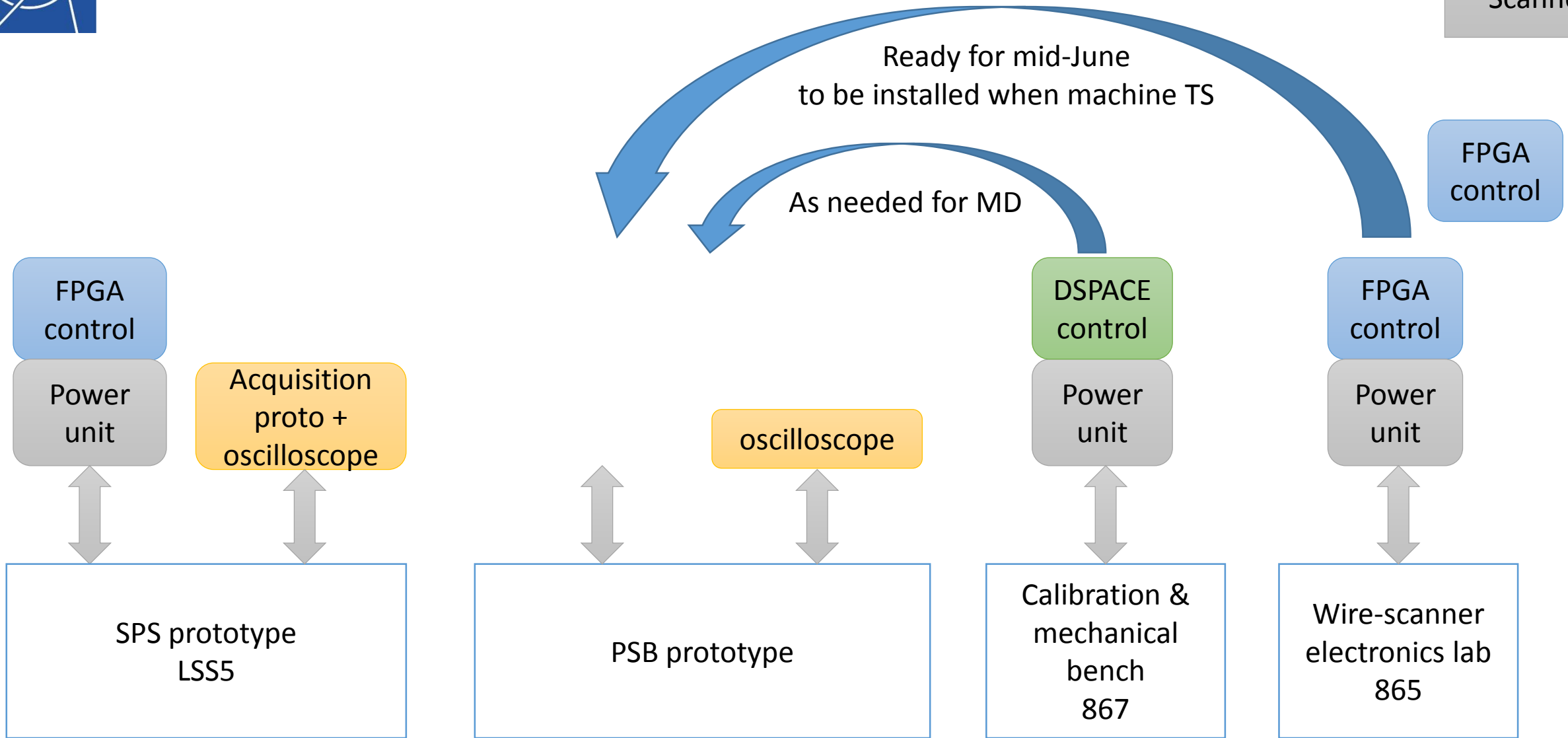
Work plan for the electronics





Electronics system usage for 2017

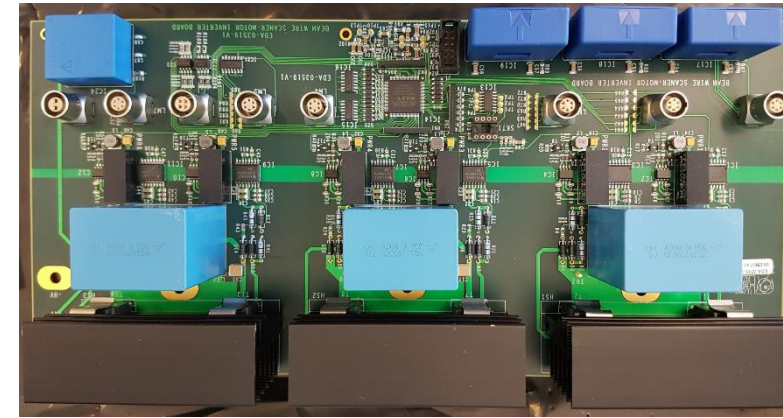
BE-BI
Beam Wire
Scanner



Motor Inverter and Cap.charger board status

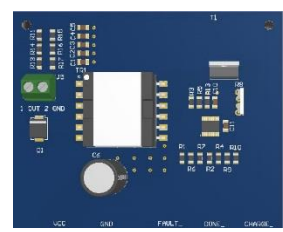
1. Motor Inverter Board

- Recived and under test.
- Will need 1 week more for basic functional test.
- 2 week's of firmware test.
- Second stage is to build up a labview test system. Which is needed because no access to the Dspace system. Is around 2 weeks programming and then 1 week test.
- **But the board need to be tested with Dspace and the motor, as soon as possible(August maybe?).**
This is needed for to be able to do a stress test.



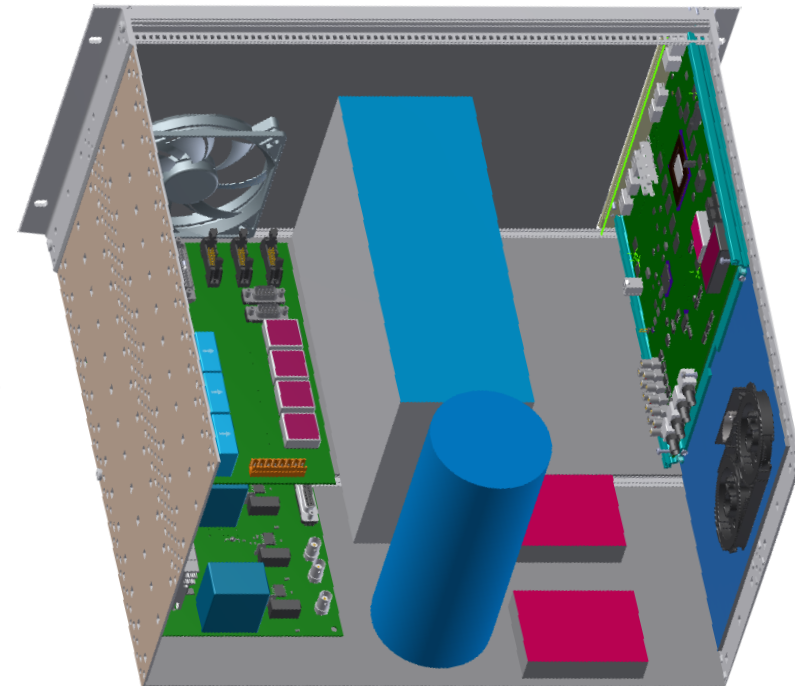
2. Cap.charger.

- Under production, could be ready end of next week 19/05.
- The it will need 1-2 week's of testing.



Intelligent drive integration

- The integration will start in July 2017.
- Missing mechanically part's is following.
 - Support Motor inverter board
 - Baseplate for the 19" box.
 - VFC & Meazzine mechanic unit.
 - Front panel and back panel,
first design done but need to be update for the VFC & Meazzine unit.
 - All this need to be designed and manufactured under May and June.



Detection and HDR Coverage

Readout & Acquisition

Back-End System (VME)

Architecture Definition

Common for all machines:

- BC-408 Scintillators
- Filter-Wheel (even if unused)
- Quad Metal package PMTs
- Active PMT bases

PSB / PS → Surface Readout (Rad, Cable lenght...)

Fast Digitalization & Digital Integration

- Resource sharing with FBCT Developments?
- FMC228 Commercial Board
- 4 x 12b ADC @ 1GSPS (600MSPS with VFC)

LHC / SPS → Tunnel Readout

Analog Integration & 40 MHz Digitalization

- GEFE + ICECAL FMC Based
- Optical GBT-link to VFC
- BST Synchronization

Common for all machines:

- VME FMC Carrier Board

Developments
2017

Procurement / Tests:

- Active Bases + PMT
- Check Rad-Tol.

Stepper motor control:

- Usage of BSRT drivers

Build PSB replica for lab tests

PSB/PS Actions:

- PMT Signal conditioning circuit
- ADC FMC interface with VFC

LHC/SPS Actions:

- ICECAL FMC PCB Design
- GEFE Experimentation
- GEFE Firmware & VFC interfacing

Important decisions to make at this stage...
Soon a design review will give some light on how to proceed

Preliminary board tests:

- Ethernet Comm.
- DDR3 Memory management
- GBT Core implementation
- Find sinergies with FBCT?

Firmware developments

Plans

Proposed Plan for 2017 (As I see it, but to be discussed...)

- Priorice on PSB/PS (BWS Prototypes for these injectors are incoming)
- Check with experts if architecture is feasible/convenient.
- Purchase required components for a complete test/system based on FMC228 & VMC (PMTs, Bases, FMC Card, VFC...)
- VFC firmware developments / Expert application for system operation.