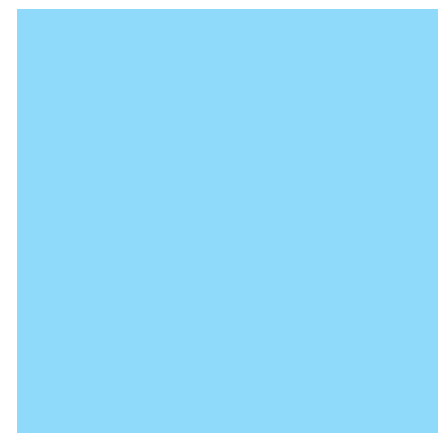




SHiP
Search for Hidden Particles



SHiP Data AcQquisition

Giovanna Lehmann Miotto CERN EP/DT-DI
On behalf of the DAQ team

+ Outline

- Architecture Overview
- Design options for back-end data flow
- Design options for detector FE interface
- Summary and Outlook



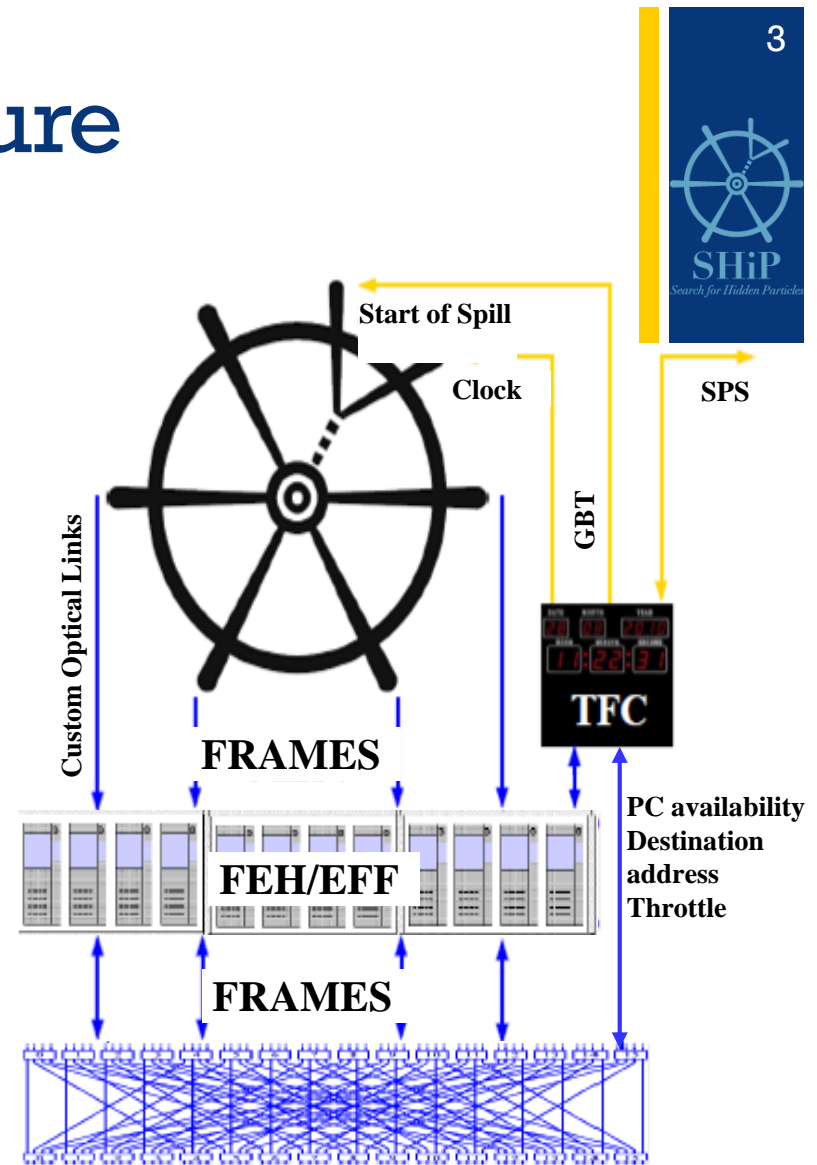
+ SHiP TDAQ Architecture

■ Main components

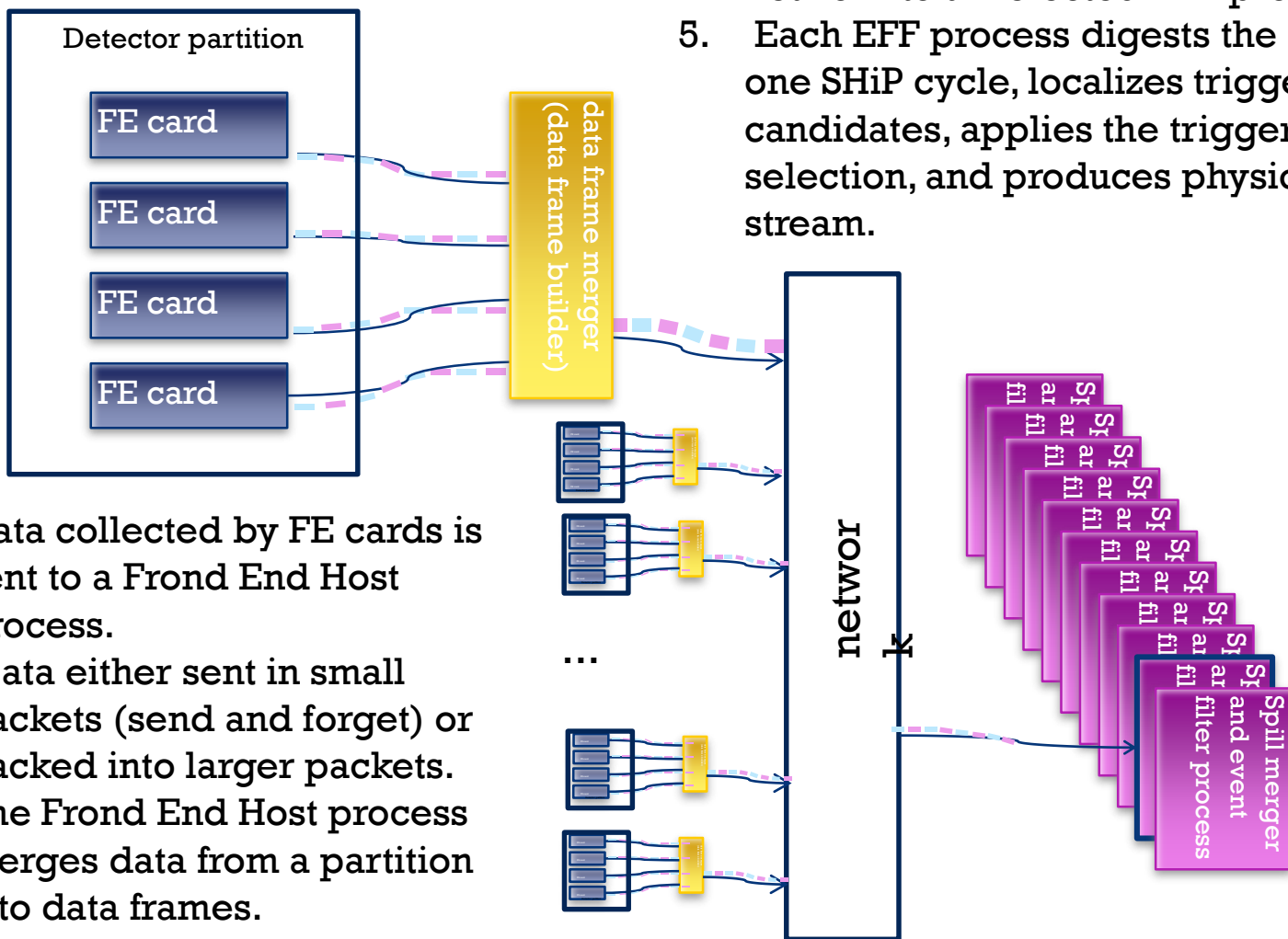
- Front End (FE) electronics producing data
- Timing controller (TFC)
- Front End Host processes (FEH)
- Event Filter processes (EFF)
- Switched network, PCs, storage

■ Notes:

- FE interface directly with a dedicated host computer (no network switch).
- The FEH pack the data frames for the EFF.
- EFF and FEH processes may share the CPU.
- SHiP data is processed on an 'elected' node on a per SHiP cycle basis.
 - An SPS extraction spill is always fully contained in a SHiP cycle.



+ Data Flow (logical view)



1. Data collected by FE cards is sent to a Front End Host process.
2. Data either sent in small packets (send and forget) or packed into larger packets.
3. The Front End Host process merges data from a partition into data frames.

4. Data from all partitions sent over the network to an 'elected EFF' process.
5. Each EFF process digests the data for one SHiP cycle, localizes trigger candidates, applies the trigger selection, and produces physics output stream.



From Architecture to Design

- In order to be able to design the TDAQ system there are still many areas for which requirements need to be specified
 - Number of FE cards and links
 - Expected data sizes (mean and peak)
 - ...
- Another important ingredient to the design is the definition of the interface to the FE cards
- We started evaluating design options in two areas
 - Backend data flow
 - Interfaces to FE



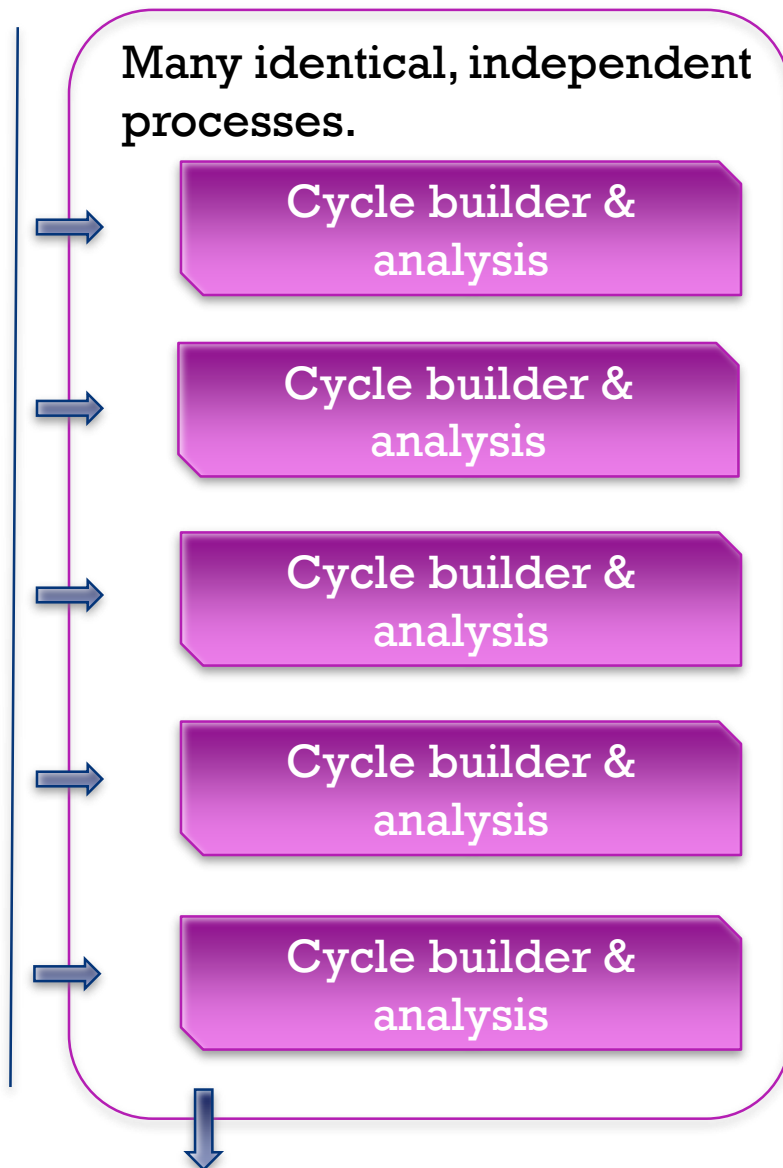
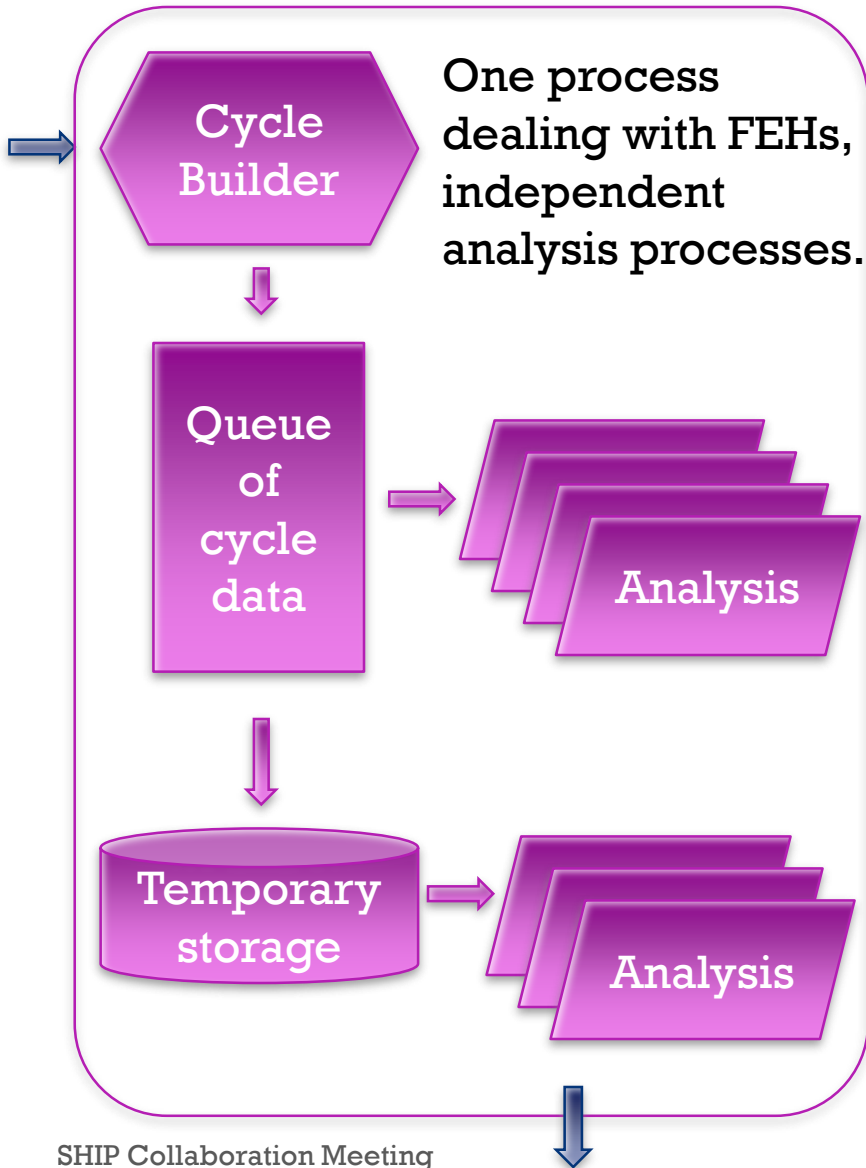
Assignment of EFF for cycle data

- EFF processes receive data corresponding to a full cycle
 - Processing done on the fly, or
 - Temporary data storage, for multi level or staged processing.
- The FEHs need to know which is the best suited EFF to receive the data for a cycle
 - A data flow manager (possibly integrated with TFC) assigns cycles to EFF nodes and notifies the decision to the FEHs, or
 - A data flow manager (possibly integrated with TFC) assigns cycles to EFF nodes and notifies the chosen EFF node which will pull the data from the FEHs.
 - Algorithm to select best EFF will be a function of their available processing and storage capacity.





EFF internal organization



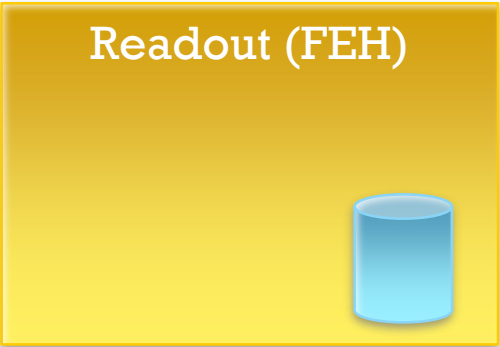


Defining the FE interfaces

- Define and agree on interfaces early on, allowing detector communities and DAQ to develop independently, towards a compatible solution
- Keep the FE as simple as possible and move complexity off-detector
- Make clear interfaces that do not pre-empt the freedom of profiting from latest technologies in the DAQ
 - If possible, limit the number of different physical interfaces to the FE
- In the next slides two approaches are presented
 - Feedback from the detector electronics experts appreciated



Interfaces to the Front End

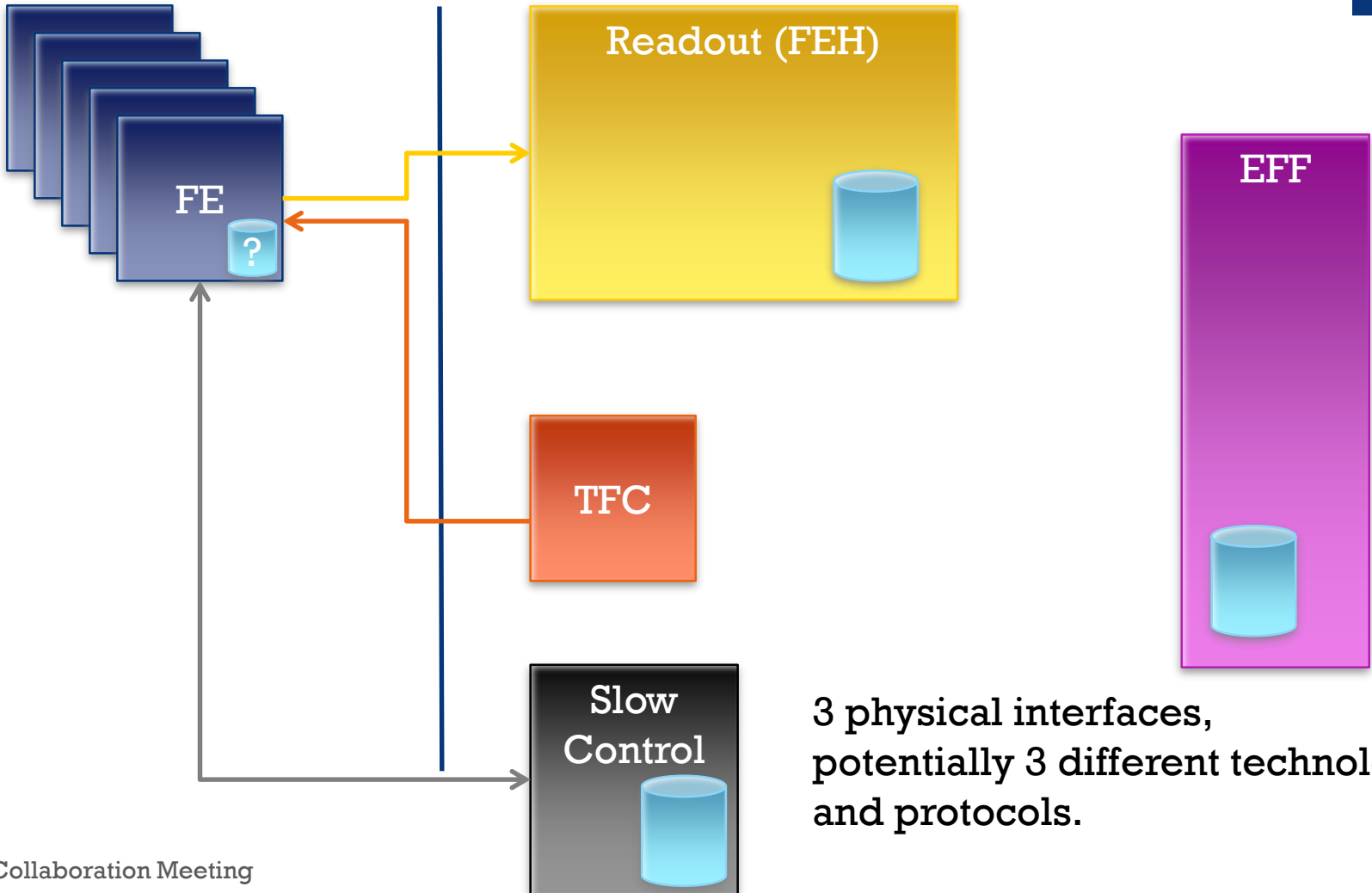


- Define early interfaces to:
- Readout
 - Timing, Fast Control
 - Slow control

- Choose as late as possible:
- Computing architecture
 - Storage architecture
 - Network topology and technology

+

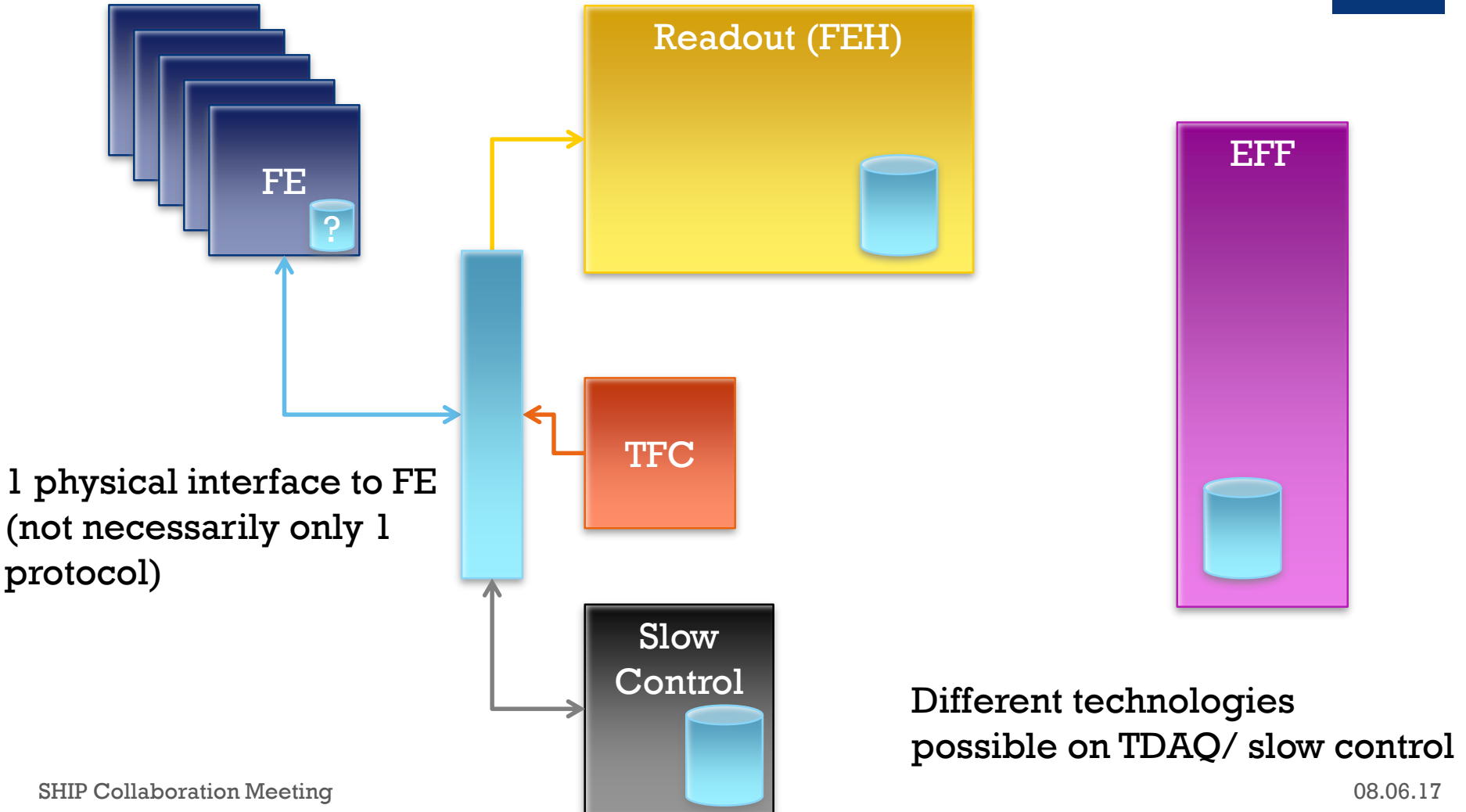
Option 1: “Traditional Approach”



3 physical interfaces,
potentially 3 different technologies
and protocols.

+

Option 2: “Integrated Approach”



+ What is and ?

- The box could be a set of servers hosting PCIe cards and a switching network.
 - Similar to the architecture being chosen by 3 out of 4 LHC experiments for their upgrades.
- The bidirectional protocol to/from the FE may be GBT
 - Alternatives may be considered, but GBT ensures synchronicity for the timing signals distribution and has implementations for Altera and Xilinx supported long-term (LHC experiments).

ATLAS



LHCb

+ Comparing Options



Option 1

- No coherence required for timing distribution, data readout, slow control
- Possible to choose the simplest technology for each
- No need for an intermediate HW layer

Option 2

- Agreement on a single physical interface/protocol(s) with FE developers
- Allow for max flexibility on technologies and topology of DAQ
- Though not mandatory for SHiP, use a solution that can be applied at CERN to many experiments in radiation environments.

Are both options feasible from a FE point of view?

+ Summary and outlook

- The overall TDAQ architecture has been defined and documented in note: : <http://cds.cern.ch/record/2162870>
- Major input still needed from detectors to be able to start designing a TDAQ system
 - Number of links, data sizes, expected data rates, ...
- In the meantime TDAQ design options are being evaluated
 - Back-end data flow and EFF internal organization
 - Interfaces to the FE
- In parallel, effort is being put into simulating the TDAQ
- Feed-back on options for defining the FE interfaces is very welcome