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High-speed concentration of sorted data streams for HEP experiments

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Presented paper describes the data stream sorting and merging architecture, fitting triggerless HEP experiments.

The presented architecture is implemented in FPGA and is expected to merge multiple streams of coarsely sorted data with single output stream throughput of up to 320 Mwords/s.

In triggerless HEP experiments multiple detectors record "continuous" stream of small (i.e., 32 bit) data samples and send them in a sequence to hardware data concentrator, which conveys them over high-speed links to software data processing units. To allow efficient splitting the data into sets containing events from the required time period, the concentrated data streams should be sorted.

The paper starts with the presentation of stream merging principles and description of FPGA implementation based on binary mergers. The binary merger picks single (older) data sample from two input FIFOs, used as stream buffers. The binary merger requires strictly sorted input streams, while certain detectors may provide only coarsely sorted data stream, (meaning that some samples are out of order, but generally the sample timestamp is increasing). Therefore, the initial sorting is needed. Additionally, binary mergers require the clock frequency equal or higher than the expected data throughput. That creates the hardware-dependent, unavoidable limitation of their usability for very high data rates.The output data rate limitation may be increased by a factor of two, by the newly proposed parallelized binary merger.

The introduced merger picks two oldest data samples from two double-width FIFOs and stores them in the output double-width FIFO, reducing the required clock frequency to a half of the data throughput.

Primary authors: GUMINSKI, Marek; Dr ZABOLOTNY, Wojciech (University of Warsaw (PL)); POZNIAK, Krzysztof (University of Warsaw (PL))

Presenter: GUMINSKI, Marek

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