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Timing optimisation in Overlap Muon Track Finder firmware

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OMTF is one of CMS trigger subsystems, tasked with analysing detector data on the boundar of barrel and endcap regions.
OMTF firmware is running on large, high-end FPGA; consuming more than 80% of FPGA resources. Main algorithm runs at 160 MHz, while data transmission subsystems run at 80, 160 or even 250 MHz. With a large FPGA utilisation it can be considered high frequency, which poses problems in achieving timing closure. Moreover, there are many clock-domain-crossing (CDC) paths; mainly on the slow control and pulser/readout paths. CDC paths must be manually constrained. Failure to achieve timing closure, or to properly constrain CDC paths, may result in data transmission errors or even functional failure.
OMTF firmware went through major timing optimisation in previous months, which should substantially improve timing results, which will increase confidence in firmware processing capabilities.

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