DAQ start of run

- Many software bugfixes during winter shutdown
- DHCmx's DDR memory controller bug fix, still to be applied to DHCsw
- Two DHCmx modules added as 0-level multiplexer instead of Slink multiplexers or in addition
  - MUX11, SrcID 920
    - MW2: 416, 417; MWPC : 448,449,450, 455; W45 : 271-274; SciFi : 208-215
  - MUX12, SrcID 921
    - SciFi : 147-159; DC5 : 971; DC4 : 259,260; Straws : 320-324;
  - Advantages
    - Reduce number of optical links
    - Equalize load to 1-level multiplexers
- Number of 0-level multiplexers will be extended
- Optimized dead-time : 4-3in30-10x25

DAQ start of run

- ECAL0 and ECAL2 run with reduced threshold
  - ECAL0 5 => 4 ADC counts , ECAL2 14 => 8
- Event size wo beam 50kB
- DAQ was running at 35kHz trigger rate
- DAQ runs stably
- Known issues :
  - Sometimes readout process gets slow and eventually crashes DAQ
  - TIGER scrambles data in a way that it leads to time out of DHCmx module