R&D on High Granularity HV/HR-CMOS Detectors for Future Experiments.[1]

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Executive summary

The UK HEP community has a strong international track record on the development of CMOS Monolithic Active Pixel Sensors (MAPS) that offer small pixel size and low mass and of planar silicon sensors that meet the most stringent requirements on radiation tolerance and fast timing. Recent advances in MAPS technology (HV/HR-CMOS) have shown great promise towards meeting HEP requirements for high-radiation tolerance, fast collection times, fast timing, small pixel size, high position resolution, high readout rate, low material budget, low power and affordability for large areas. There is a growing consensus that HV/HR CMOS MAPS will become the technology of choice for future HEP vertex, tracking and digital calorimetry detectors over the course of the next 10 years. Application of this technology will enable or extend the reach of future physics experiments and UK groups believe that now is an optimal time to invest in this technology. The leadership UK groups have established in silicon sensor technology places the UK in an excellent position to fully exploit the opportunities presented by the technology.

For the development of CMOS MAPS technology, comparison with international activities shows that key to a successful R&D programme is long-term continuity of funding. This is required to enable regular submissions of prototype designs for evaluation; to develop lasting relationships with foundries (accessing their expertise and commercially-restricted information); to establish a core team of designers exclusively engaged in this technology and to train the next generation of experts. The key elements of the proposal are therefore

- to encourage STFC to adopt a long-term oriented approach to strategic technology R&D areas and identify the R&D towards applications of HV/HR CMOS technology as (one of its) strategic technology priorities,
- for UK groups to create a national HV/HR CMOS R&D consortium that, working closely with international partners, will develop applications of this technology in the near future and carry out the required R&D to meet the most challenging performance requirements of HEP applications in the long-term future,
- for UK groups to prepare a bid requesting a sustained funding line that would establish a core team of designers in the UK and allow for the regular submission of prototypes.

The technology advances expected to be achieved are of interest to other STFC areas such as the Diamond Light Source, and to application areas which can benefit from STFC technology developments. The proposed strategic approach to the development of HV/HR CMOS sensors, could also serve as a model for the development of other

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STFC long-term technology priorities.

Introduction

UK groups have long held a strong international lead in the development of silicon sensors and in the construction of silicon detector systems for tracking applications in particle physics. Sensor development for the LHC in particular saw substantial improvements in the capability of planar silicon sensors to sustain very high radiation levels and to allow operation at high rates. The baseline silicon technology for much of the silicon vertex detectors and the tracker for the High Luminosity LHC (HL-LHC) is n-in-p sensor technology originally proposed and to a large degree developed by UK researchers, working with UK industry.

The UK also took an early lead on the development of more highly integrated silicon technology developing charged particle detectors first in CCD and later in CMOS technology. Such technology is already the preferred solution in experimental environments where the material budget is more critical than requirements on radiation tolerance or rate performance. Recent developments in CMOS sensor technology appear to be overcoming the limitations in radiation tolerance and rate capability that traditionally limited the application of this technology. This opens the door to a much wider range of experiments. Many experts in the field now foresee that, with the proper investment, further developments in novel CMOS technology will result in new sensor concepts that will largely replace planar silicon technology in the near future.

An extensive programme driving CMOS technology to address the challenging radiation dose and rate capability performance requirements, previously beyond the scope for this type of technology, will open the door to detector systems with a higher level of integration of analogue and digital processing that can be used in a much wider range of experiments than today. Since current costs for mass-produced microelectronics wafers can be as low as 0.3€/cm^2 (although CMOS wafers for imaging applications such as mobile phones are somewhat higher), CMOS technology has already supplanted CCDs in the $38 billion image sensor market (IC insight report). By using fully commercial technology, CMOS is substantially more cost effective than traditional detector systems based around bespoke planar silicon sensors. This provides scope for large area, low mass detectors, pixel tracking at large radii, and high granularity calorimetry in both lepton and hadron collider environments.

Performance Drivers

CMOS Monolithic Active Pixel Sensors (MAPS) have long been in development for use in scientific instrumentation as a replacement for CCD technology. Cost, read-out speed and better radiation tolerance have been the primary drivers. Applications in particle physics included a long line of development targeting future e^+e^- facilities (doi:10.3390/s8085336) and more recently the successful implementation of MAPS technology for the two innermost layers of the STAR Heavy Flavour Tracker at RHIC (doi:10.1016/j.phpro.2015.05.067). This has led to 7 layers of MAPS based detectors being proposed by ALICE for its Inner Tracking System upgrade (doi: 10.1088/1748-0221/10/03/C03030).

Table 1 summarises some of the application areas where enhanced CMOS technologies can find use in future particle physics experiments and related areas. The table focusses on challenging performance aspects that can benefit from new developments in CMOS technology. This means that, in particular, those applications are listed for which a combination of the general benefits of CMOS technology with greater timing resolution or radiation-hardness would be beneficial. The table represents the different emphasis for different applications (requiring different optimisations) through the intensity of the background colour in each cell. More details on the performance drivers are given below along with some of the target parameters. Many of the particle physics performance drivers overlap with the requirements of CMOS technology in other areas of the STFC programme. Previous development work on CMOS MAPS on planar silicon technology benefitted applications in many areas, including astronomy (e.g. star tracking and Earth observation), nuclear physics (e.g. R3B Tracker or CBM@FAIR), light sources (XFEL, LCLS or DLS), medical imaging, hadron therapy, high-speed imaging, transmission electron microscopy and mass spectroscopy. The UK development of HV/HR CMOS, offering much improved performance in terms of speed and radiation tolerance in MAPS detectors, will open the door to improved applications in many of these areas, in particular in nuclear physics, hadron therapy and high speed imaging.

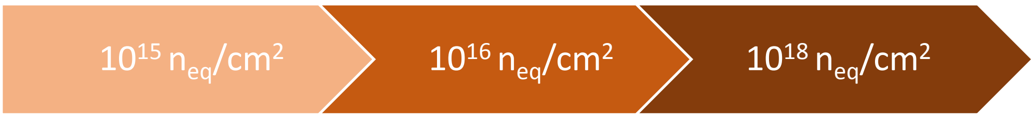
Technology Driver / Target Application	Pixel Size (Granularity)	Pixel Size (Resolution)	Radiation Hardness	Timing Resolution	Radiation Length	Collection Thinness	Large Area (Cost)	Low Power
HL-LHC Vertex			**Outer radii**					
HL-LHC & LHCb Phase 2 Tracker	**Position encoding**							
LHCb Phase 3 Vertex				**Vertex timing**				
Future hh Vertex								
Future hh Tracker								
Future hh HG ECAL	**Count hit pixels**	**Pre-shower cells smaller**				**Match to pitch**		
Proton EDM								
Future e-h								
Nuclear Physics incl. HI & FAIR								
e^+e^- Vertex (ILC/circular)			**Higher for Circular**	**TS (ILC)**				
e^+e^- Vertex (CLIC)				**Time Stamp (TS)**				
e^+e^- Tracker (ILC/circular)				**TS (ILC)**				
e^+e^- Tracker (CLIC)				**Time Stamp (TS)**				
e^+e^- HG ECAL						**Match to pitch**		
cLVF rare muon decays (Mu3e)		**Scattering dominated**		**Vertex timing**				
Hadron Therapy	**$>10^{10}$ tracks/s**	**Scattering dominated**		**$>10^{10}$ tracks/s**				

Table 1 Performance drivers for different applications. Darker backgrounds indicate increased importance for each application.

Radiation tolerance

Since the start of silicon sensor developments for the LHC experiments, radiation tolerance has been a critical performance aspect. A large increase in the radiation dose that can be sustained whilst retaining an efficient sensor capability was achieved through a strong R&D programme led through the CERN RD50 collaboration with many UK researchers making leading contributions to this effort. In particular, the importance of establishing design-capability was recognised as being central to the success of the programme with UK physicists and design-engineers collaborating on the development of the mask-designs required for each photo-lithographic step.

Current MAPS technologies only target total ionising dose up to 700 krad and non-ionising energy loss up to 3×10^{10} $n_{eq}cm^{-2}$, so significantly enhanced radiation tolerance is needed to meet challenges going much beyond these values. Recent developments in CMOS sensor technology, deep well technology for automotive applications and the availability of CMOS on high resistivity substrates have opened the door to the development of CMOS sensors capable of surviving the extreme radiation levels expected at for example the HL-LHC or a future hadron collider facility.



Radiation Tolerance Requirements (current state-of-the–art, short-term and long-term R&D targets)

Time Resolution and High Rate Capability

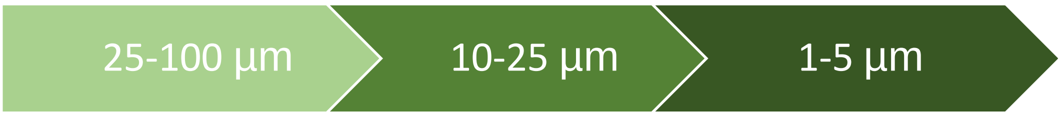
Good detection rate capability and radiation tolerance go hand-in-hand to a large degree, as the latter often relies on a fast signal collection to reduce the effects of charge trapping. An important handle along with spatial resolution to identify the common origin of particles is to have a very accurate measure of the timing of hits from charged particle tracks (HL-LHC, LHCb Phase 2, Mu3e Phase 2). In applications with time structures that give long trains of particle bunches interspersed with periods of no activity (ILC, CLIC, fixed target, synchro-cyclotrons for hadron therapy) buffering on-chip or in-pixel with an accurate time stamp can be employed, with full read-out being synchronised to the time period between the bunch trains. In other applications with continuous data taking, extremely large online data filtering is required, often requiring on-sensor intelligence combined with deep pipe-lines for data storage while global event trigger decisions are made.

Timing Resolution Requirements (current state-of-the–art, short-term and long-term R&D targets)

Pixel Granularity and Position Resolution

Track densities in the detector can drive different optimisations. In low occupancy environments, high resolution can be achieved with lower granularity detectors using hit clustering if the signal/noise is high enough. Moving to thinner detectors and, in higher occupancy environments, to CMOS devices that collect charge by drift rather than diffusion, a more direct correlation between pixel granularity and position resolution is expected. For electro-magnetic calorimetry applications, where the transverse shower width is considerably greater than the intrinsic pixel size, excessive off-detector data rates can be avoided by combining information from many pixels into a smaller number of cells (strip or pads). For example implementing logic that simply counts the number of pixels with minimum ionising particle (MIP) hits above threshold within the larger cell.

In high energy physics, many energy and precision frontier experiments now have to cope with higher rates of collision or decay events to probe extremely rare processes. Backgrounds from coincident events are resolved through high granularity detectors giving excellent vertex position resolution identifying which observed particles stem from a common vertex. The ability to place the first layer of detectors with excellent position resolution as near as possible to the interaction point is critical (HL-LHC GPDs, LHCb and LHC heavy ion, e^+e^-, future hh or proton EDM experiments).



Pixel Size Requirements (current state-of-the–art, short-term and long-term R&D targets)

Radiation Length and Collection Thinness

Multiple-scattering dominates the resolution for precision track fitting even to quite high momenta and for secondary vertex finding is a key limitation at all future facilities. Heavy ion, nuclear physics, rare muon decay experiments and ion therapy applications also operate in a multiple-scattering dominated regime. ALICE has demonstrated for the ITS that MAPS ladders can be built that achieve a total material contribution equivalent to less than 0.3% of a radiation length, whilst the Mu3e experiment proposes a smaller detector, in which vertex and tracking layers achieve approximately 0.1% of a radiation length. Thicknesses of the sensors down to 50µm can be achieved, beyond which mechanical supports, read-out bus-tapes and cooling services typically dominate. In many devices, the substrate thickness influences the signal, with even an increase of signal occurring with additional radiation dose (in a given range) due to changes in substrate effective doping. While more signal is always beneficial (with ~80e^-h^+ pairs per micron) there are some applications where too great a signal generating thickness can be problematic. The ideal space-point measurement for many applications is a voxel with the same dimensions along all three axes. This is particularly an issue where there are strongly inclined tracks or a uniform response to MIPs is required which is typical for some of the possible calorimeter applications or generally where a binary output is required to meet data transmission limitations.

Device Thickness (current state-of-the–art, short-term and long-term R&D targets)

Device Area (Cost) and Power

In particular in the general purpose detectors at particle colliders, the trackers, pre-showers and calorimeters require large area sensor planes from a few hundred m^2 up to potentially ten thousand m^2 in future large calorimeter applications. This drives a strong focus on cost reduction which is also vital for example for future medical applications to allow affordable systems to be developed for clinical use. While systems with trillions of pixels must be operable with tolerable total power consumption, there is also the issue of getting power in and out of the detector array. For compact arrays requiring very low multiple-scattering, low power is also mandatory if cooling is not to compromise the overall material budget of the detector system.

Detector Array Area (current state-of-the–art, short-term and long-term R&D targets)

CMOS technology: UK track record and roadmap

In a wide range of future experiments in particle physics, as identified above, significant benefits could be achieved with enhanced CMOS sensors with greater radiation-hardness and signal collection speed.

For near future applications, CMOS foundries offering the possibility of devices with significant sensitive depletion depths (HV/HR CMOS) should be targeted as good radiation hardness has already been demonstrated by the RD50 and ATLAS groups. UK groups have already, with international collaborators, submitted (or plan to submit) prototypes with several of these foundries (AMS, LFoundry and TowerJazz Panasonic), developing prototypes (CHESS and Pixel demonstrators) for the HL-LHC upgrades of the tracking and pixel detectors for the ATLAS Inner Tracker upgrade. LHCb requirements for a tracker in Phase Ib (LS3) have strong synergy with these. Building on our collaborations with international colleagues through RD50, the LHC programme and AIDA-2020 we expect to fast-track a limited number of reticule scale prototypes addressing in particular the performance requirement for the HL-LHC. A further (Phase 2, LS4) upgrade of the LHCb experiment could benefit from development work on these technologies as it seeks in particular a substantial improvement in the timing resolution (< 100 ps) of the vertex detector to aid the association of tracks to the correct collision vertex; such a device would be of interest across LHC experiments. ALICE is also considering a further upgrade to their pixel vertex detector, requiring much higher radiation tolerance than currently envisaged for the ITS. Outside LHC, there are excellent near-term opportunities in developing small trackers and vertex detectors using HR/HV CMOS for upcoming high precision experiments. Prospects include an alternative to straw trackers at g-2 Phase II and the construction of the outer layers of HV-CMOS pixel tracker for Mu3e (for which an SOI has been submitted).

Given that very long lead-times are needed for R&D aimed at meeting the severe requirements of proposed new colliders and fixed target facilities, there is a strong case for a sustained programme to start now. UK groups have already been involved and expect to continue to be involved in the development of CMOS sensors for both the tracking detectors and calorimeters of experiments at a possible future e^+e^- facility. If such a facility were approved there is strong potential for a UK lead in the sensor development for a large area pixel tracker, building on work with foundries and looking to exploit UK links with some of the larger producers of commercial CMOS devices with future large area arrays in mind. Work has begun on understanding the needs of future hadron colliders. The FCC-hh presents the greatest challenge with respect to radiation-hardness, speed and functionality.

A UK meeting on CMOS detectors for particle tracking discussed the state of affairs in this area of R&D and was attended by 54 participants representing 16 institutes from across the whole UK particle physics community. UK groups intend to submit a joint SoI to Science Board that would be followed by a bid, aiming to establish a UK consortium under the umbrella of which the R&D on these emerging technologies would be pursued and to secure a funding line that provides the required continuity to build and retain long term expertise. This would allow the UK to develop a comprehensive design-led strategy targeting both applications in the short term, for which the bulk of resources would come through the associated projects, as well as the most challenging performance aspects that need to be met in the longer future. It is felt that the key to a successful development program is long-term, consistent funding to enable regular submissions of prototype designs for evaluation, to develop lasting relationships with foundries to access their expertise and commercially-restricted information, and to establish a core team of designers exclusively engaged in this technology. These ingredients would provide the backbone of a programme that addresses applications for near and long term future projects. Funding for training and PhD programmes would be highly desirable as the development of these skills in the youngest members of our community is central to the ambitions of this programme.