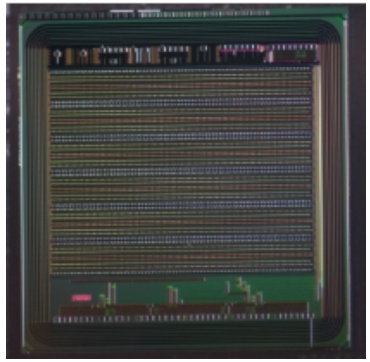
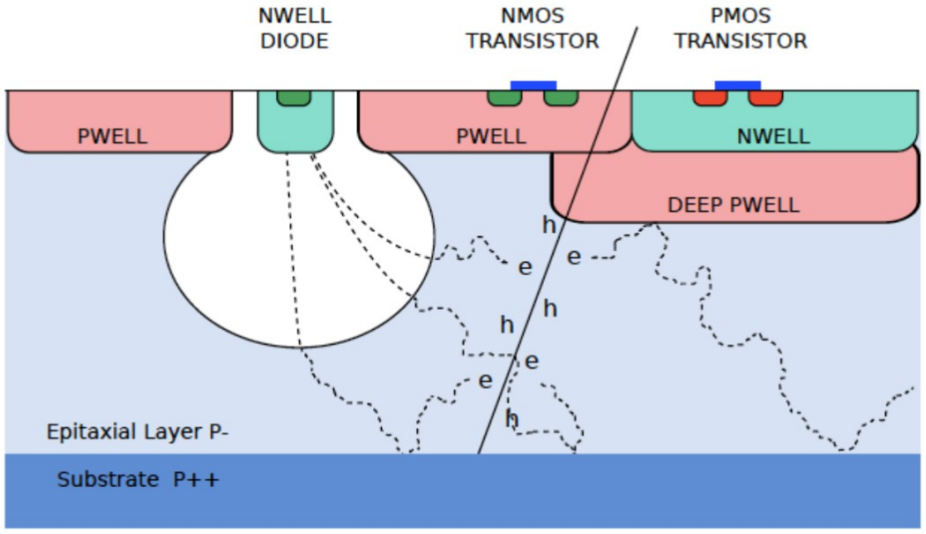
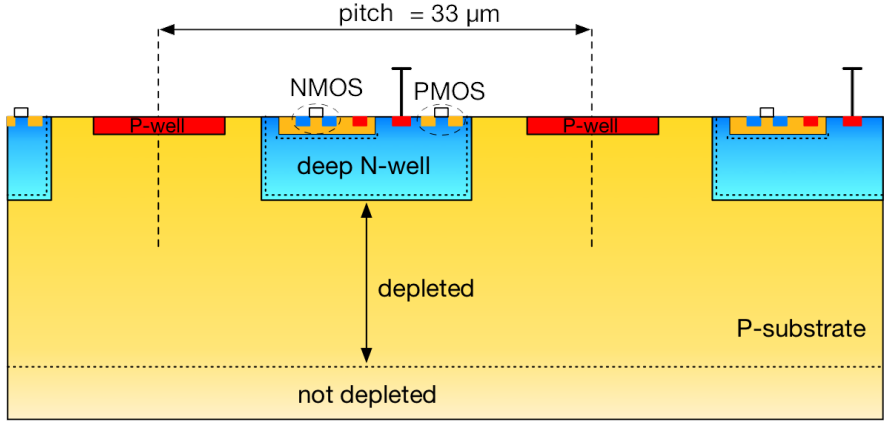
Advances in Radiation-Hard Monolithic Pixel Detectors

Technology Overview





Schematic cross-section of CMOS pixel sensor
(*ALICE ITS Upgrade TDR*)

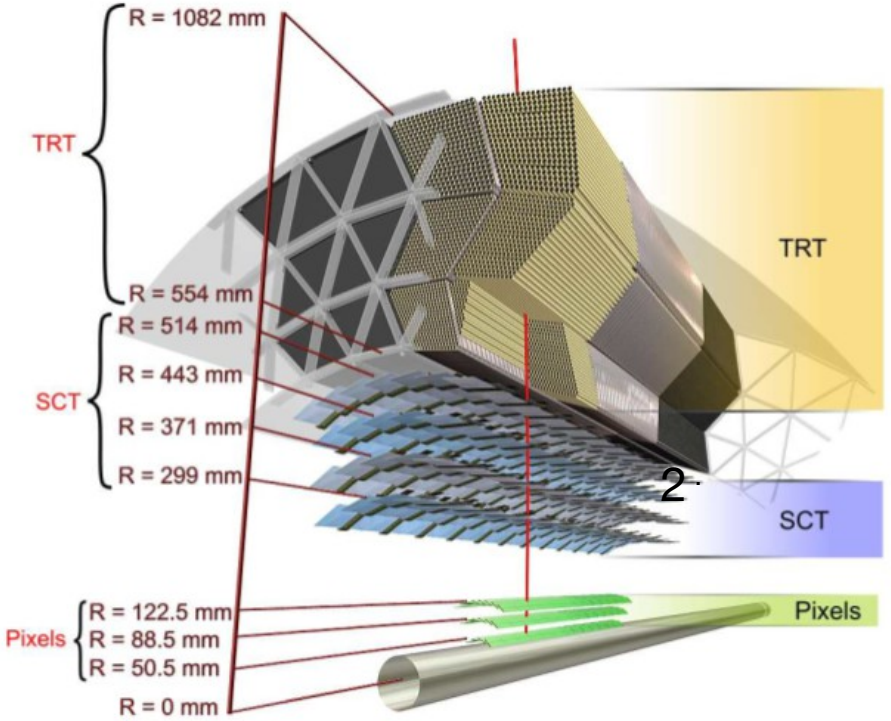


What this presentation is about

- Potentially, not everyone already has a background in radiation-hard CMOS detectors
- Therefore: briefly recall
  - potential radiation environments to be endured
  - the differences between “classical” tracking detectors and CMOS detectors
  - advantages of CMOS detectors – in particular if monolithic
  - branches of CMOS/terminology:
    - HV-CMOS
    - HR-CMOS
    - DMAPS
    - fill factors
  - radiation tolerance and peculiarities of CMOS detectors

One example: ATLAS HL-LHC Upgrade

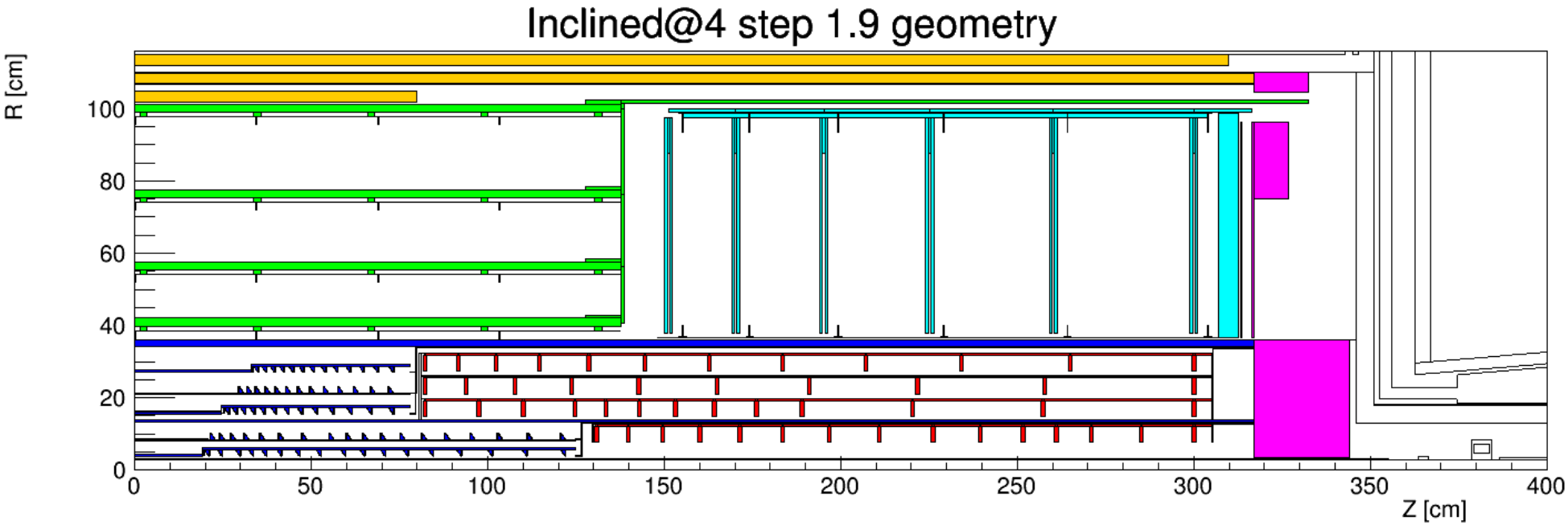
- Main challenges:
  - occupancy
  - radiation damage
  - data rate/trigger rate
- Components needing upgrades:
  - TRT
    - occupancy-limited beyond about 10^{34} cm^{-2} s^{-1} (40% occ.@ inner radii)
      → replace by all-silicon inner tracker



  - SCT
    - radiation damage limited (p-in-n sensors collect holes → n-in-p to collect e-)
    - occupancy limited (long strips → replace inner layers by short strips)
  - Pixel
    - data rate limited (inefficiency expected in b-layer above $3 \cdot 10^{34}$ cm^{-2} s^{-1})
      → replace with new readout chip
    - better resolution for pile-up rejection

How to replace? ITK

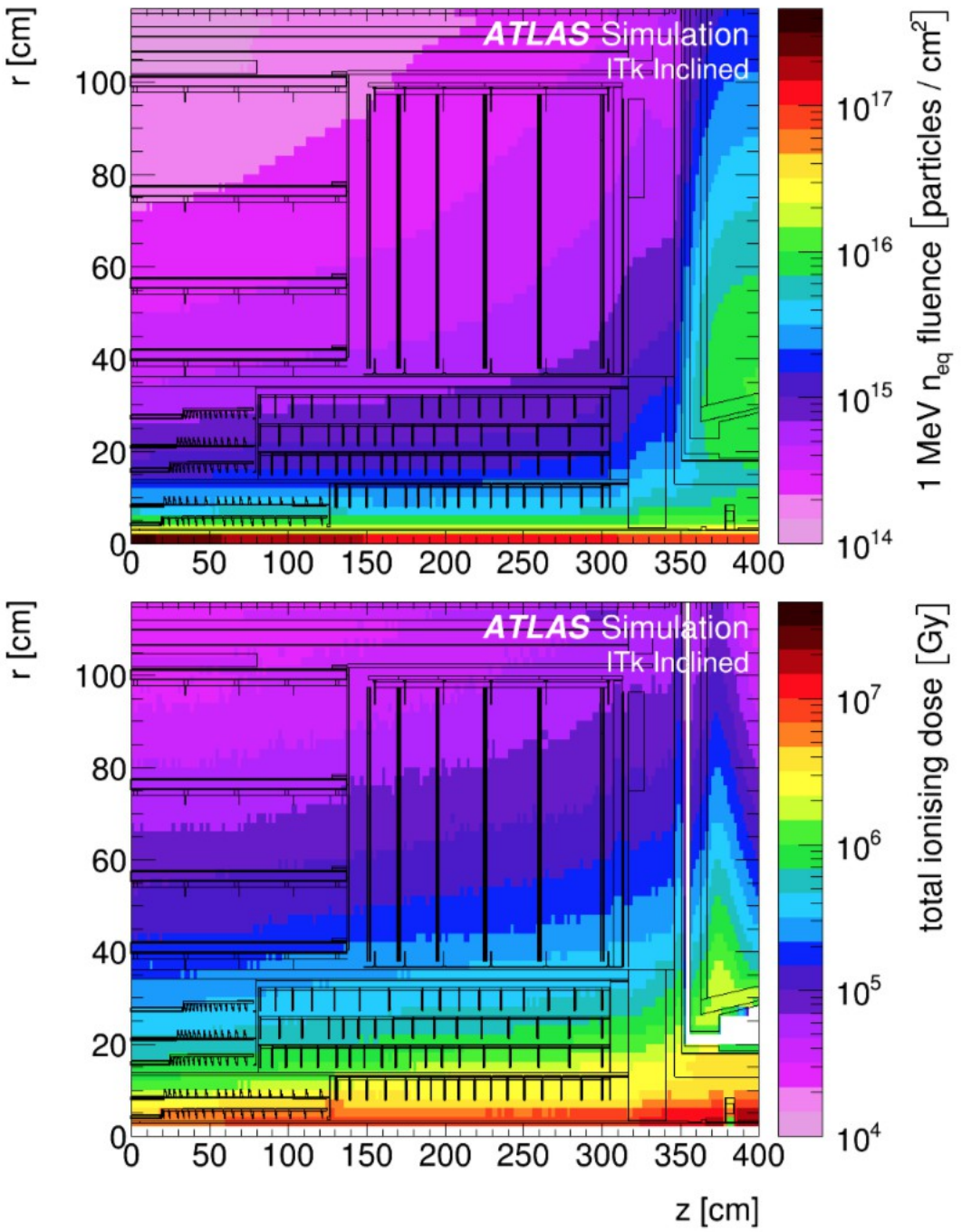
- Favoured layout: “FullyInclined”
  - ~165 m^2 of silicon strips (short and long), up to 14 m^2 of pixels → cost!



Expected Radiation Damage

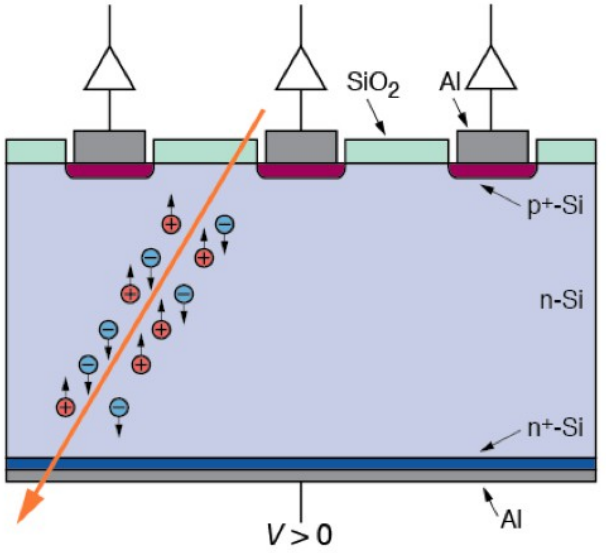
ITK strip TDR: ATLAS-TDR-025

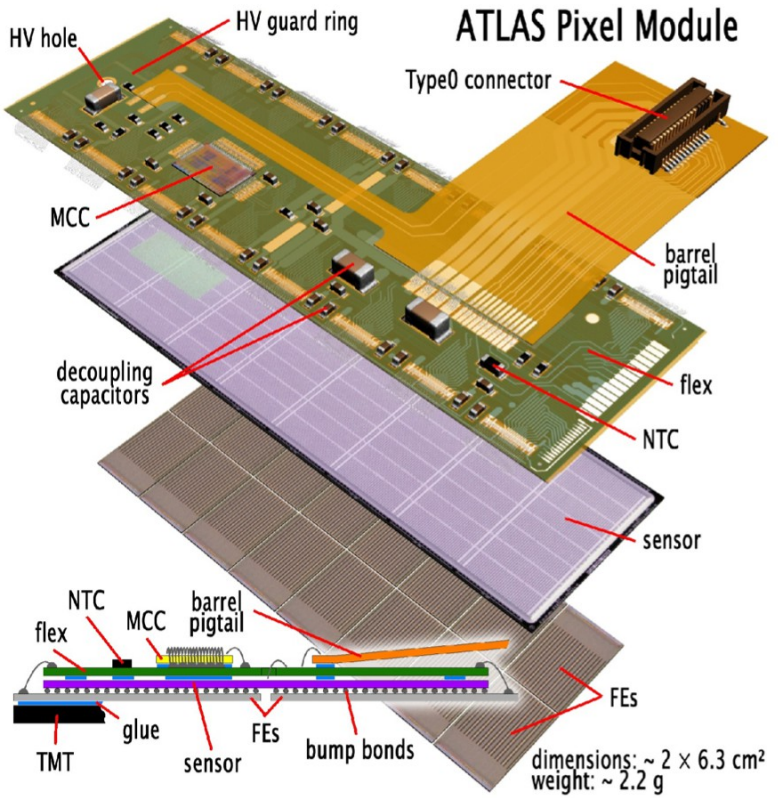
- integrated luminosity: 4000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 4 cm radius:
    - ~1.2 • 10^{16} n_{eq} cm^{-2}
    - ~950 MRad
    - (exchange after 2000 fb^{-1})
  - at 30 cm radius (outermost pixel)
    - ~2.2 · 10^{15} n_{eq} cm^{-2}
    - ~110 MRad
    - several m^2 of pixel detectors
  - strip region
    - up to ~1.5 · 10^{15} n_{eq} cm^{-2}
    - up to ~60 MRad
    - ~160 m^2 of silicon
- new ID sensors need to be more rad-hard and cheaper at the same time (more area to cover)

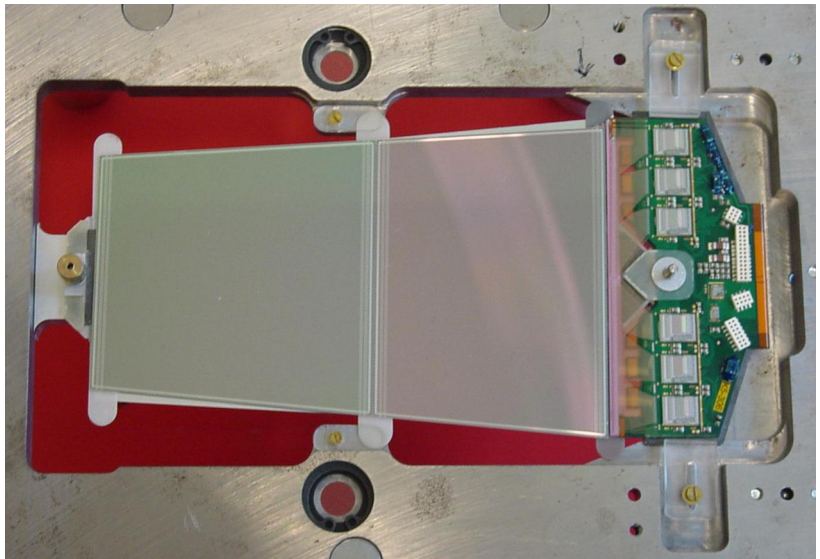


Classical tracking detectors

- Sensor volume and readout electronics separated
- one side is patterned, many strip/pixel electrodes
- apply electric field over bulk
- charges drift and induce signal on electrodes
- small signal, needs amplification
  - dedicated readout ASICs
  - connection with sensors via wirebonds (strips) or bump-bonding (pixels) → modules

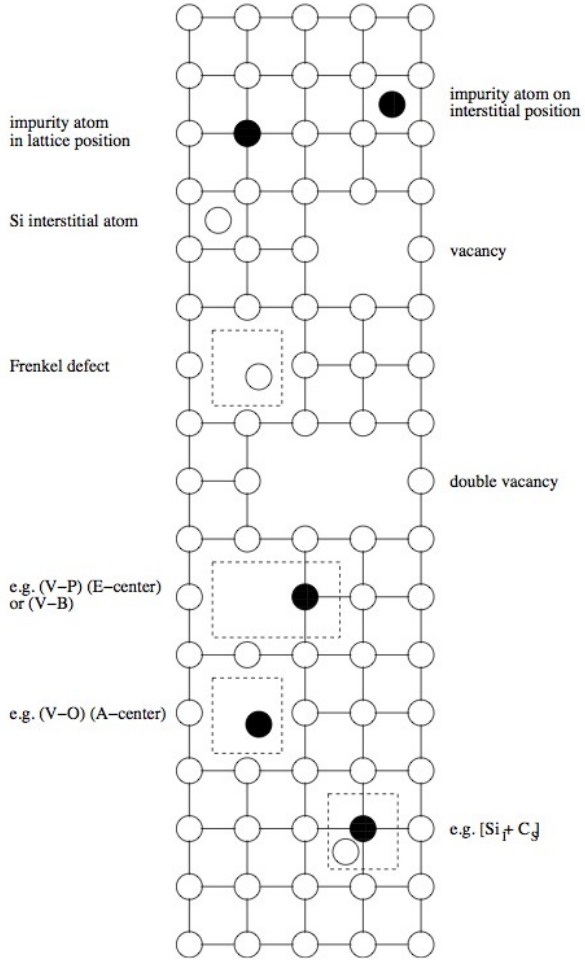






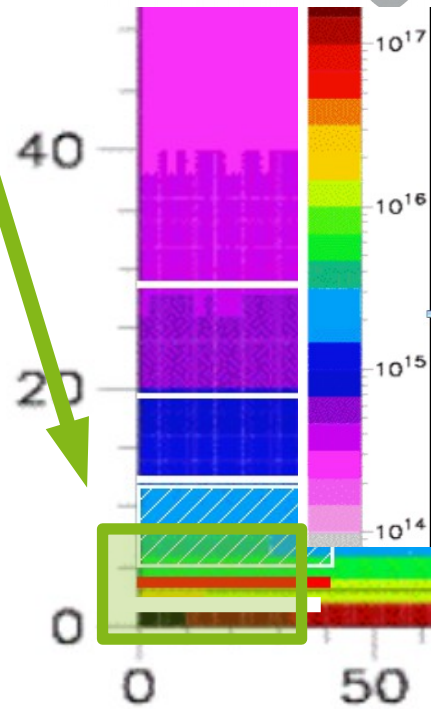
Silicon sensors and radiation damage

- Very briefy: The silicon crystal gets damaged by radiation – lattice atoms get moved around...
- There are 3 different effects all caused by radiation-induced damage to the crystal lattice:
  - charge-carrier trapping (main effect at high fluences)
    - localised trapping centers
    - thermal de-trapping timescale much longer than charge collection time
    - loss of induced charge → reduction of signal
  - leakage current
    - thermal generation of charge carriers → more noise → more cooling required
  - change of N_{eff}/V_{dep} (main effect at low fluences)
    - the material usually behaves effectively more “p-type” which leads to increasing full depletion voltages → higher bias voltages
- The usual unit for radiation damage is the particle fluence normalised to 1-MeV-equivalent neutrons
- Also Total Ionising Dose (TID) is relevant (oxide charges, electronics)

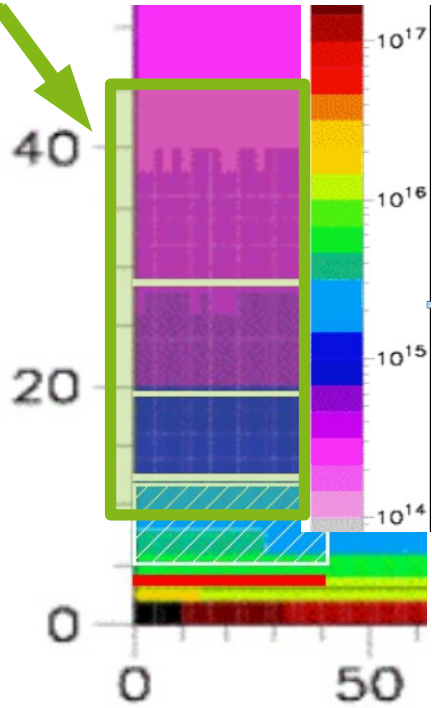


Pixel radii@HL-LHC: Different regimes

- Inner layers
  - ~$1 \cdot 10^{16}$ n_{eq}/cm^2
  - Trapping becoming the dominant effect
  - data indicates not a real issue for hybrid detectors with thinned sensors
  - comparatively small area – cost not dominant requirement
  - might profit from smaller pixel sizes – limited by hybridisation



- Outer layers
  - Rad-hardness up to $2 \cdot 10^{15}$ n_{eq}/cm^2 at 600V bias voltage was already established for current ATLAS Pixel Detector
    - rad-hardness not an issue
  - But: Costs? 1.8 m^2 → ~10+ m^2
    - bump-bonding large fraction of the cost (1/3 to 1/2)
      - could be avoided by monolithic detectors

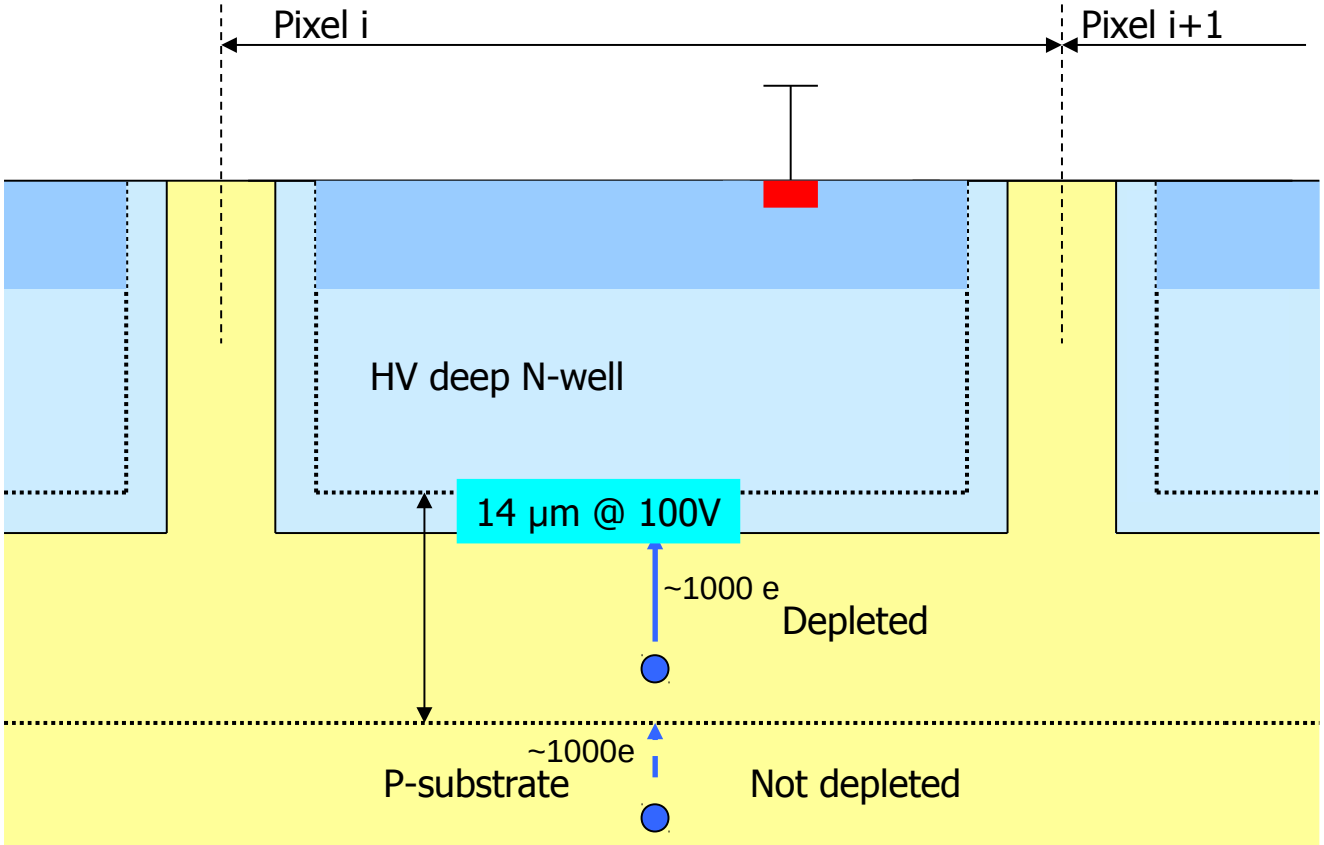


Improving cost and granularity

- Use
  - industrialised processes
  - large wafer sizes
  - cheap (or no) interconnection technologies
    - no interconnection would also help to reduce pixel size – CLIC development limited by bump-bonding requirement
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - application of **drift field** required for sufficient rad-hardness
  - 8” to 12” wafers
    - wafer thinning quite standard
- Basic requirement: Deep n-well (→ allows high(er) substrate bias)
  - existing in many processes
  - usually deepest in HV-CMOS → highest possible bias
  - also existing in specialised imaging processes → HR-CMOS

A CMOS sensor...

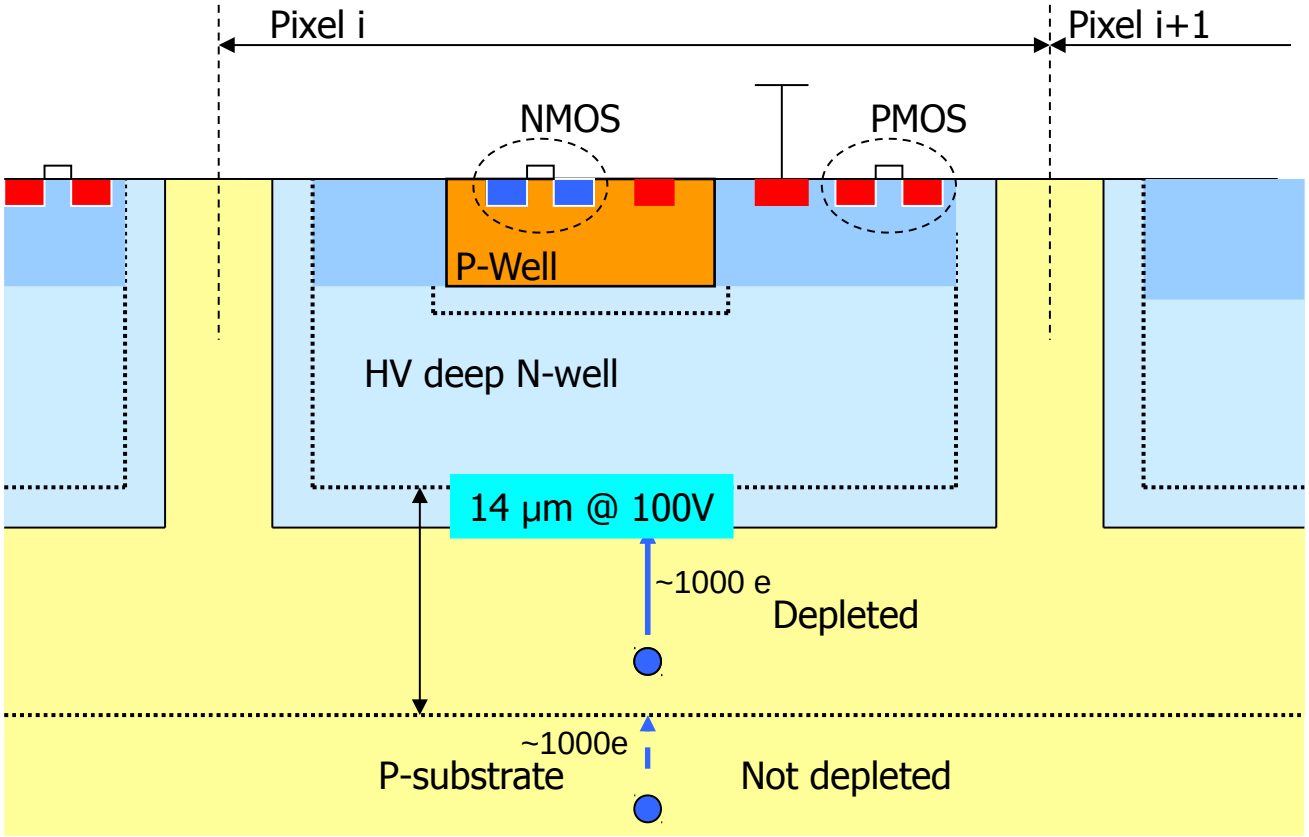
- is essentially a standard n-in-p sensor
- standard HV-CMOS: substrates ~20 Ohm*cm
  - depletion zone ~10-20 µm: signal in the order of 1-2ke$^-$
  - challenging for hybrid pixel readout electronics
- HR-CMOS: up to kOhm*cm
  - alternative vendor even for passive hybrid sensors



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

Add circuits: HV/HR-CMOS

- Choices: implementation of
  - only first amplifier stages – e.g. for CCPD sensors for CLIC
  - additional cuircuits: discriminators, impedance converters, logic, … - CCPD
  - all readout circuits: DMAPS (Depleted MAPS)



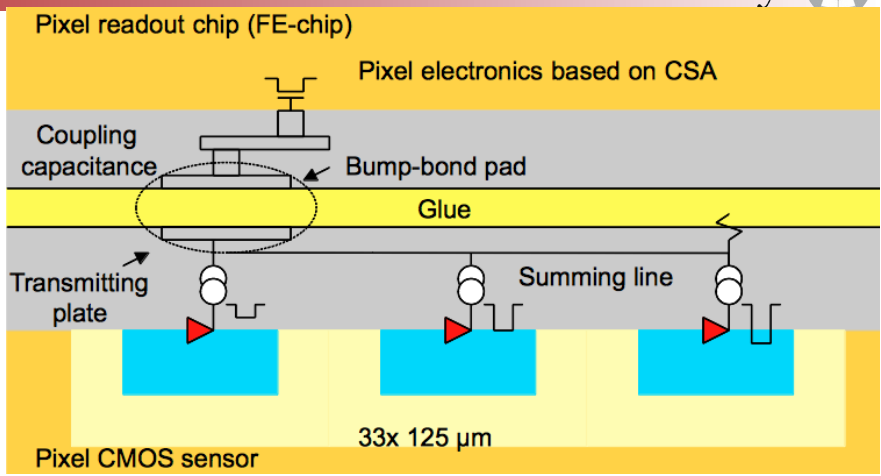
CMOS electronics placed inside the diode (inside the n-well)

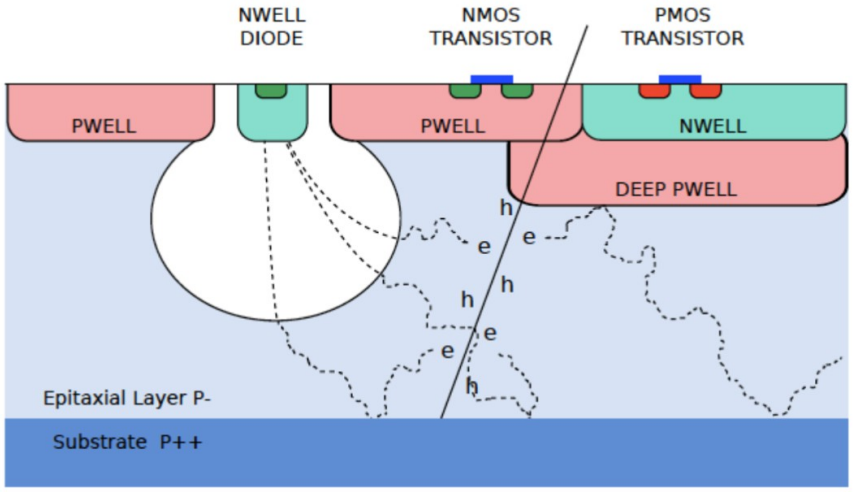
Nomenclature

- Amplification enables AC coupling (by gluing) of CMOS sensor and readout chip → Capacitively Coupled Pixel Detector (CCPD)

- Monolithic Active Pixel Sensors (MAPS, e.g. Mimosa) historically relied on diffusion for charge collection → too slow, not radiation-hard (cannot cope with trapping)

- Use Depleted MAPS (DMAPS) to collect charge by electric field





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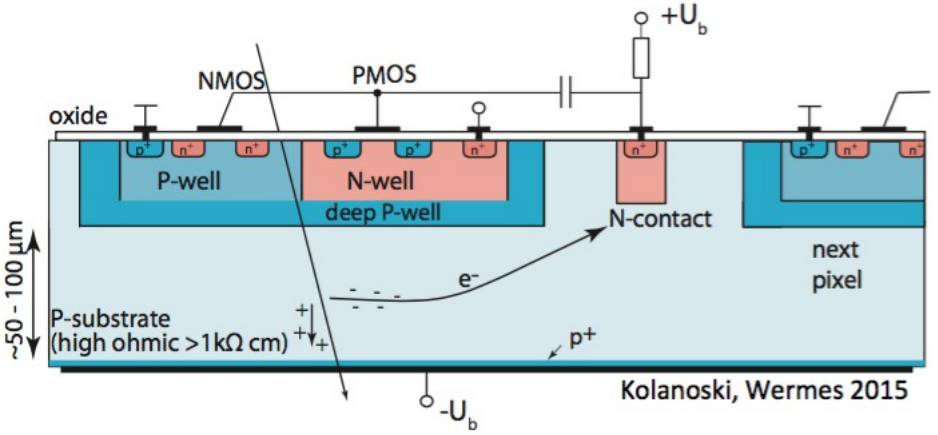
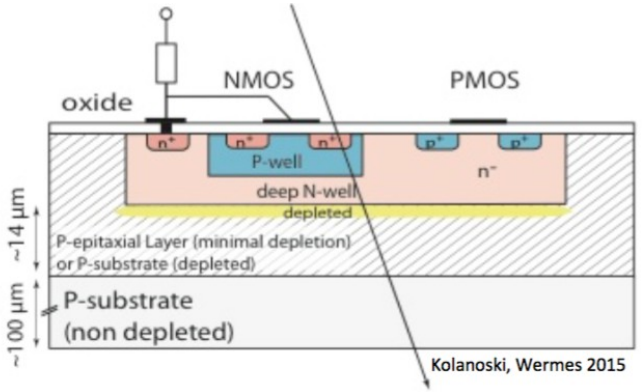
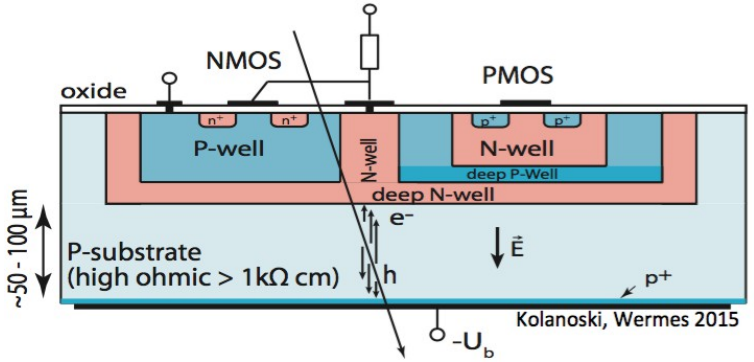


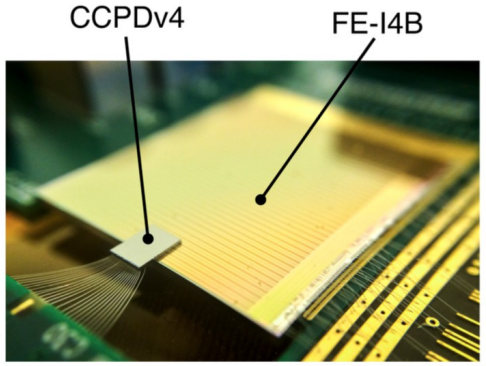
Nomenclature: several dimensions

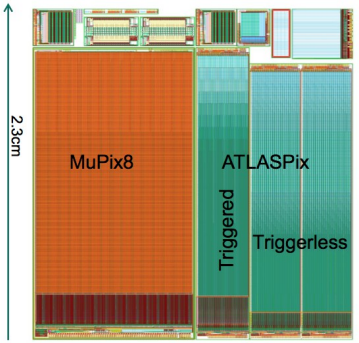
- HV vs. HR CMOS: low vs. high resistive substrate (historically!)



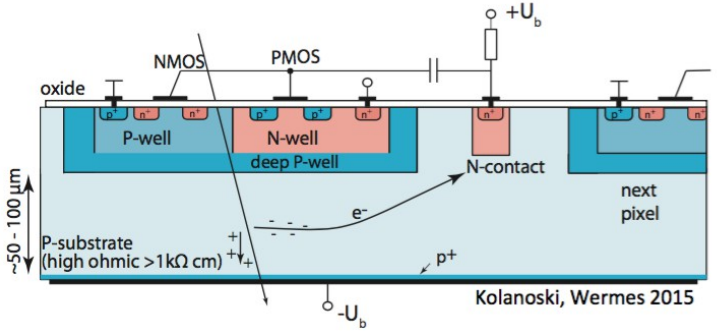


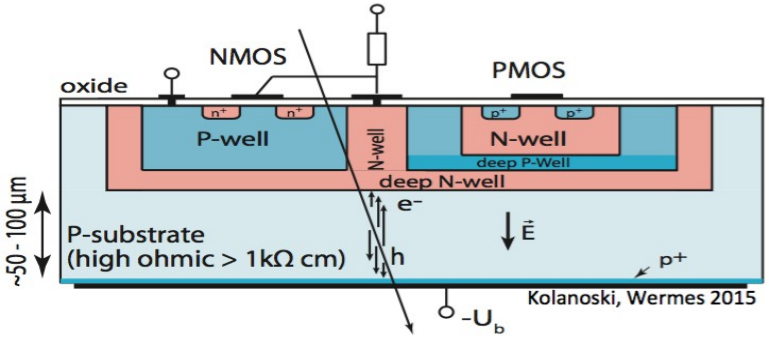
- CCPD vs. DMAPS: level of integration – separate readout chip or not





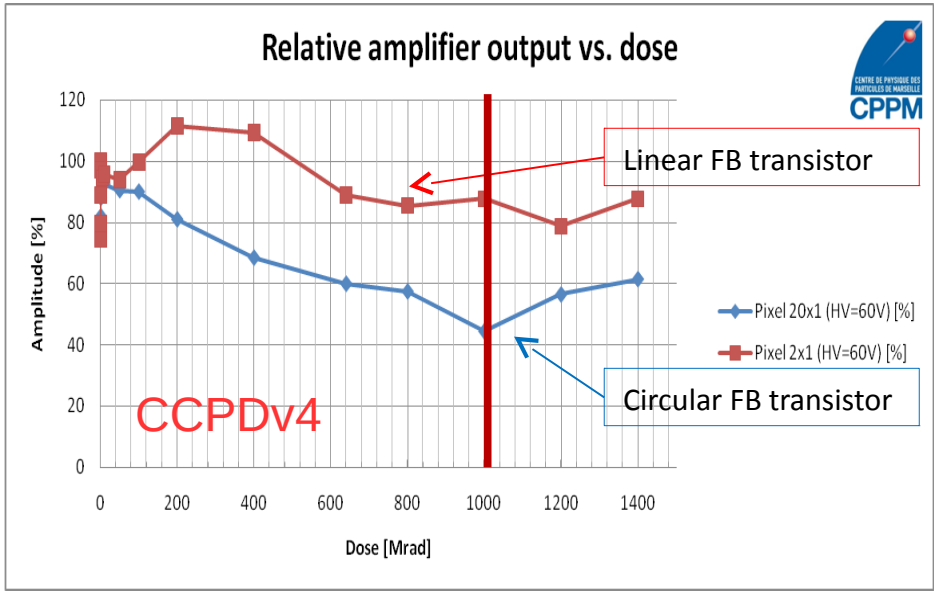
- small vs. large fill factor: size of collection electrode → input capacitance → noise

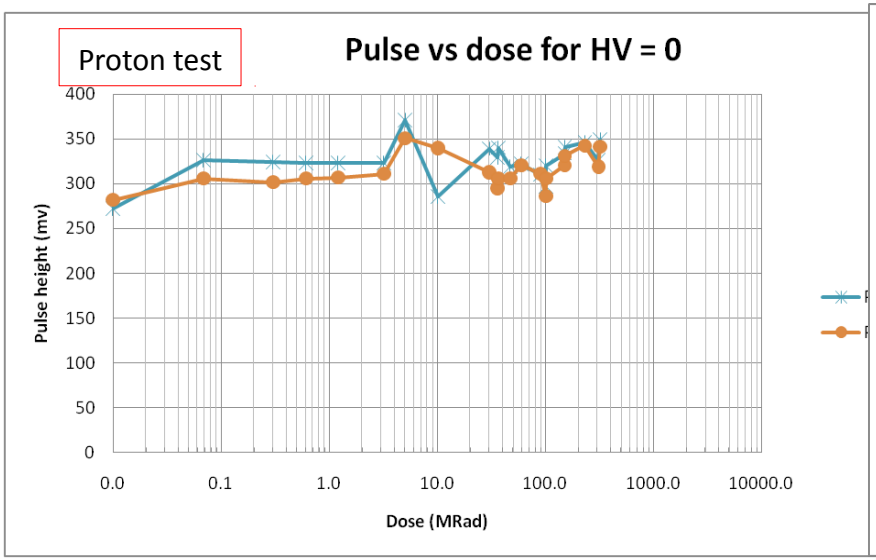


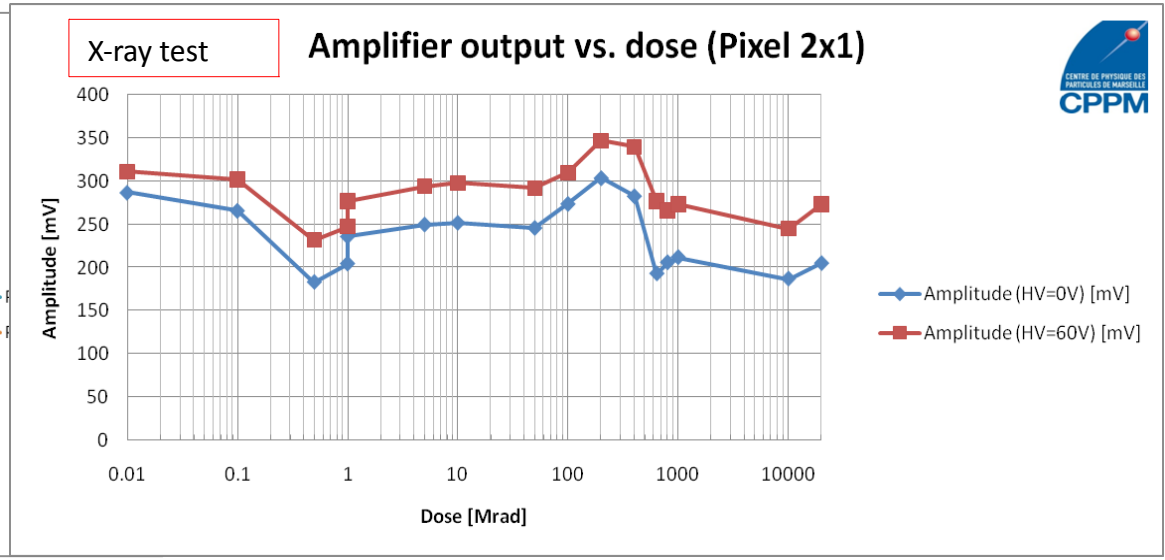


Irradiation effects: dose

- "Deep sub-micron" processes have potential to be rad-hard (thin oxide → oxide charges can tunnel)
- Still rad-hard design required
  - e.g. enclosed transistors
- Most visible analogue effect: changes in amplification
  - can be managed

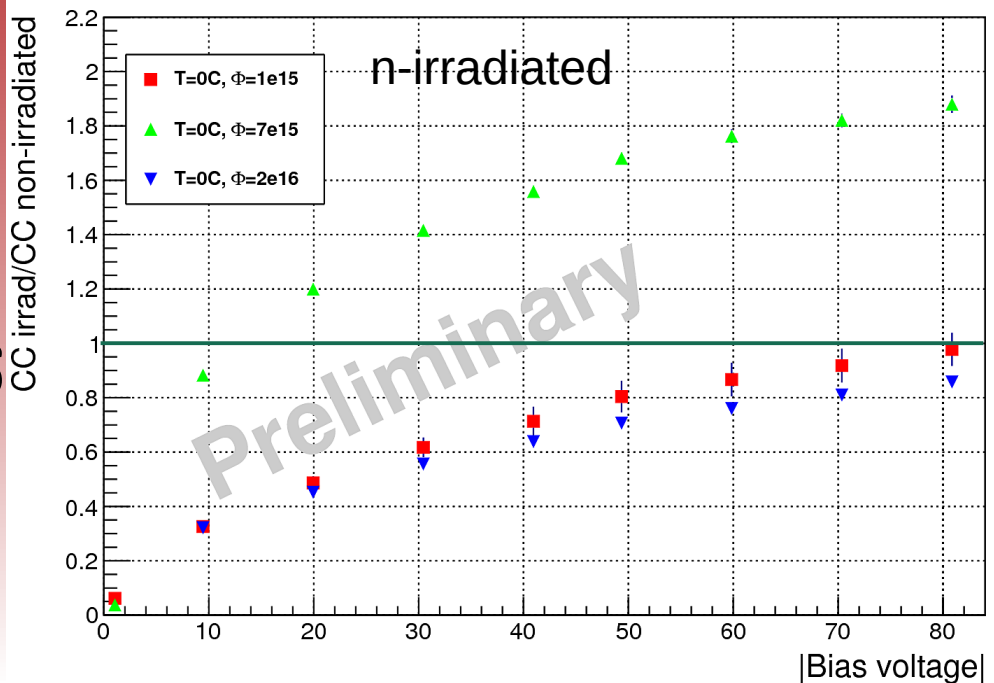


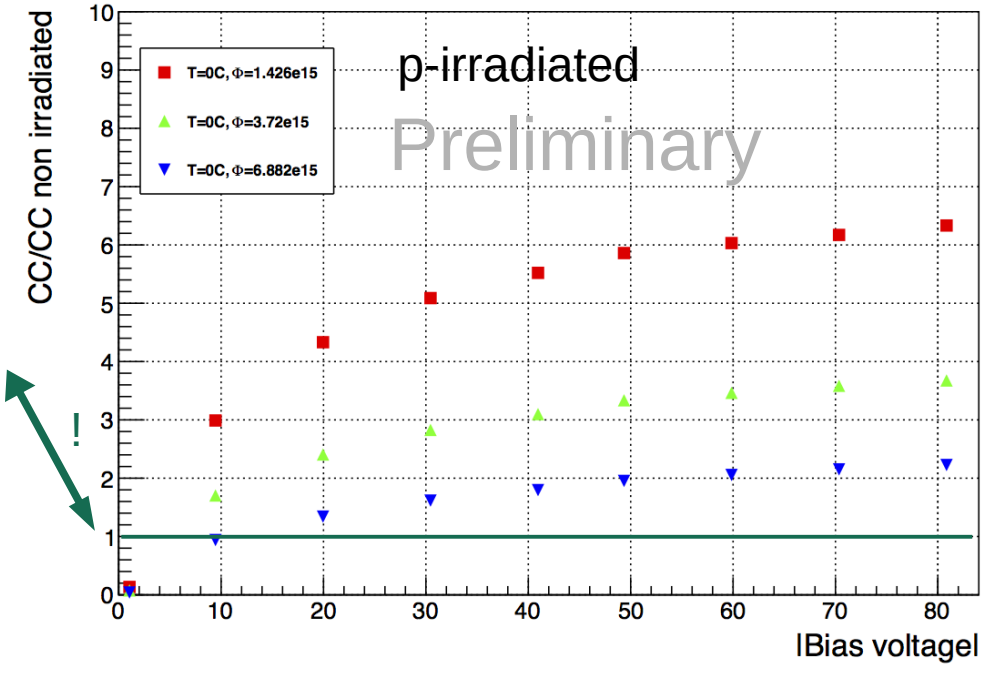




Irradiation effects: fluence

- Numerically, depletion depth for 10 Ohm*cm substrate is about 10 µm at 100V of bias
  - Classically, this should yield less than 800 electrons of collected charge
  - Yet ~1500-1900 e^- are observed before irradiation – large diffusion component?
- Characterised with Edge-TCT method
  - reduction for small fluences (< 5e14 neq/cm2) → loss of diffusion
  - increase (!) up to a factor 6 (!!) in collected charge for higher fluences
    - larger depleted zone thanks to acceptor removal, stronger for p-irradiation
    - note that even 2e16 neq/cm2 has reasonable CC, but cuircits might be an issue...

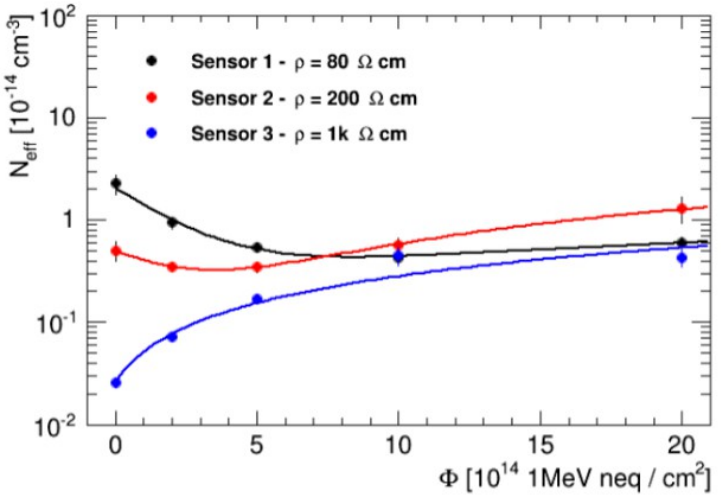




Recent trends

- Merging of HV and HR CMOS
  - Some HV-CMOS foundries offered to use higher resistive substrates while keeping the same (HV) process
    - high resitive substrates only loose resistivity
    - medium resistive substrates are “more stable”
      - might be an advantage as sensor behaviour changes less
  - Some HR-CMOS (imaging/CIS) processes allow the application of a (certain) bias voltage to the bulk

- Good CCPD results encouraged fully monolithic designs
  - several different processes, partially CCPD and monolithic on the same reticule for comparison
  - several different approaches



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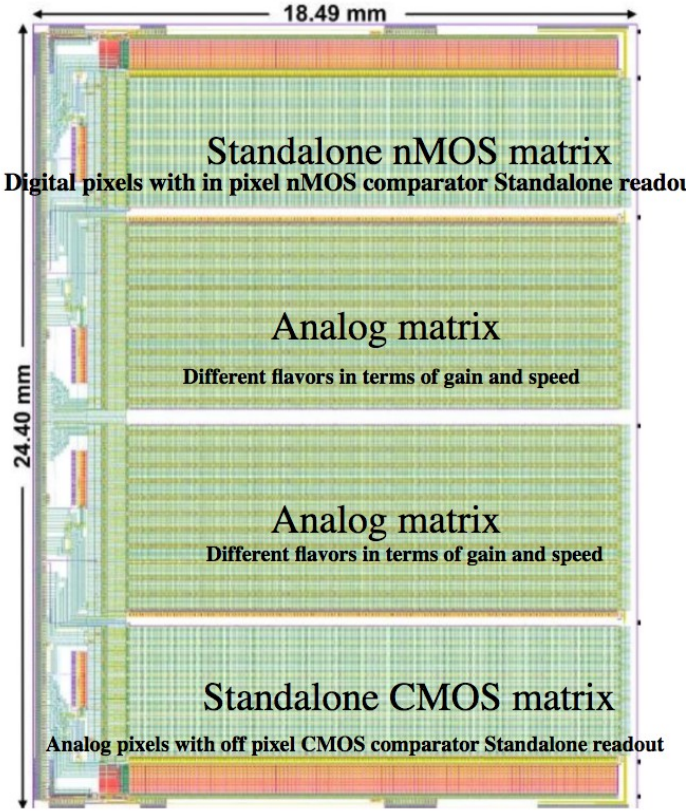


DMAPS types

Many processes more and more similar, main differences start to be design-related:

- simple pixel vs. complex pixel
  - the simple pixel approach has only (analogue) amplifier in-pixel, digital circuits are moved to periphery (à la LePix/MuPix) → less cross-talk, allows for small pixel, requires many traces to periphery and has potentially larger inactive edge area
  - complex pixel has comparator and potentially storage in-pixel → more potential for cross-talk, allows for bus to periphery
    - **many** different readout/bus architectures currently being explored!

- large fill factor vs. small fill factor
  - large fill factor has a large collection well → short drift distance, but large(r) capacitance
  - small fill factor has only a small collection well and hides other circuits behind deep p-wells → longer drift path, potential issues with lateral depletion, but less capacitance

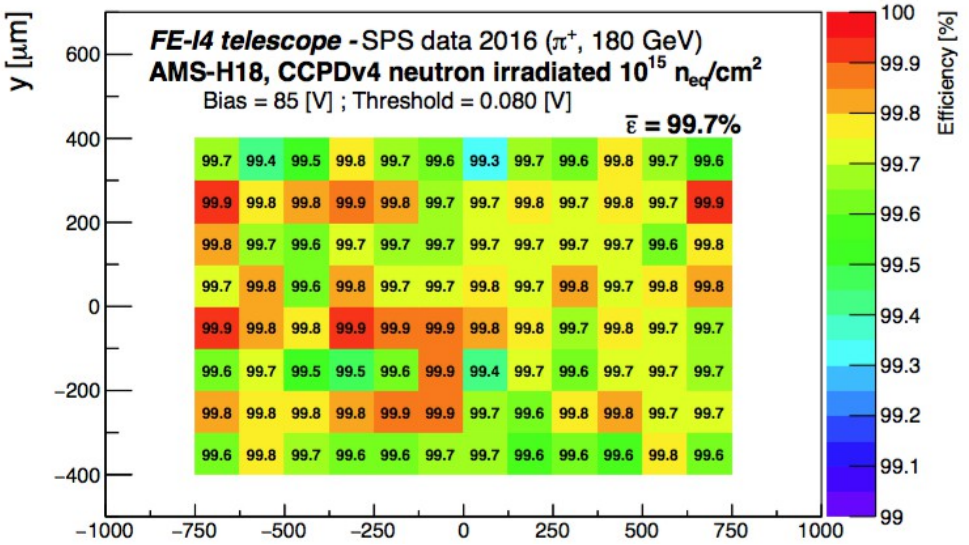
Summary

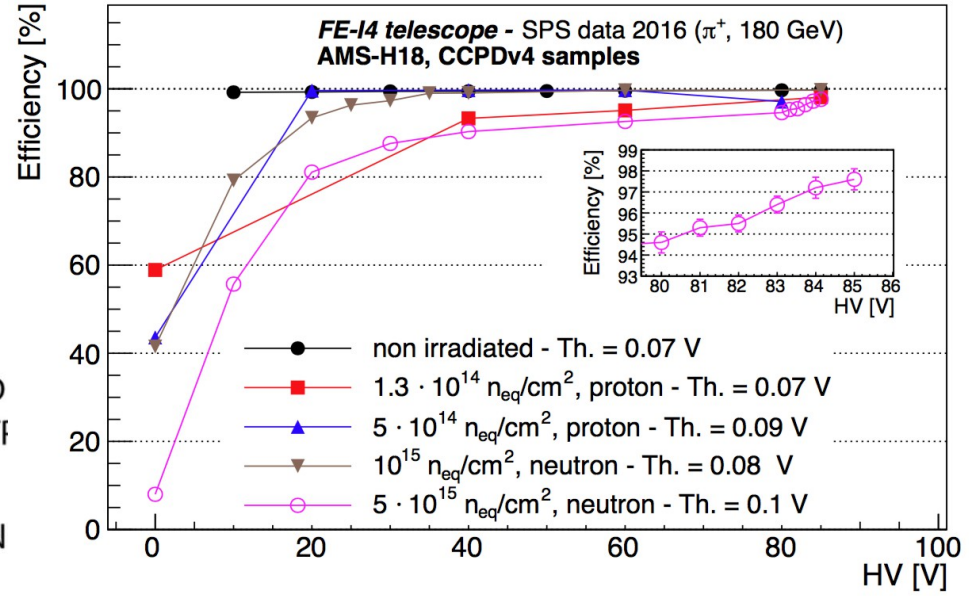
- CMOS detectors essentially n-in-p sensors that integrate the readout electronics on the same wafer
- Enabling technologies: deep n-wells, processing of high resistive wafers possible, triple/quadruple wells to shield circuits from depletion zone
- Several processes could be used and are actively explored – see later talks today
- Radiation hardness enabled thanks to drift (bias voltage), deep sub-micron process (thin oxide) and excellent threshold values achievable thanks to in-pixel amplifiers → low signal levels can be coped with
- Main differences:
  - applicable bias voltage (HV/HR-CMOS)
  - small/large fill factor → input capacitance, drift length, lateral depletion
  - comparator/circuitery in-pixel or in periphery
  - readout scheme – (a)synchronous, bus-based, column-drain, …
- Very active and fast-moving field!

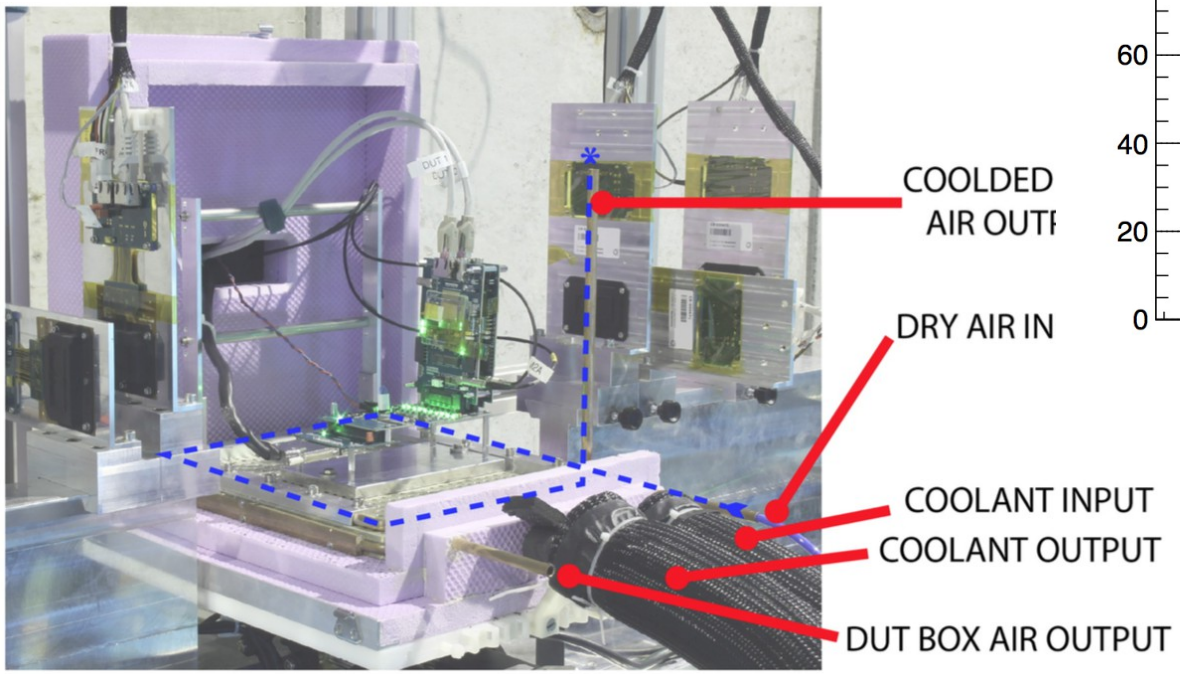
Lancaster University

Testbeam data

- CCPDv4 glued to FE-I4
- Very high efficiencies possible even after irradiation: >99.7% (!!)
- “valley of tears” at lower fluences
  - trapping kicks in
  - depletion depth not yet bigger
    → go for higher resistivity values







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