General HV-CMOS

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Outline

1. ATLAS

- H35DEMO
- ATLASpix

2. Mu3e

- MuPix

3. R&D

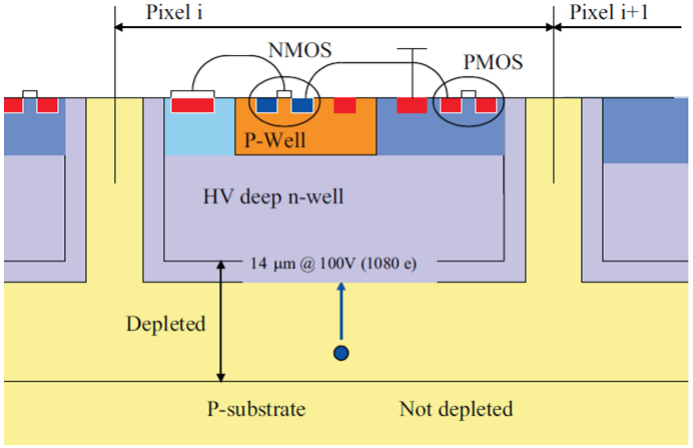
- Developments within RD50

4. Instrumentation for proton therapy

5. Summary

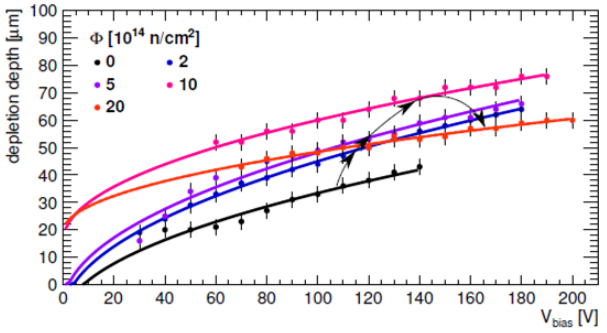
ATLAS – Technology details

- **Technology** — **0.35 µm HV-CMOS from ams**
- **Metal layers** — 4
- **Fill-factor** — Large
  Analog front-end can be implemented in the same deep n-well that acts as the collecting electrode
- **HV** — < 120 V
- **HR** — 20 Ω·cm – ~1k Ω·cm
- **Depletion region** — ~40 µm @ 200 Ω·cm & 140 V (before irradiation)
  ~60 µm @ 200 Ω·cm & 200V (after irradiation $2 \cdot 10^{15}$ n_{eq}/cm^2)
- **Radiation tolerance** — ~10^{15} n_{eq}/cm^2
- **Efficiency test beam** — 98% (before irradiation)
- **Backside biasing** — Not possible at the foundry
- **Stitching** — Not possible at the foundry



I. Peric, NIMA 650 pp. 158-162, 2011

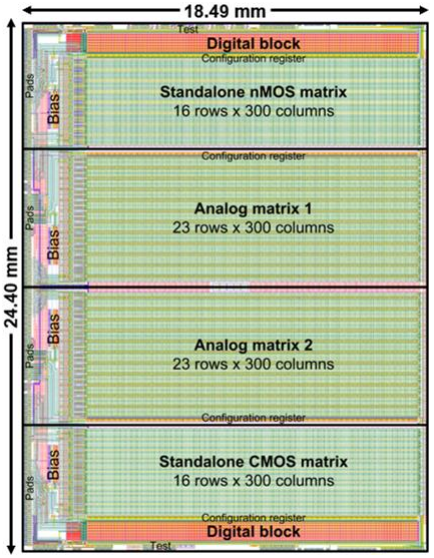
Neutron irradiation at Ljubljana + e-TCT
200 Ω·cm



E. Cavallaro, JINST 12 C01074 2017

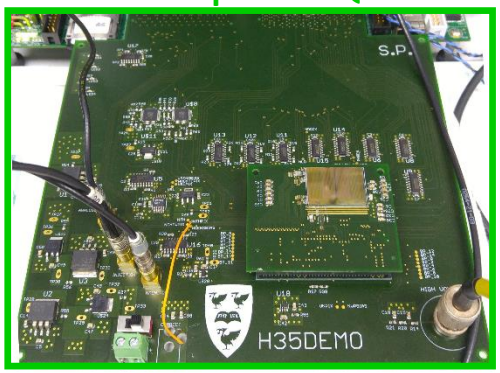
ATLAS – H35DEMO

- **Technical details (eng. run, tape out October 2015)**
  - First engineering run in 0.35 µm ams
  - Manufactured on wafers with different substrate resistivities: 20 Ω·cm, 50-100 Ω·cm, 100-400 Ω·cm, 600-1.1k Ω·cm
  - Fab out in December 2015
  - 4 pixel matrices. Details:
    - 2 pixel matrices with R/O via FE-I4. Pixels without comparators.
    - 2 pixel matrices with standalone R/O. Pixels with nMOS/CMOS comparators. Digital blocks (FE-I3 style) in the periphery of the matrices.
    - Pixel size → 50 µm x 250 µm for 1-to-1 connection to FE-I4
    - Rad-hard design
    - Timing resolution → 25 ns
    - Readout speed → 320 MHz
    - Efficiency in test beams > 98%
  - Test structures for TCT/e-TCT
- **This chip is being extensively tested**
  - Electric measurements in-lab
  - TCT, e-TCT and TPA
  - Test beams
  - Measurements after irradiation
- In Liverpool, we will start measurements with irradiated chips very soon

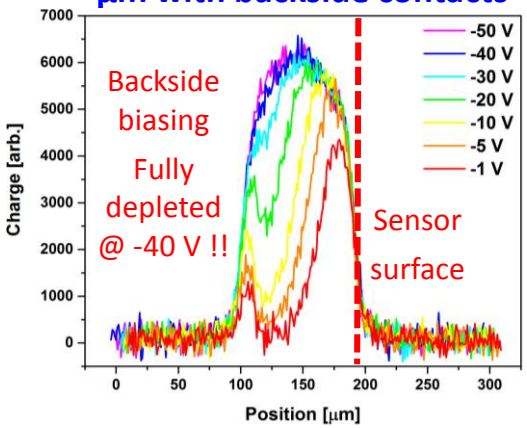


E. Vilella, JINST 11 C01012, 2016

Liverpool DAQ



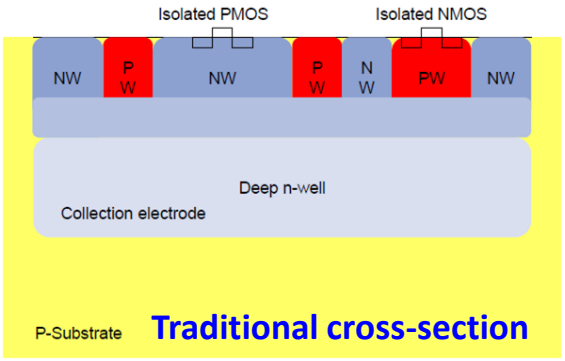
1k Ω·cm chip thinned to 100 µm with backside contacts

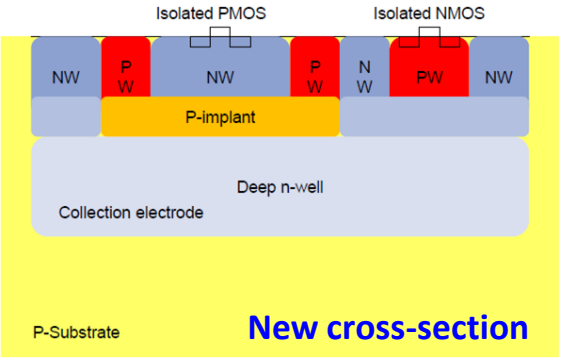


E. Vilella, JINST 12 C05001, 2017

ATLAS – Technology details

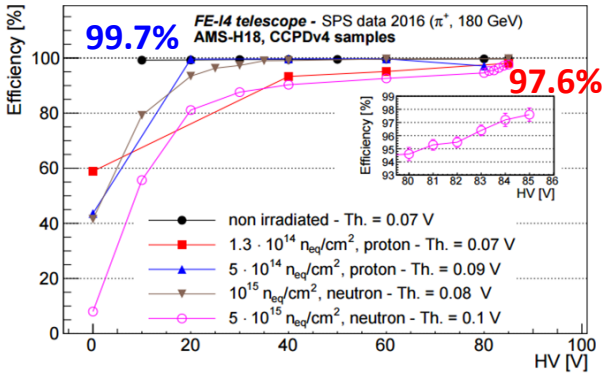
- **Technology** — **180 nm HV-CMOS from ams**
- **Metal layers** — 6
- **Fill-factor** — Large
  Analog front-end can be implemented in the same deep n-well that acts as the collecting electrode
  Currently working with the foundry to develop an isolating deep p-well
- **HV** — < 120 V
- **HR** — 10 Ω·cm – ~1k Ω·cm (since 2017)
- **Depletion region** — ~30 µm @ 10 Ω·cm & 90 V (before irradiation)
  ~45 µm @ 10 Ω·cm & 90V (after irradiation $4 \cdot 10^{15}$ n_{eq}/cm^2)
- **Radiation tolerance** — ~10^{15} n_{eq}/cm^2
- **Efficiency test beam** — 99.7% (before irradiation)
  97.6% (after irradiation $5 \cdot 10^{15}$ n_{eq}/cm^2)
- **Backside biasing** — Not possible at the foundry
- **Stitching** — Not possible at the foundry





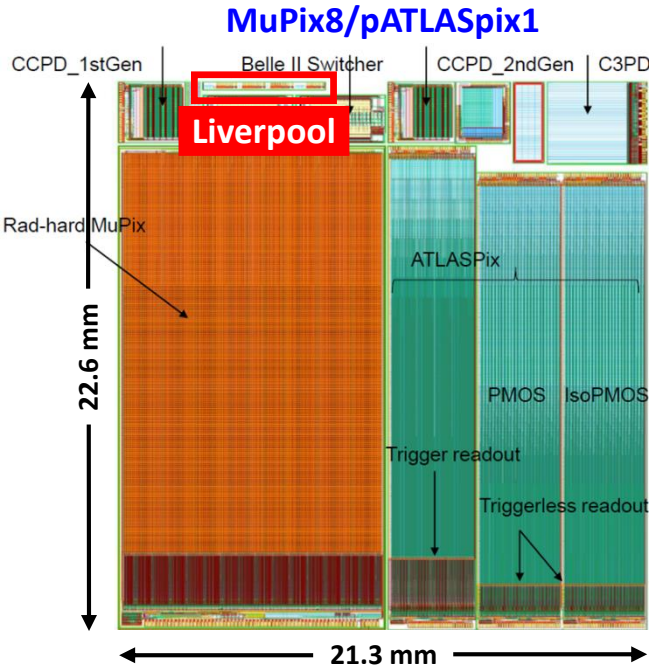
I. Peric, 12th Trento Workshop, 2017

Efficiency in test beam



M. Benoit, arXiv:1611.02669v1, 2016

ATLAS – ATLASpix series



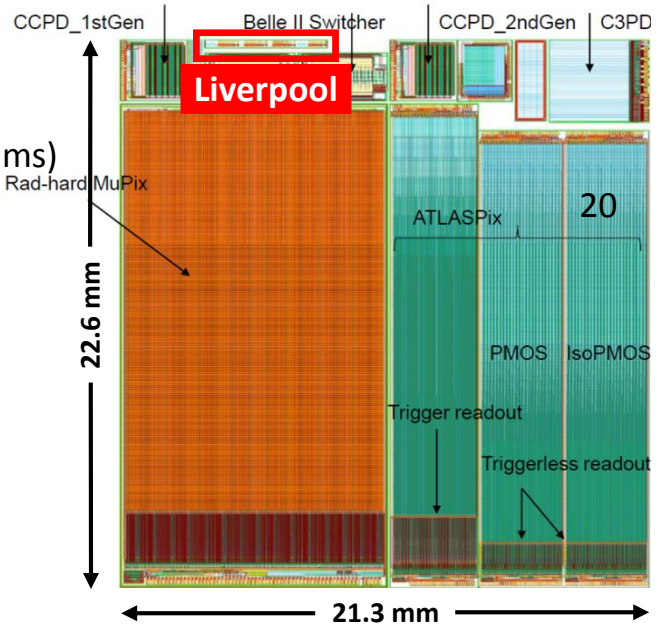
I. Peric, 12th Trento Workshop, 2017

- **pATLASpix1 (eng. run, tape out January 2017)**
  - Shared submission with MuPix8 (first eng. run in 180 nm ams)
  - Manufactured on wafers with different substrate resistivities: 10 Ω·cm, 50-100 Ω·cm, 100-400 Ω·cm, 600-1.1k Ω·cm
  - Fab out in July 2017
  - 3 pixel matrices with different layouts and comparator isolation from sensor + basic periphery logic
  - Measurements: Characterise pixel matrices implemented in special aH18 process with pMOS isolation from deep n-well and different substrate resistivities
- **pATLASpix2 (MPW, tape out August 2017)**
  - No pixel matrix
  - Prototype periphery blocks: channel synchroniser, command decoder (CD), CD to matrix interface, Aurora 8b/10b encoder, fast control state machine, SEU tolerant configuration memory, trigger buffer with ToT and content addressable, PLL, serializer, bandgap, ADC and power regulator
- **pATLASpix3 (eng. run, tape out February 2018)**
  - Full matrix + periphery (foreseen area is ~10% of the chip) with detailed verification
  - Target pixel size ~50 µm x 100 µm
- **ATLASpix (eng. run, tape out 2018) → Ultimate goal is to provide a drop-in solution for ATLAS ITk**
  - 2 cm x 2 cm full scale monolithic HV-CMOS sensor with readout compatible with lpGBT and RD53A DAQ

Mu3e – MuPix series

- **MuPix8 (eng. run, tape out January 2017)**
  - Shared submission with pATLASpix1 (first eng. run in 180 nm ams)
  - Manufactured on wafers with different substrate resistivities: 10 Ω·cm, 50-100 Ω·cm, 100-400 Ω·cm, 600-1.1k Ω·cm
  - Fab out in July 2017
  - 1 pixel matrix with 200 x 128 pixels. Details:
    - Pixel size is 80 µm x 80 µm
    - In-pixel CSA and output driver only
    - Hit info → x-address, y-address, 10-bit TS, 6-bit amplitude
    - Hit driven, triggerless R/O
    - Time resolution → 6.25 ns
    - Nominal power consumption → 300 mW per matrix
  - Test beam campaigns scheduled

MuPix8/pATLASpix1

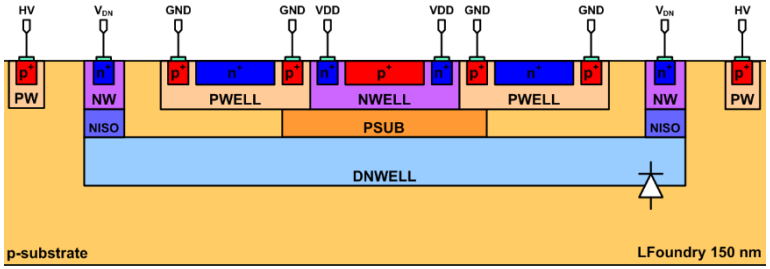


I. Peric, 12th Trento Workshop, 2017

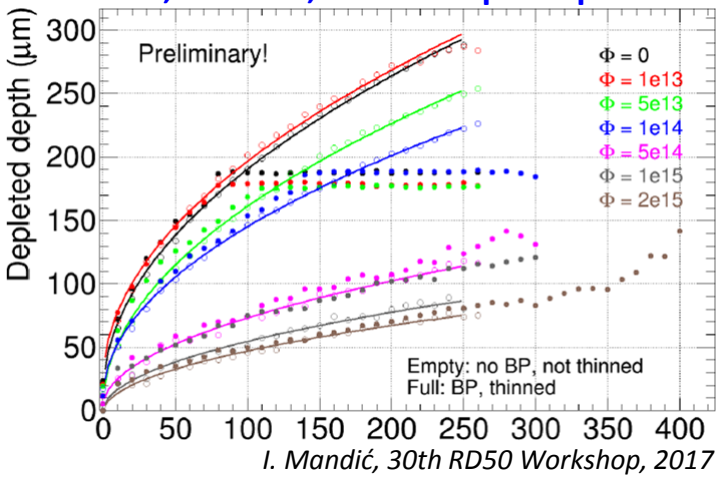
- **MuPix9 (MPW, tape out August 2017)**
  - Chip to fix bugs and improve features (Uni. Liverpool → design of analog buffer as part of slow control)
  - Only standard resistivity (10 Ω·cm) is possible
  - Fab out in November 2017
- **MuPix10 (engineering run, tape out scheduled February 2018)**
  - Production chip with a full size of 20 mm x 23 mm
  - Fab out in summer 2018 (expected)
- Uni. Bristol, Uni. Liverpool and Uni . Oxford → assembly of outer pixel layers

ATLAS and R&D – Technology details

- **Technology** — **150 nm HV-CMOS from LFoundry**
- **Metal layers** — 6
- **Fill-factor** — Large
  Analog and digital front-end can be implemented in the same deep n-well that acts as the collecting electrode
  Deep p-well (PSUB) to isolate n-wells from deep n-well (collecting electrode)
- **HV** — < 300 V (depends on sensor design)
- **HR** — 10 Ω·cm – ~4k Ω·cm
- **Depletion region** — ~300 µm @ 2k Ω·cm & 300V (before irradiation)
  ~80 µm @ 2k Ω·cm & 250V (after irradiation $2 \cdot 10^{15}$ n_{eq}/cm^2)
- **Radiation tolerance** — ~10^{15} n_{eq}/cm^2
- **Backside biasing** — Possible at the foundry
- **Stitching** — Possible at the foundry



e-TCT, 2k Ω·cm, BP = back plane processed

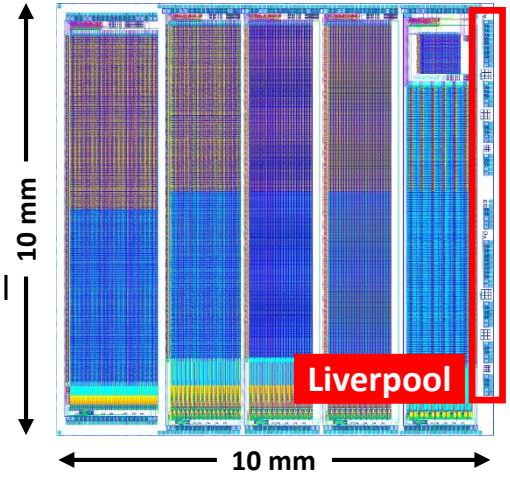


I. Mandić, 30th RD50 Workshop, 2017

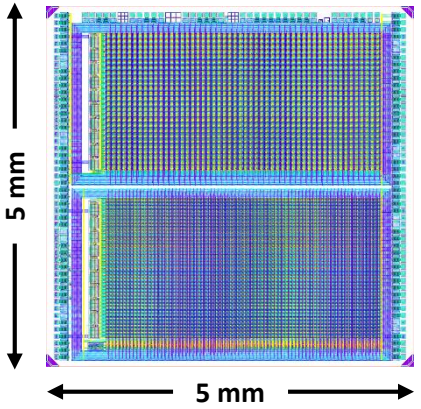
ATLAS – LF_ATLASpix series

- **LF_ATLASpix (MPW, tape out August 2016)**
  - Manufactured on wafers with different substrate resistivities: 100 Ω·cm, 500-1.3k Ω·cm, 2k-2.5k Ω·cm and 3.6k-3.9k Ω·cm
  - Fab out in February 2017
  - Design contributions from IFAE, KIT, Uni. Geneva and Uni. Liverpool
  - 6 pixel matrices (1 CCPD and 5 fully monolithic)
  - Test structures for TCT and e-TCT
  - Measurements: Have just started
- **LF2 (MPW, tape out November 2016)**
  - Manufactured on wafers with different substrate resistivities: 500 Ω·cm and 1.9k Ω·cm
  - Fab out in April 2017
  - Design contributions from IFAE, Uni. Geneva and Uni. Liverpool
  - 2 fully monolithic matrices with standalone R/O. Details:
    - Pixel size → 50 µm x 50 µm
    - Analog and digital front-end is embedded inside the pixel area
    - Digital front-end is based on FE-I3 (ToT information, pixel address)
  - Test structures for TCT and e-TCT
  - Measurements: Have just started (issue with leakage current and low breakdown voltage)

LF_ATLASpix



LF2



R&D – Plans

- **MPW**
  - Target → Test technical details to guarantee the success of the main production:
    1) Apply the **required HV for efficient signal collection and good radiation tolerance:** Maximum HV is dependent on the PWELL/NWELL gap
    2) Study the **parasitic capacitance of the sensor and its implications on the timing and noise:** Large contribution from the PSUB/DNWELL junction
    3) Analyse **isolation between PWELLs at different ground voltages** (analog and digital ground) inside the pixel sensing area
  - TCAD simulations to study the sensor are running in parallel to the design of the chip
  - Tape out → 14-August-2017 (if time allows) or 23-October-2017
  - Measurements will reveal details before the submission of the MLM/engineering run and corrections will be implemented where required
- **MLM/Engineering run**
  - Target:
    1) Improve the **timing resolution** of HV-CMOS sensors with different solutions implemented at the readout circuit level
    2) Study **new sensor cross-sections**
    3) Study **pre-stitching options** to increase the device area beyond the reticle size limitation
    4) Test structures
  - The design of this submission will continue in parallel to the design of the MPW submission

R&D – Plans

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  - Target → Test technical details to guarantee the success of the main production:
    1) Apply the **required HV for efficient signal collection and good radiation tolerance:** Maximum HV is dependent on the PWELL/NWELL gap
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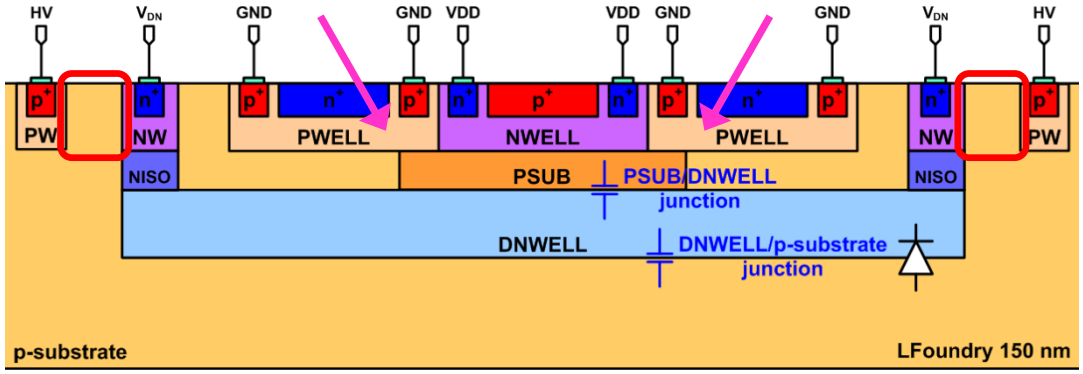
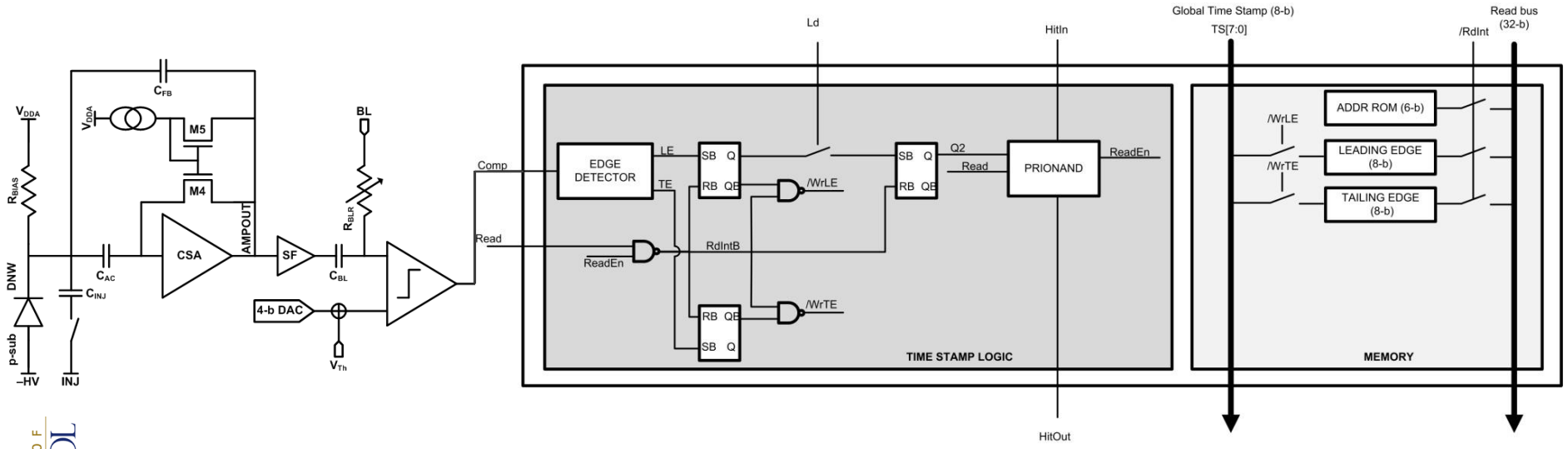


R&D – MPW



- The **analog readout** is based on a **biasing circuit, CSA, low-pass/high-pass filters and discriminator**
  - The CSA is a single folded Cascode with pMOS input transistor with programmable discharging current
  - The baseline (BL) voltage and low-pass/high-pass filters are adjustable
  - The discriminator has a local 4-bit DAC to compensate for offset variations
- The **digital readout** is based on the FE-I3:
  - **Two 8-bit DRAM memories** that continuously store two time stamps (Leading Edge, Trailing Edge)
  - ToT = TE – LE (off-chip)
  - **One 8-bit ROM memory** to store the pixel address
  - **Electronics (edge detector)** to process the output of the discriminator and tell when the LE and TE have to be stored
- Pixel receives an 8-bit Gray encoded TS running at 40 MHz
- Design effort by IFAE and the University of Liverpool

R&D – MLM/Engineering run

CERN/RD50 collaboration:

- International project to develop radiation hard semiconductor devices for very high luminosity colliders

Target of this submission:

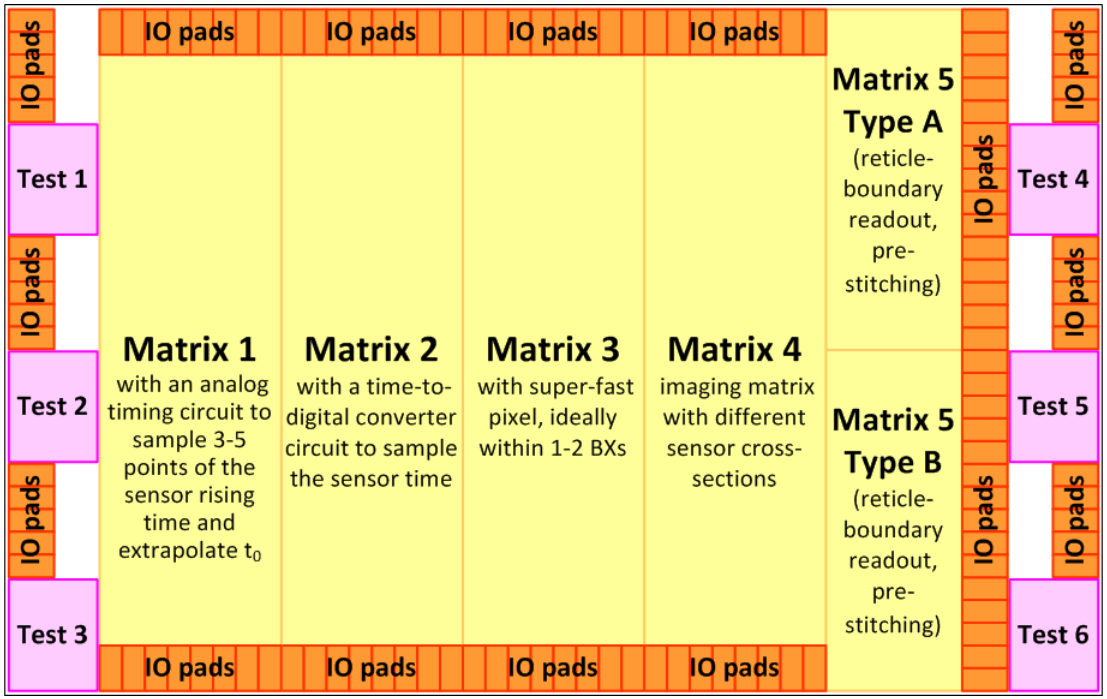
- Improve the timing resolution of HV-CMOS sensors with different solutions implemented at the readout circuit level
- Study new sensor cross-sections
- Study pre-stitching options (increase the device area beyond the reticle size limitation)

Technology:

- 150 nm HV-CMOS from LFoundry

Design effort:

- IFAE (R. Casanova)
- Uni. Barcelona (O. Alonso)
- Uni. Liverpool (S. Powell, E. Vilella and C. Zhang)
- FBK (N. Massari and M. Perenzoni)



Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

R&D – MLM/Engineering run

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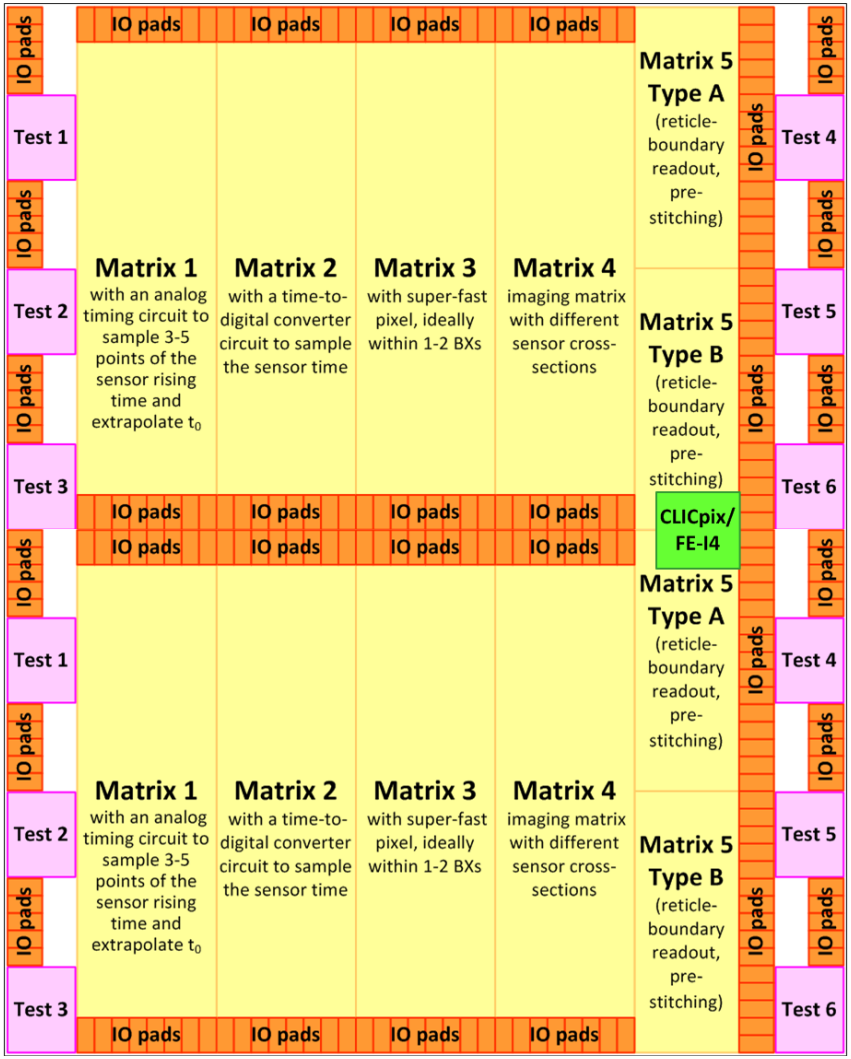
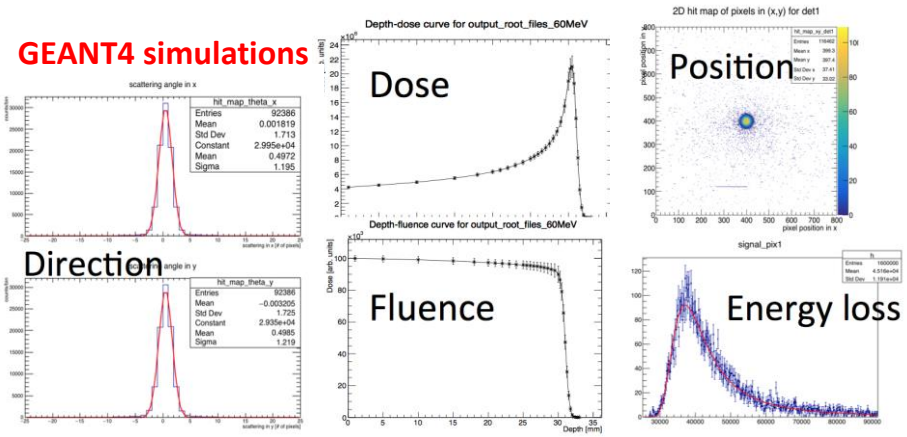
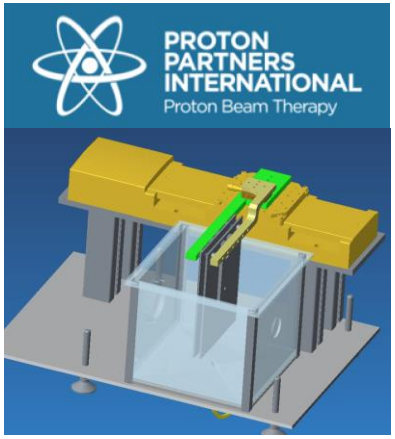


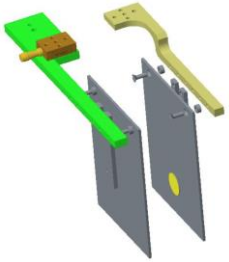
Instrumentation for proton therapy

- **A novel water phantom for hadron therapy using HV-CMOS technology**
  - **Grant →** G. Casse, J. Taylor, 1 RA and 1 technician with funding from Proton Partners International (£0.8M)
  - **Plan →** CMOS design by FBK and Uni. Liverpool
    Assembly in Uni. Liverpool cleanrooms
    Test beams planned with 60-229 MeV protons in Trento (IBA spot scanning facility)





  - 3D Water phantom design based on previous design of a 1D water phantom (using a thin silicon diode). The new design is proposed using a pair of HV-CMOS detectors designed specifically for this application.
  - A pair of thin HV-CMOS detectors offer the following **advantages**:
    - High 2D position resolution with low MCS
    - 3D dosimetry from movement along only a single axis
    - Tracking to resolve doses at high fluence
    - Tracking to measure divergence of the beam profile as a function of depth



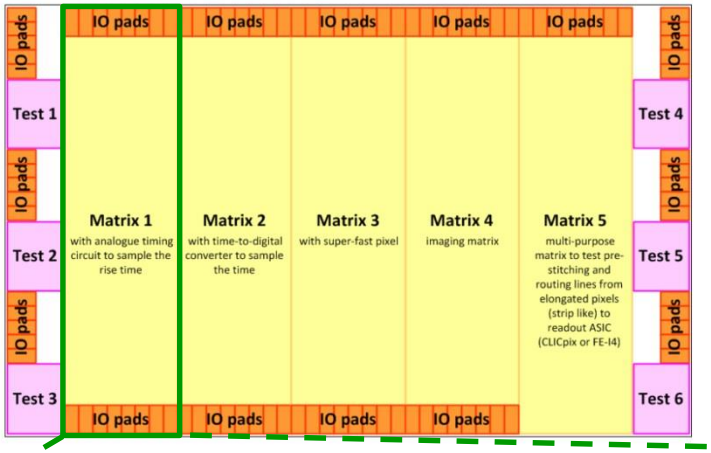
Summary

- The University of Liverpool is currently involved in the development of HV-CMOS/HV-MAPS detectors aimed at a few different applications:
  - **ATLAS**
    - In 0.35 µm and 180 nm HV-CMOS from ams, 150 nm HV-CMOS from LFoundry
    - H35DEMO → In Liverpool, we have developed our own DAQ to read the nMOS standalone matrix
      → We will start measurements with irradiated chips very soon
    - pATLASpix → Ultimate goal is to provide a drop-in solution for ATLAS ITk
    - pATLASpix1 → We are waiting for chip delivery
    - pATLASpix2 → We are contributing to the design of this chip
  - **Mu3e**
    - In ams 180 nm HV-CMOS from ams
    - MuPix8 → We are waiting for chip delivery
      → In Liverpool, we will contribute to the measurements of this chip
      → Uni. Bristol, Uni. Liverpool and Uni . Oxford → assembly of outer pixel layers
  - **R&D**
    - In 150 nm HV-CMOS from LFoundry
    - MPW → Test technical details to guarantee the success of the main production
    - Eng. run → Improve the timing resolution of the sensor, study new cross-sections and study pre-stitching options to increase the device area
  - **Instrumentation for proton therapy**

Many thanks for your attention!

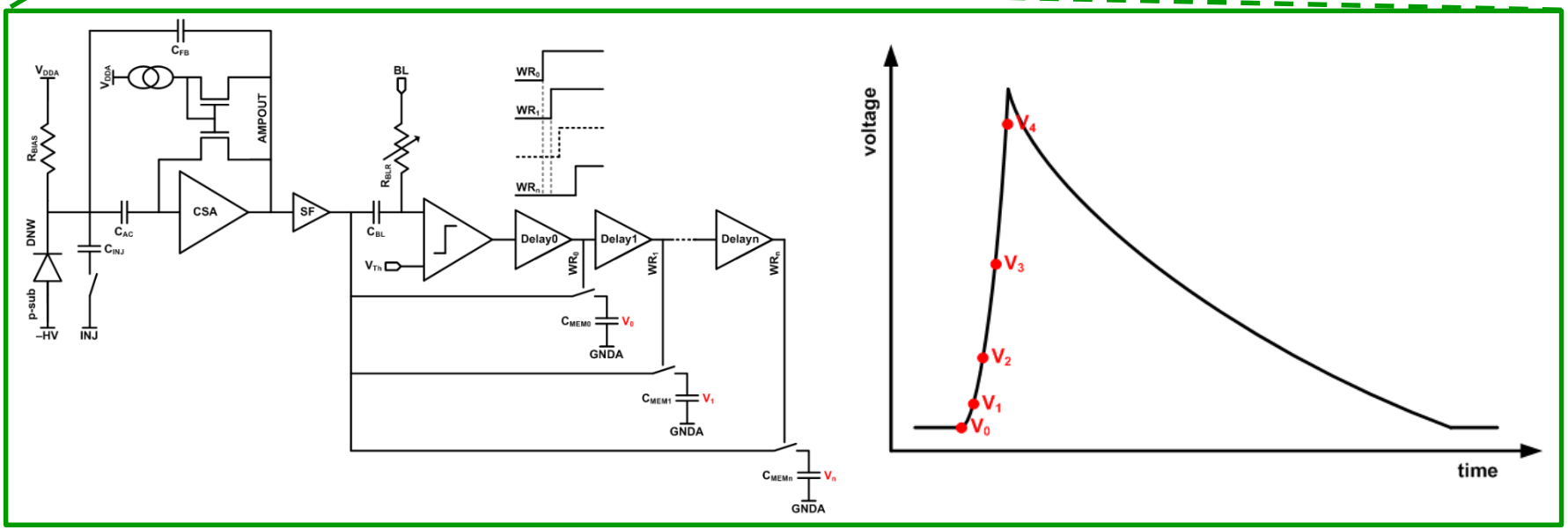
Back up slides

R&D – Matrix 1

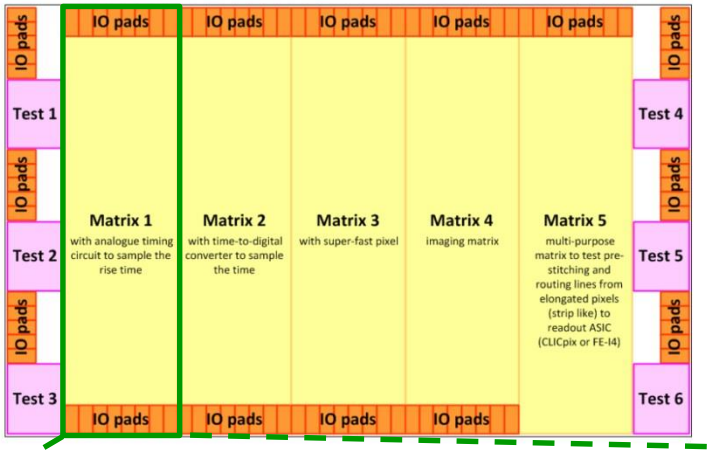


Matrix with analog sampling circuit:

- Chain of delay elements to generate WR_0, WR_1, …, WR_n (signals to enable writing the sensor analog value, i.e. the voltage) when there is an event
- First value is the baseline voltage
- Time-stamp of first value + programmable delay
- Analog memories based on metal-insulator-metal capacitances (< 5 per pixel)
- Analog serializers to send the data off-chip + off-chip ADCs
- Off-chip processing to determine t_0 (time of event)



R&D – Matrix 1



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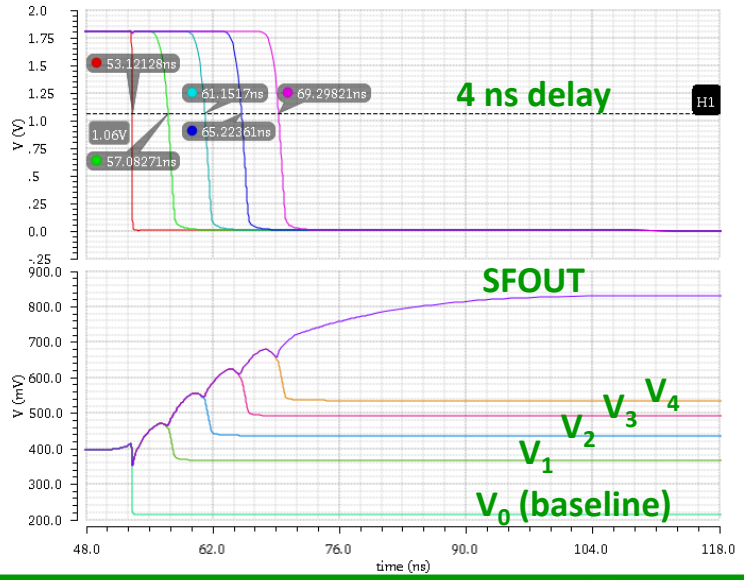
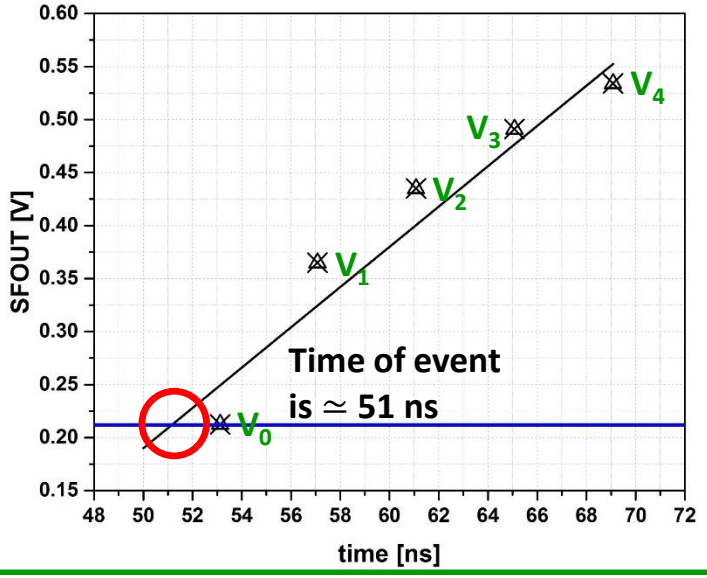
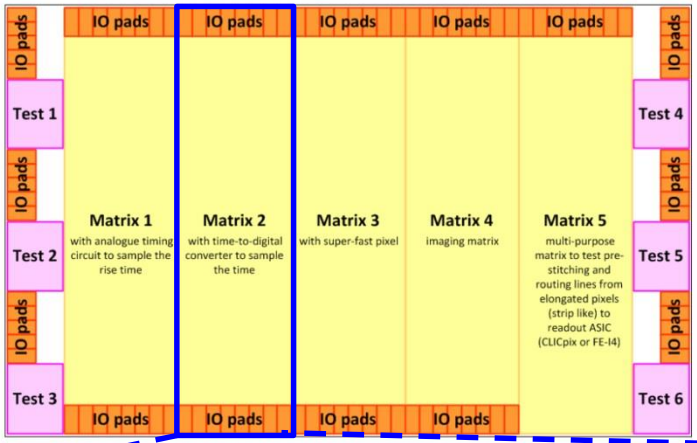


Off-chip processing →

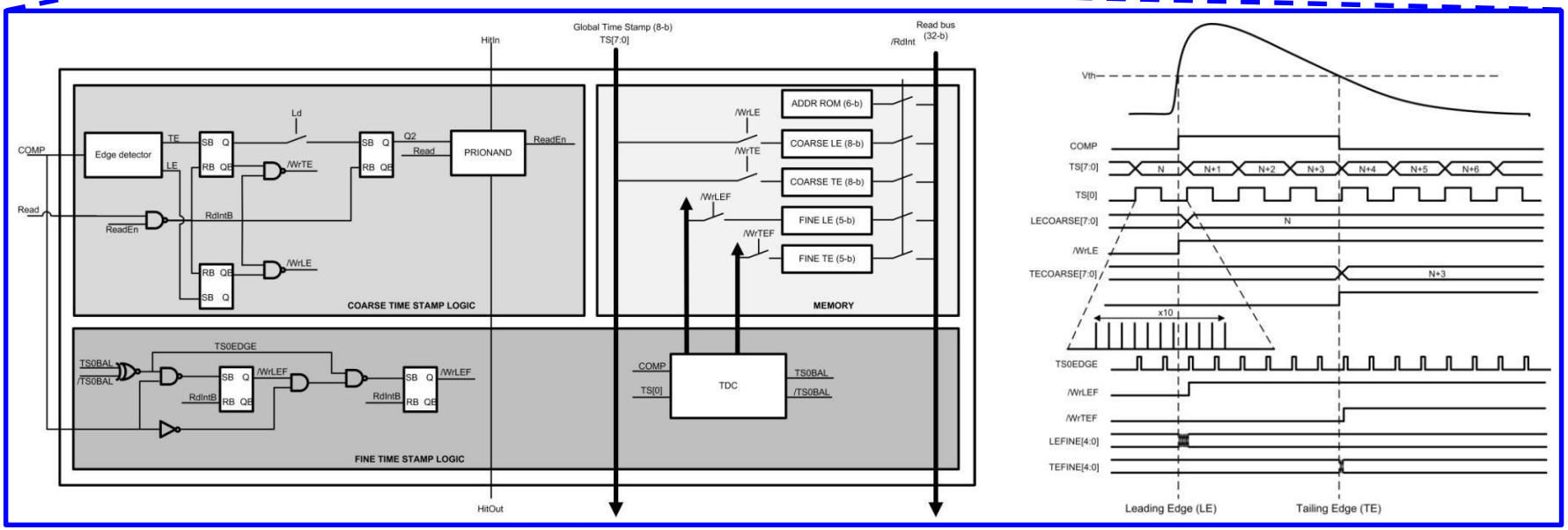


R&D – Matrix 2

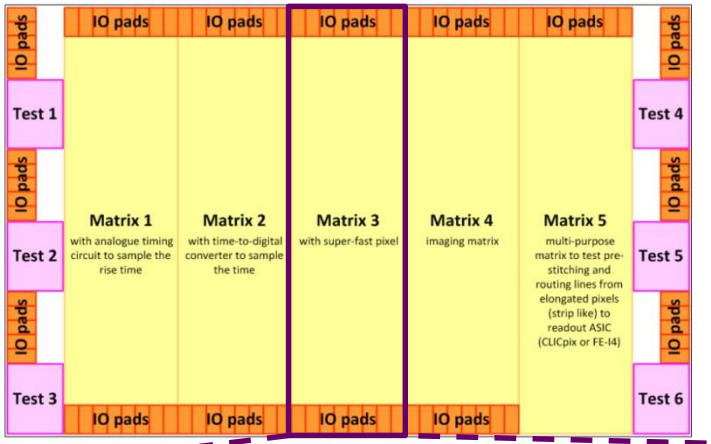


Matrix with in-pixel Time-to-Digital Converter (TDC):

- Leading Edge and Trailing Edge time stamp capture
- TS measured with 2.5 ns accuracy:
  - Coarse time measurement (25 ns accuracy) → global time stamp
  - Fine time measurement (2.5 ns accuracy) → TDC

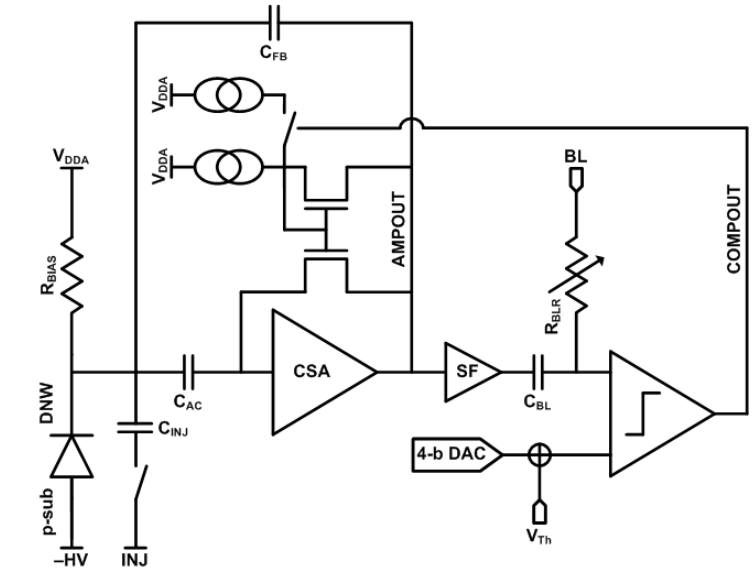


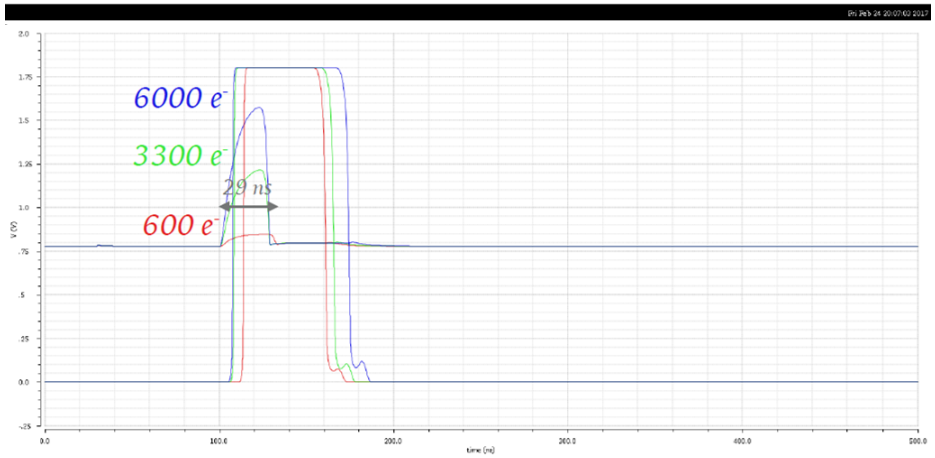
R&D – Matrix 3



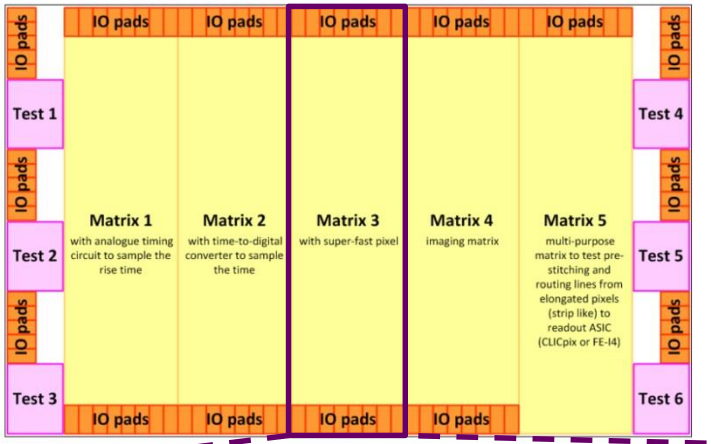
Matrix with very fast amplifier:

- The target is to recover BL voltage after an event in < 2 BXs
- **Option 1** → Amplifier with continuous slow reset + switched fast reset
- The output of the comparator is used to enable the fast reset when there is an event
- The current consumption is slightly higher only when there is an event (total power consumption per pixel is ≃ 30 µW)
- Total recovery time < 50 ns (independent of input energy)
- No ToT info is possible





R&D – Matrix 3



Matrix with very fast amplifier:

- The target is to recover BL voltage after an event in < 2 BXs
- **Option 2** → Fast amplifier with continuous reset
- Optimized transistor sizing and biasing
- Total recovery time is ≃ 50 ns (dependent on input energy)
- ToT info is possible