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Depleted Monolithic Active Pixel Sensors for ATLAS Upgrade

Dima Maneuski et. al.

Presentation Plan

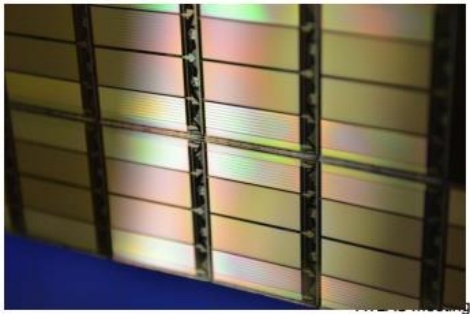
- Motivation for the ATLAS ITk
- Performance requirements
- CMOS options
- CMOS technologies
- Current CMOS developments
- AMS
- LFoundry
- TJ
- Conclusions

ATLAS Inner Tracker (ITk) for HL-LHC: ~200 m^2 silicon

- Radiation tolerant to expected fluencies
- Can operate with 25 ns bunch crossing and increased pile up
- Increased granularity
- Reduced material budget
- Low cost modules with high production throughput

Potential alternative to planar silicon sensors is commercial CMOS

- **Cost:**
  - Several vendors
  - High volume
  - Large wafers (8-12 inch)
- **Performance:**
  - Radiation hardness
  - Thinner charge collection layer
  - High S/N

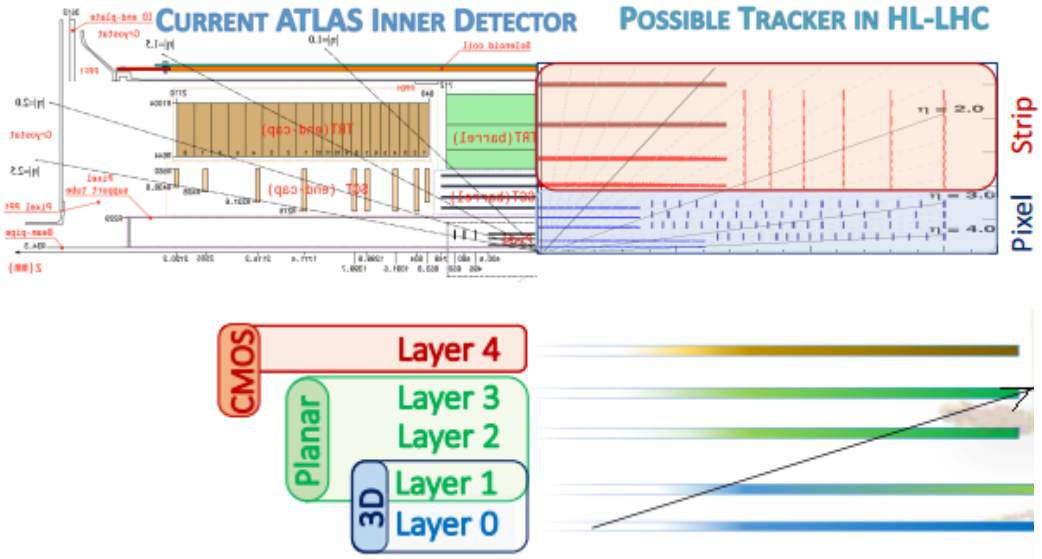


Time scale: expected switch on time around 2024

Performance requirements

- Converging on the CMOS sensor for the ITk Pixel Outer Layer 4
- 1.5x10^{15} n_{eq}/cm^2 and 80 Mrad TID
- Hitrates up to 2 MHz/mm^2 (peak)
- Timing: < 25 ns
- Efficiency: > 95% after irradiations
- Pixel size: < 50 um
- Chip size like ATLAS-1 Pixel FE chip

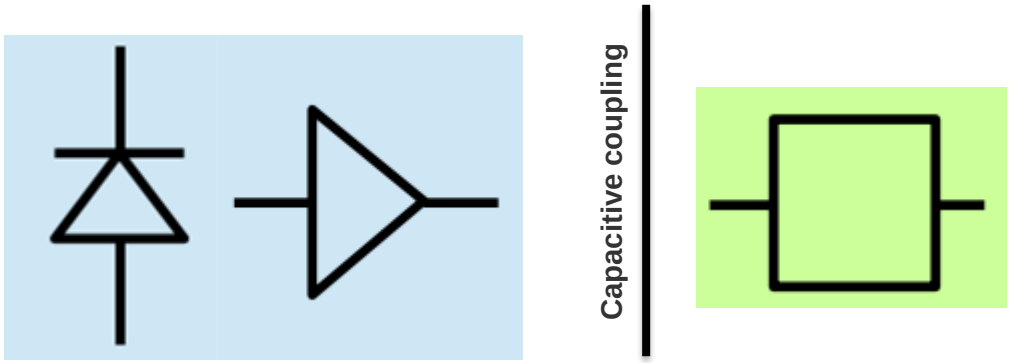
Credit: **A. Gaudiello et al.**, IWORID'17



- CMOS to be integrated into quad and double chip modules like Hybrid Pixel Module
- Interface compatible with Hybrid Quad Module towards powering and readout

CMOS options

Capacitively coupled pixel detector (CCPD)

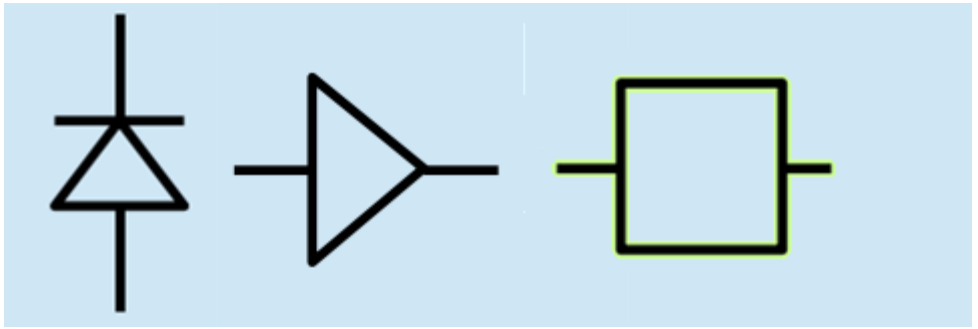


Diode + Preamp

Front End chip

- CMOS pixel + FE chip
- Thinner devices
- Flip-chip simplification

Monolithic Active Pixel Sensor (MAPS)



Diode + Preamp + Processing electronics

- Collecting diode + readout + processing electronics on wafer
- No flip-chip
- Thin devices
- Increased granularity
- Lower analog power (for small pixel capacitance designs)

Fabrication foundries under consideration

- **AMS (180 and 350 nm)**
- ESPROS (150 nm, High Resistivity option)
- Global Foundry (130 nm, High Resistivity option)
- **LFoundry (150 nm, High Resistivity option)**
- XFAB (180 nm, SOI option)
- ST Microelectronics (160 nm)
- Toshiba (130 nm)
- **Tower Jazz (180 nm, High Resistivity Epi option)**
- IBM (130 nm)
- ON Semiconductor (180 nm)

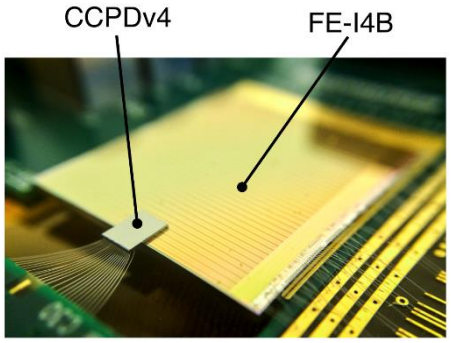
Current developments

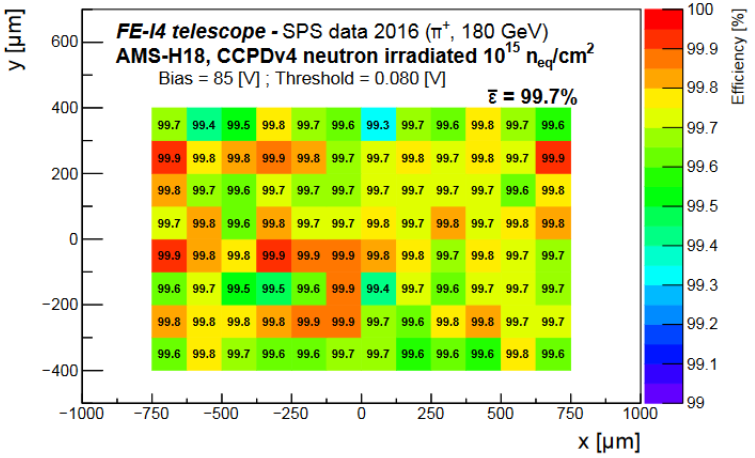
	Vendor	Sensor name	Technology node	Size (mm²)	# pixels	Pixel size (um²)
Monolithic structures – CCPD*	AMS	H18_CCPD	180 nm	2.2x4.4	Various	25x25, 33x125, 25x125, 25x350
	LFoundry	LF_CCPD	150 nm	5x5	32x140	33x125
	AMS	H35_DEMO	350 nm	18.5x24.4	16x300, 23x300	50x250
	LFoundry	LF_CPIX	150 nm	9.5x10	34x168	50x250
	TowerJazz	TJ investigator	180 nm	5x5.7	134 matrices	20x20 -> 50x50
Monolithic + periphery	LFoundry	Monopix	150 nm	9.5x10	36x142	50x250
	TowerJazz	TJ_MALTA	180 nm	18x18	512x512	36x36
	TowerJazz	TJ_Monopix	180 nm	10x18	256x512	36x40
2nd generation	AMS	ATLASPix / MuPix8	180 nm	21.3x22.6	2 matrices	56x56
	LFoundry	ATLASPix	150 nm	10x10	5 matrices	40x100, 40x60, 40x250

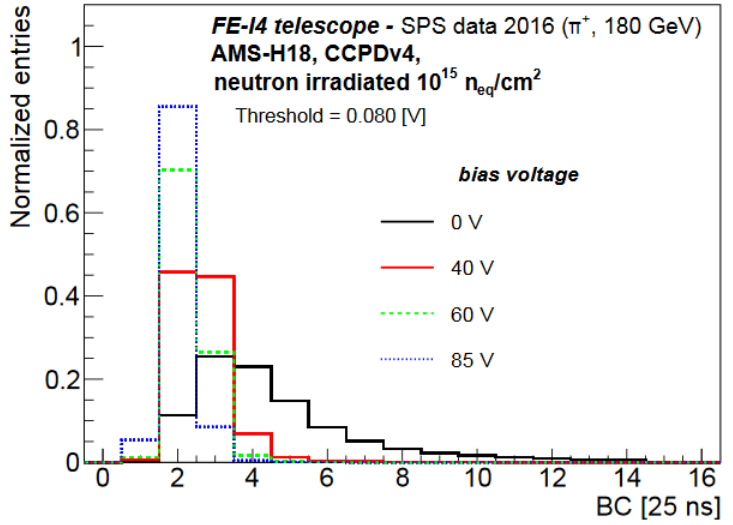
*Capacitively coupled pixel detector (CCPD)

AMS H18 CCPD (CCPDv4)

- Standard 10 Ω·cm substrate
- Irradiated to 1.3e14 and 5e15 n_{eq} / cm^2
- Developed gluing process
- Pion test beams
- Hit efficiency 97.6% (irradiated) to 99.7% (unirradiated)
- Efficiency performance comparable to planar Silicon



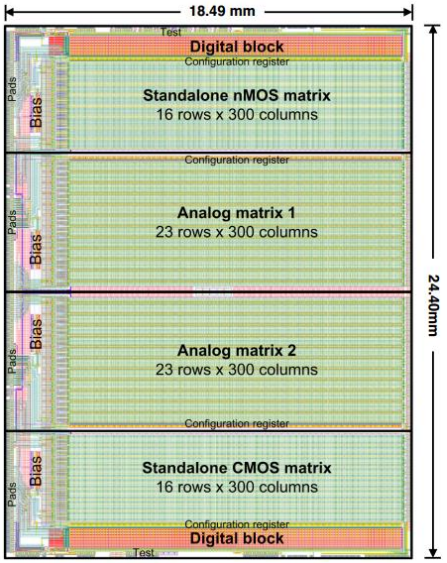


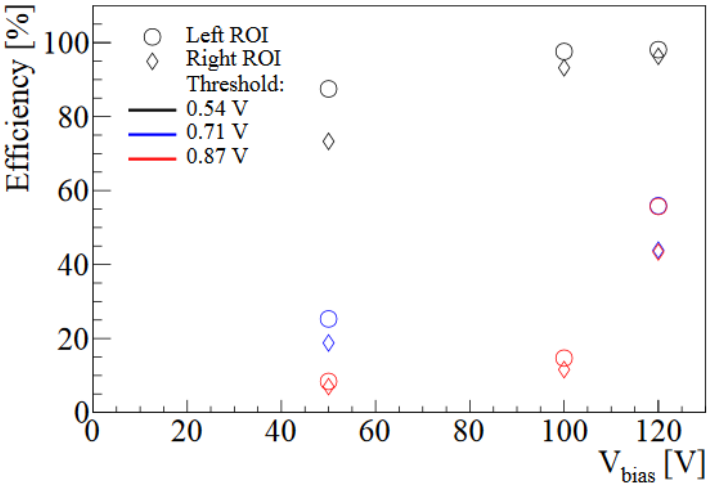


Credit: **M. Benoit et. al.** arXiv:1611.02669

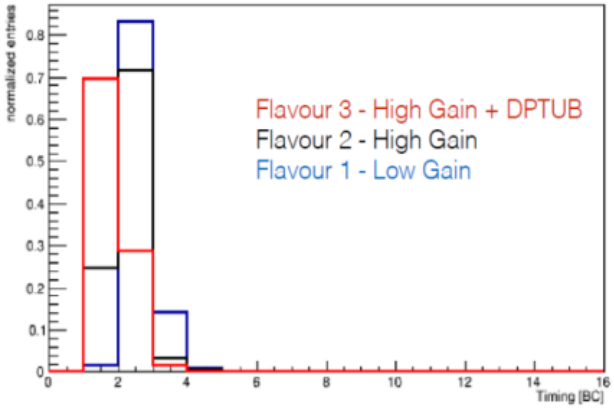
AMS H35 Demo

- Monolithic sensor demonstrator
- Different pixel flavours
- Different substrate resistivities
- Efficiency before irradiations demonstrated 99.1%
- 99% of charge collected within 2 BC





Credit: **S. Terzo et al.,** JINST 12 (2017) no.06, C06009

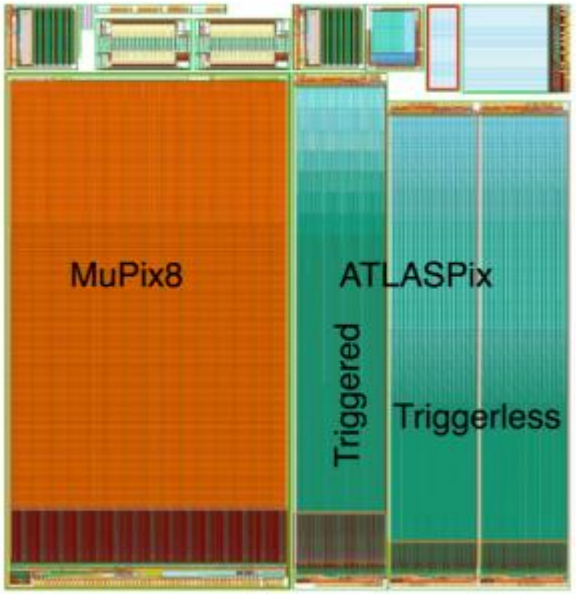


Credit: **A. Gaudiello et al.**, IWORID'17

What's next in AMS process?

AMS H18 ATLASPIX

- Drop-in solution for outer layers
- Fully integrated
- Large fill factor monolithic design
- 180 nm AMS HV CMOS
- Default resistivity is 20 Ω cm
- Triple well process



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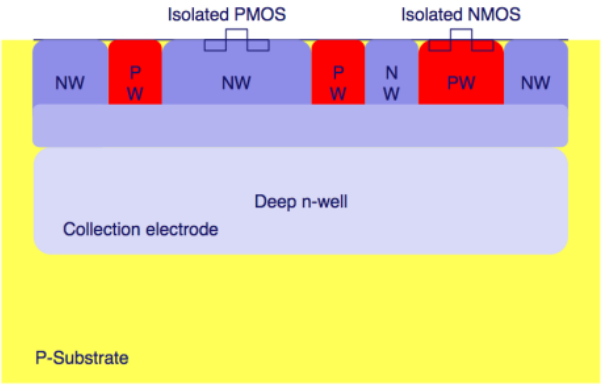
Roadmap:

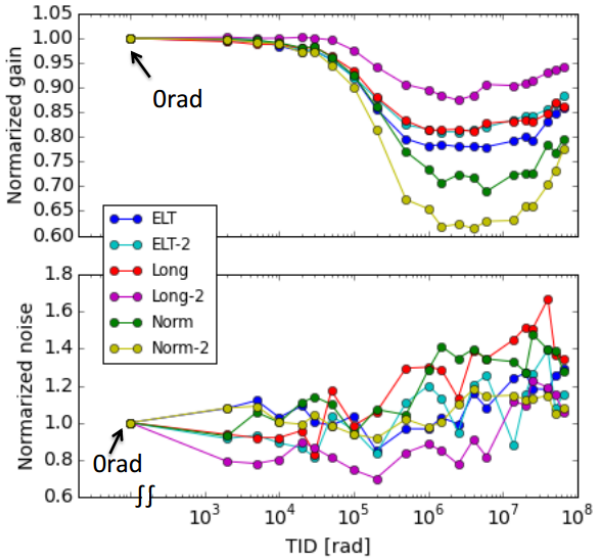
- pATLASpix-1a/b/c prototype, February 2017
- pATLASpix-2 prototype, August 2017
- Periphery blocks
- pATLASpix-3 prototype, February 2018
- Periphery + full matrix
- ATLASpix final design, 2018



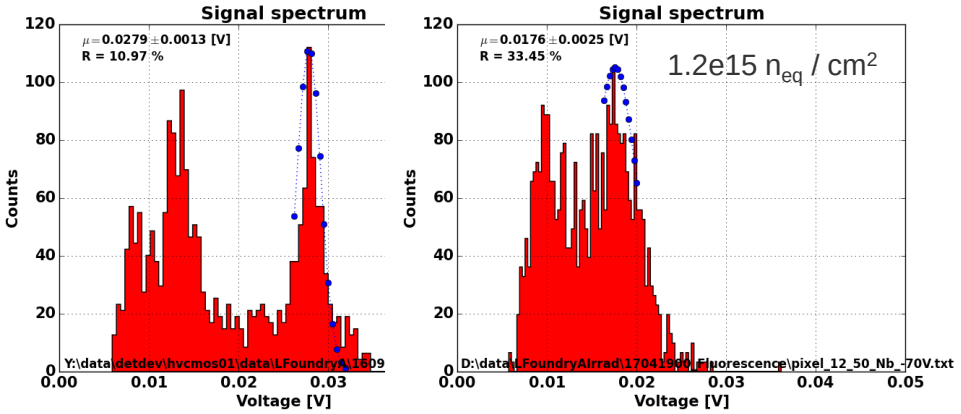
M. Prathapan, AIDA 2017

LFoundry LF_CCPD

- L-Foundry 150 nm process
- Resistivity of wafer: >2000 Ω·cm
- Chip size 5 x 5 mm
- 33 x 125 um pixel size
- 24 x 114 pixels, 3 pixel flavours
- R/O coupled to FE-I4 and stand alone
- Subpixel decoding demonstrated
- Irradiated to 50 Mrad TID
- Irradiated to 1.2e15 n_{eq} / cm^2



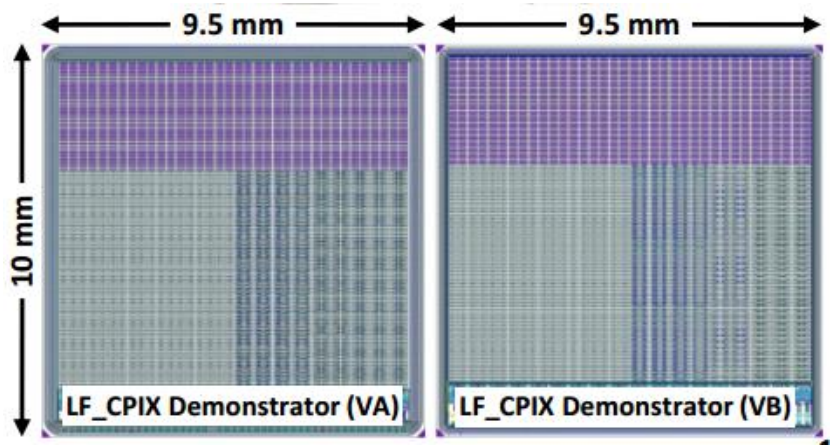
Credit: **T. Hirono et. al.**

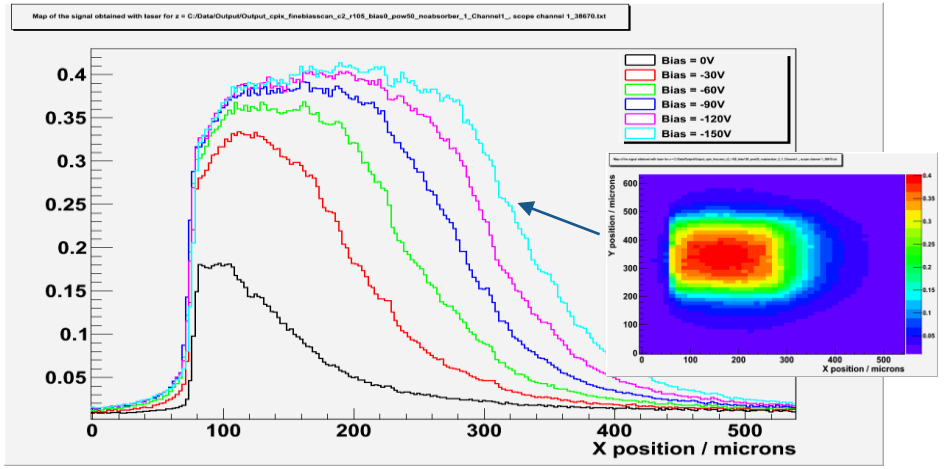


Credit: **D. Maneuski et. al.**

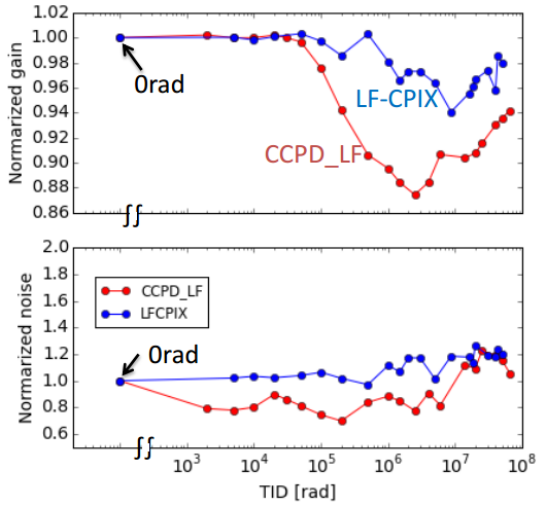
LFoundry CPIX (LF_CPIX)

- L-Foundry 150 nm process
- Resistivity of wafer: 2000 Ω·cm
- High fill factor
- Chip size 9.5 x 10 mm
- Pixel size 50 x 250 um
- 36 x 158 pixels, three pixel flavours
- Process to thin down to 100 um developed
- Better leakage current
- More radiation tolerant





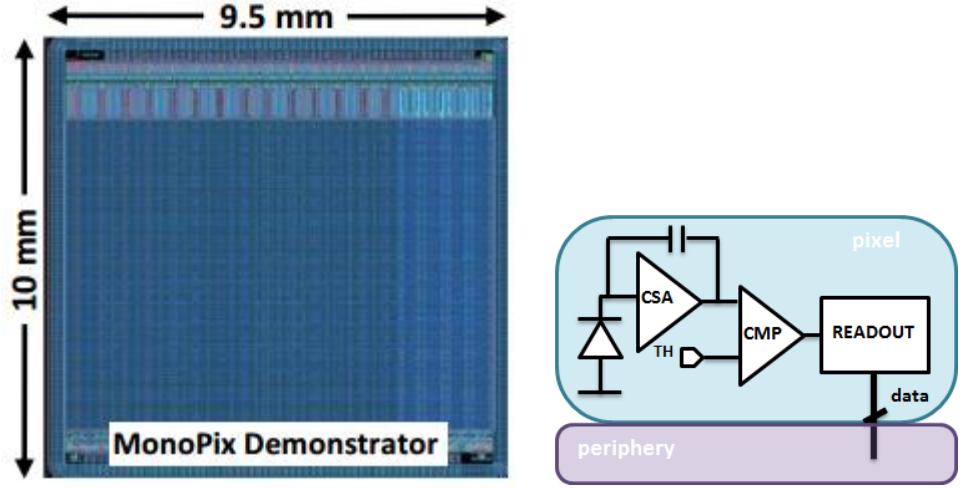
Credit: L. **Vigani et. al.**



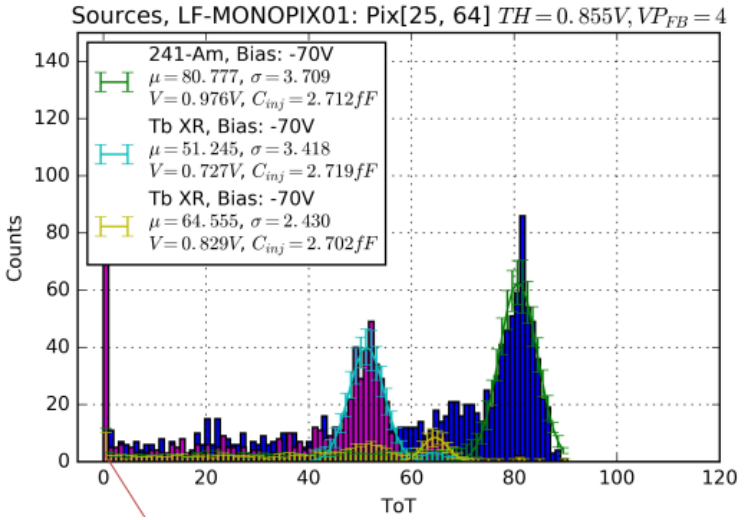
Credit: **T. Hirono et. al.**

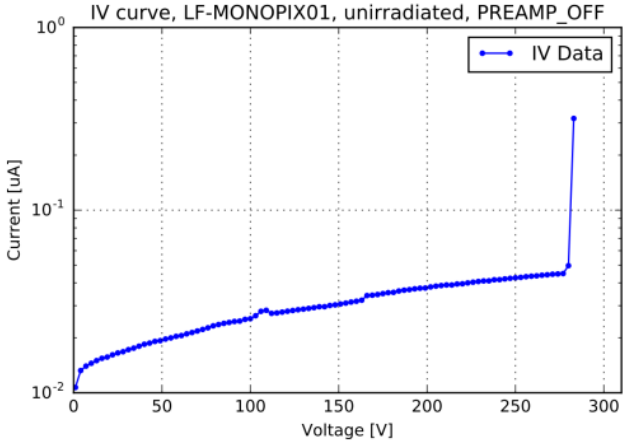
LFoundry Monopix

- Monolithic: amplifier, discriminator, ToT, readout
- Designed to satisfy noise, time, speed requirements
- Resistivity of wafer: >2000 Ω·cm
- Pixel 50 x 250 um
- 129 x 36 pixels @ 40 MHz clock
- Backside processing



Credit: **T. Wang et. al.** 2017 JINST 12 C01039



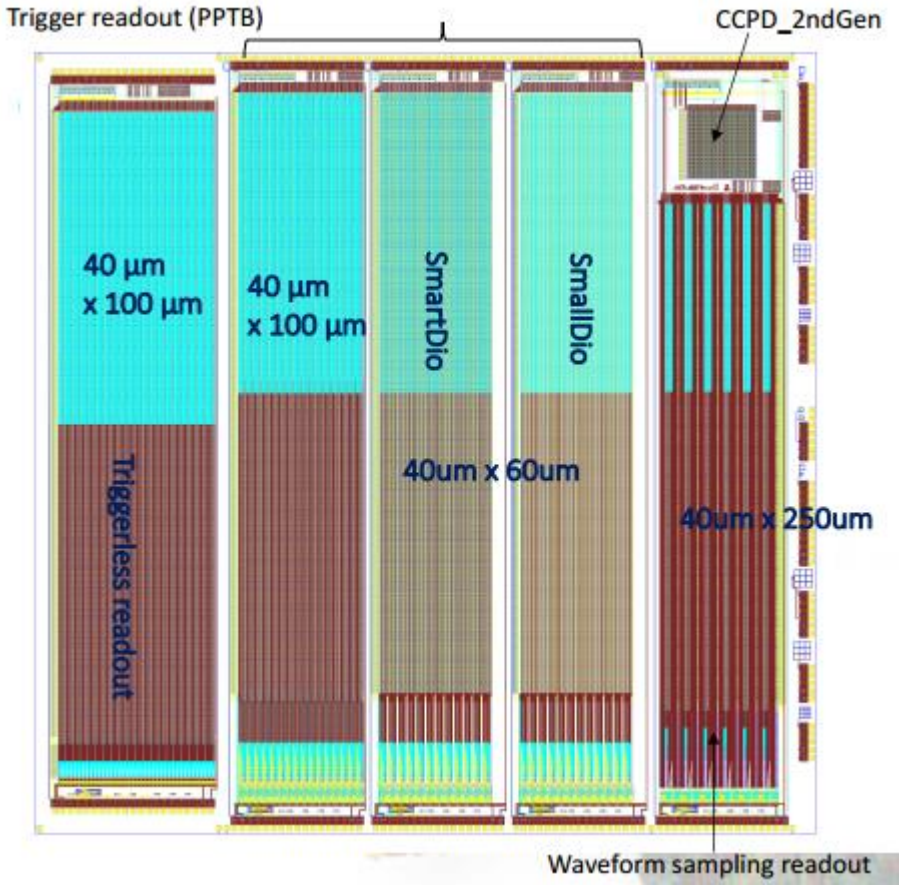


Credit: **I. Caicedo et. al.**

What's next in LF process?

LFoundry ATLASPix

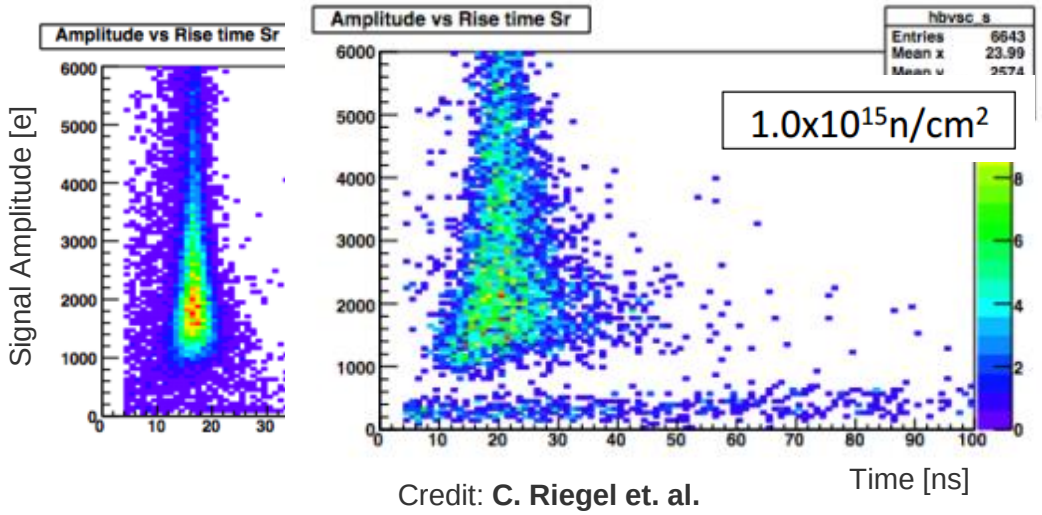
- Technology LFA15 (150 nm)
- Different pixel sizes
- Different matrices (1 CCPD and 5 monolithic) and test structures
- Resistivities: 100 Ω·cm, 500-1k Ω·cm, 1.9k Ω·cm and 3.8k Ω·cm
- 4-well HVCMOS process
- Different Readout concepts



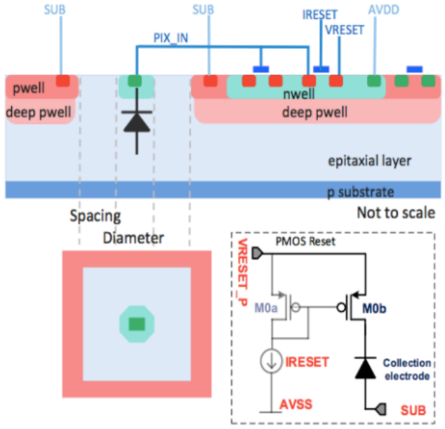
TowerJazz Investigator

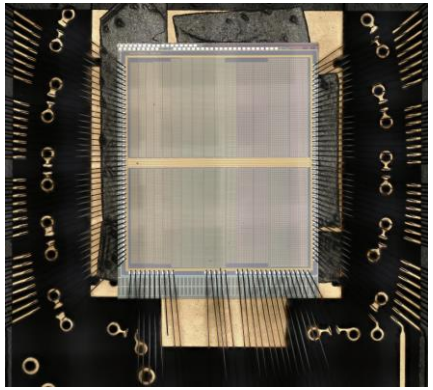
- Designed as part of the ALPIDE development for the ALICE ITS upgrade
- Emphasis on small fill-factor and low capacitance
- Epitaxial layer on high resistivity substrate
- Many variations of pixel size and layout

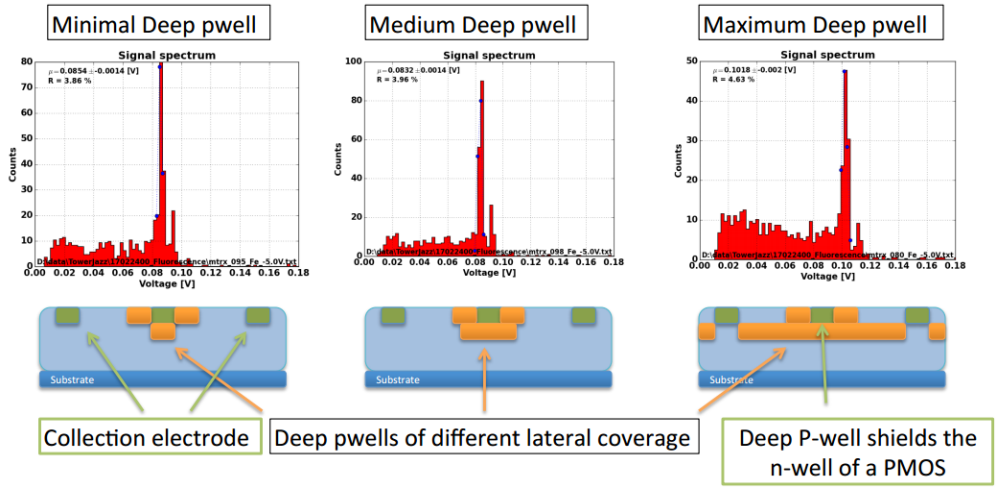
Sr90 MIP



Credit: **C. Riegel et. al.**







Credit: **D. Maneuski et. al.**

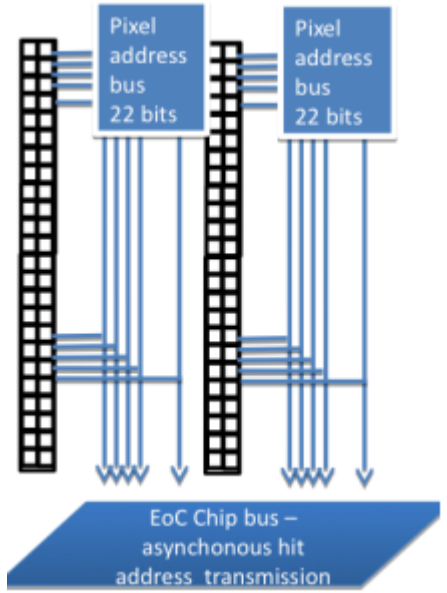
What's next in TJ process?

TJ_Malta

- Full matrix 512x512 pixels
- Active area 18 x 18 mm^2
- Hit memory in active matrix
- All hits are Asynchronously transmitted over high- speed bus to EOC logic
- No clock distribution over active matrix to minimize power and digital-analog cross-talk

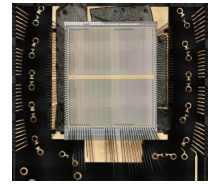
TJ_MonoPix

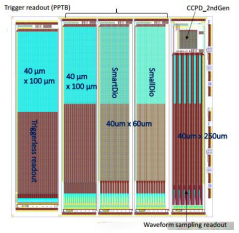
- Full matrix 512x256 pixels
- Active area 18 x 10 mm^2
- Hit memory in active matrix (2 flip-flop per pixel)
- Synchronous column drain architecture
- Hit address asserted to bus with 40MHz token
- 6 bit TOT coding at end of column

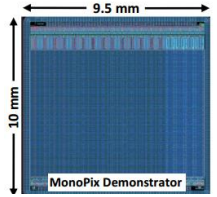


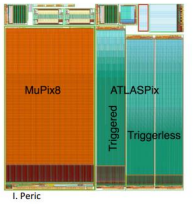
Conclusions

- Demonstration continues to show **CMOS** technology could be a **viable candidate** for the ATLAS ITk upgrade
- CMOS devices from different foundries generally **shown to operate after the expected radiation damage** at the mid/outer layer of the ATLAS ITk
- Many performance **issues** found in first iterations of designs were **addressed** in the full scale demonstrators
- General consensus to work on **Monolithic CMOS** sensor for the **outer layer** of the ITk for the TDR 2017
- Aim at the **drop-in module** solution









- CMOS developments have huge potential in fields outside particle physics

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Thank you for your attention

Any questions?