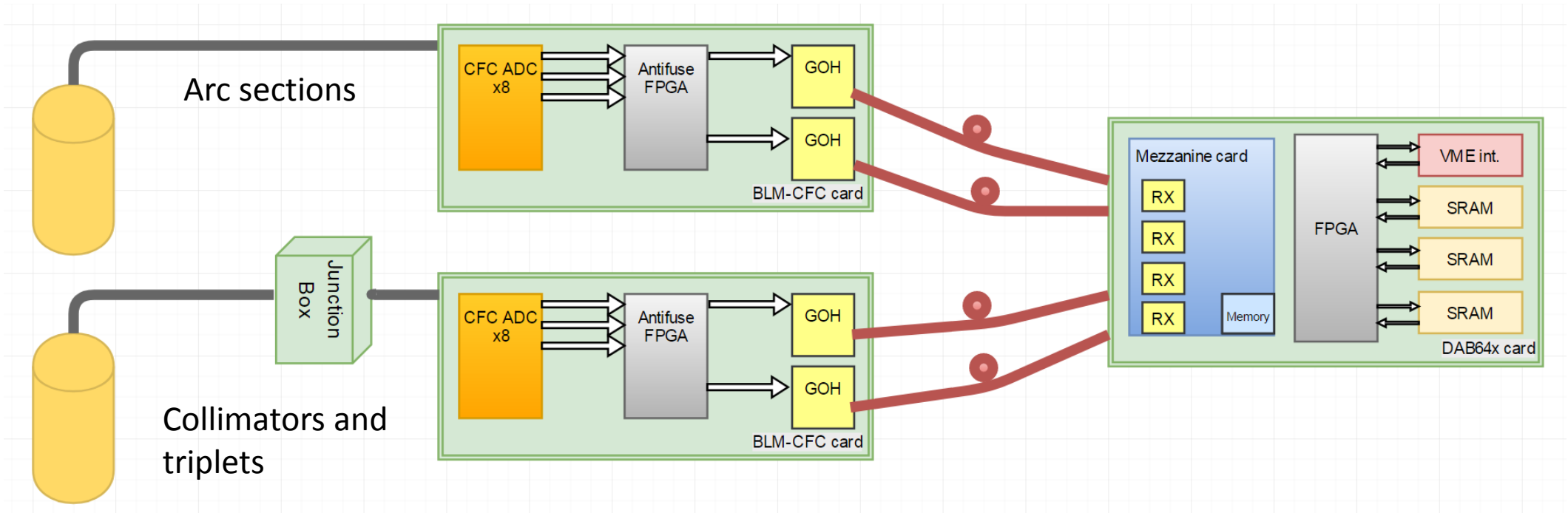
BLM ASIC V3

Overview of the project

Outline

- BLM ASIC: motivation
- Development history
- Architecture 1: Adaptive Current-to-Frequency Converter
- Architecture 2: DeltaSigma Converter
- Planning and future developments

BLM ASIC: motivation

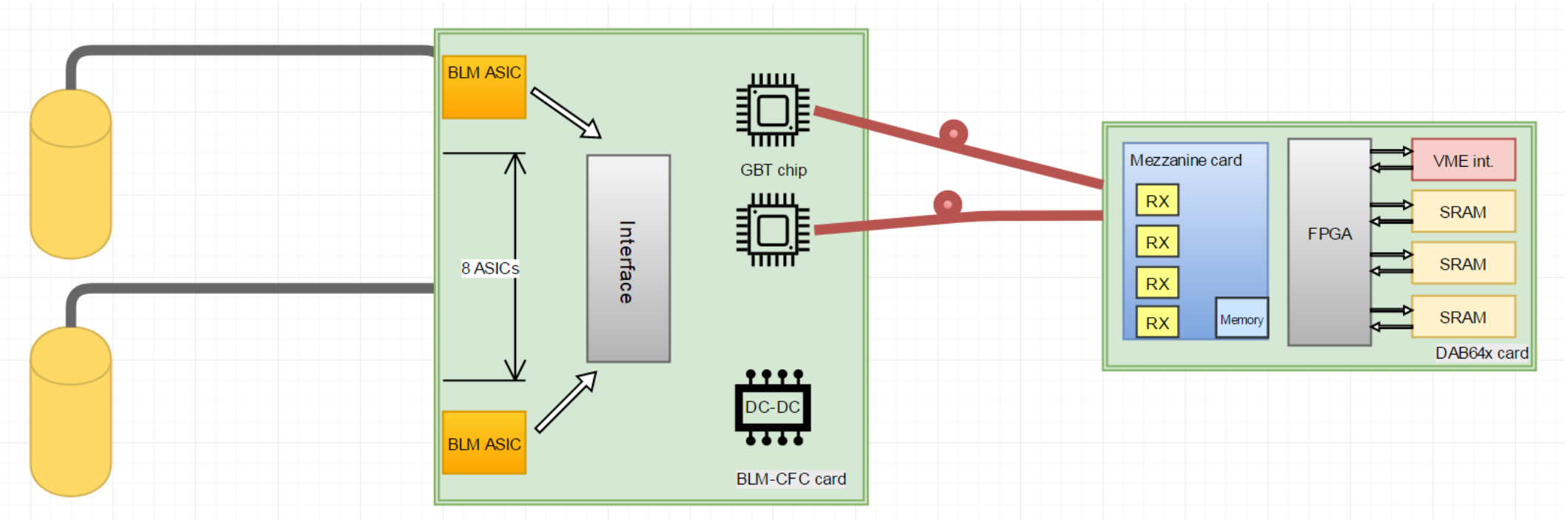


→ Idea behind the project:

a) Remove the cables and the CFC card
b) Place a readout chip next to the ionization chambers
c) Send digital data through optical link to the surface

→ BLM ASIC development

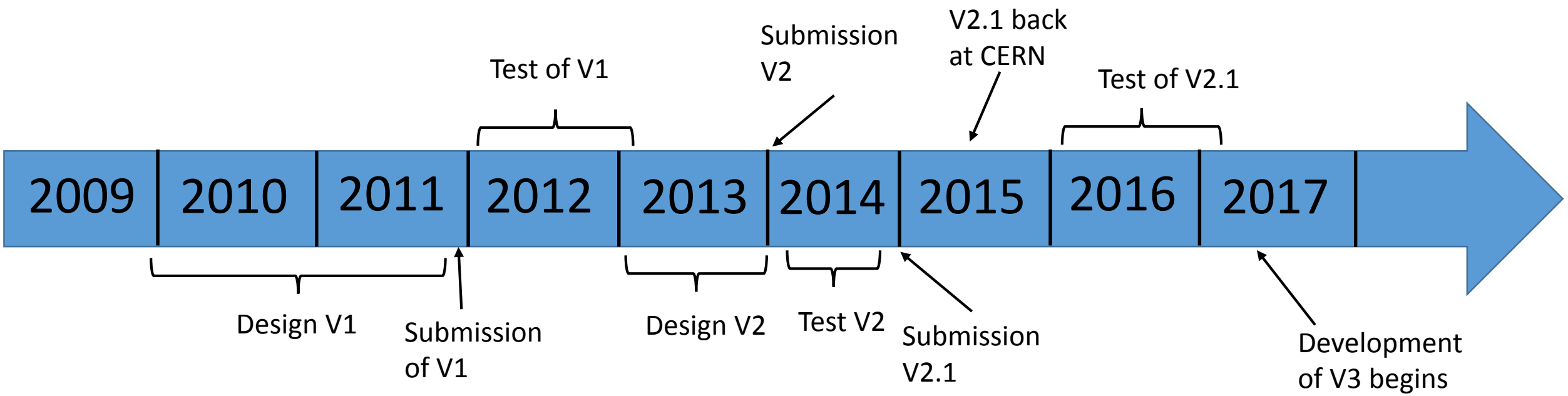
BLM ASIC: new setup under study



Some ASIC specifications:

- Dynamic range: 1 pA – 1 mA
- Dual polarity input
- Radiation hard: Total Ionizing Dose 10 kGy in 20 years → no FPGA on board

Development history

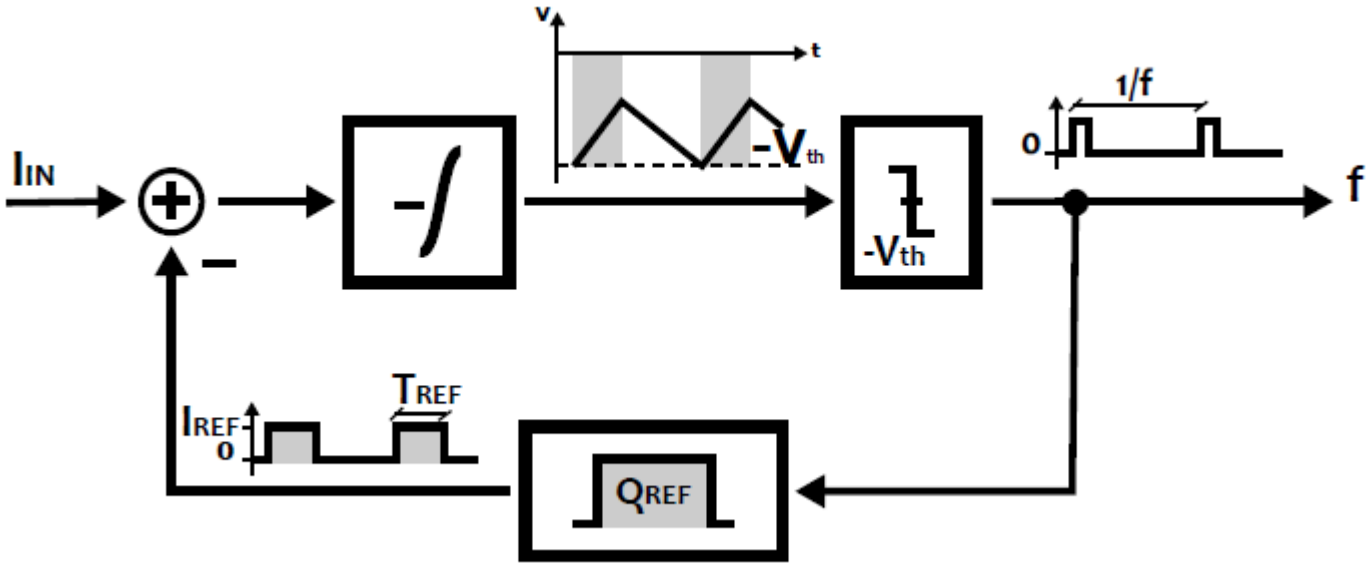


Notice:

- Technology change in V3: 250 nm → 130 nm
- Project is “restarting”
- Possibility to explore other ideas for the architecture
- Fall-back to V2 architecture if problems arise

Architecture 1: Current-to-Frequency Converter

Basic concept

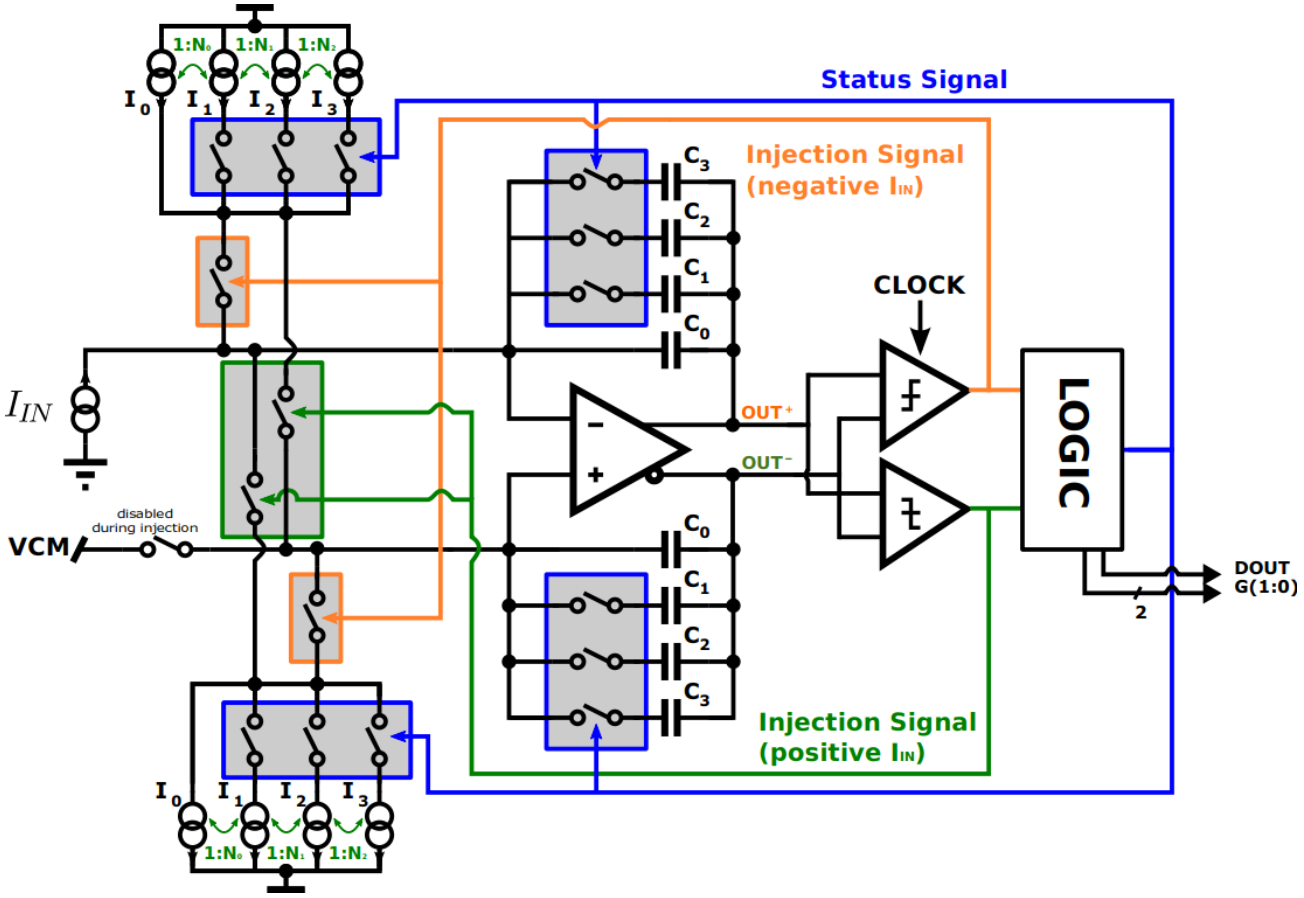


Cycle of operation (ideal) based on the charge-balance principle:

- Input current is integrated
- When the output voltage of the integrator reaches a predetermined threshold, the (clocked) comparator “fires”
- The comparator output pulse activates a current source
- The current source is used to discharge the integrator to the initial value
- The frequency of the output pulses is related to the input current: $f=I_{in}/Q_{ref}$

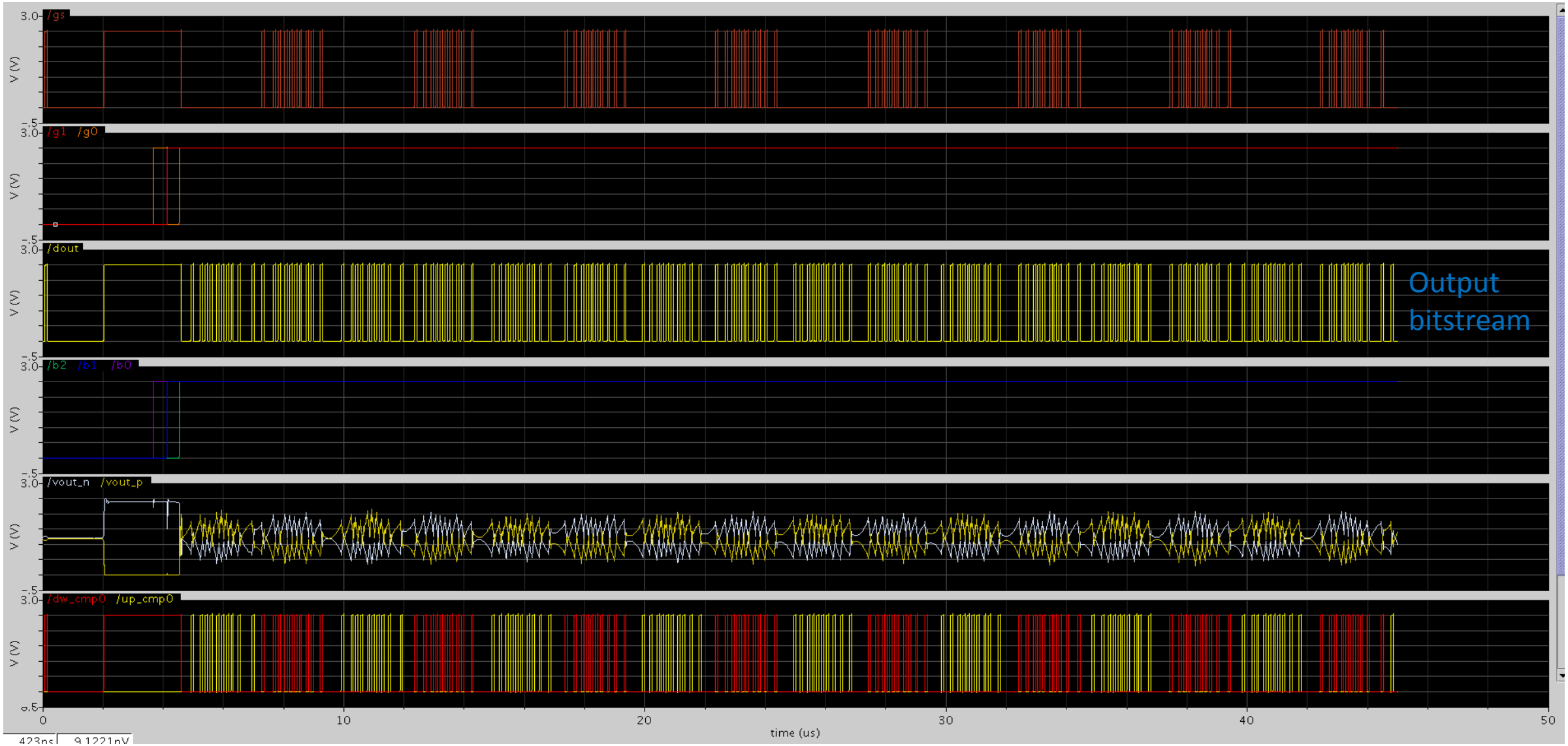
Adaptive CFC

Used in V1.0 and V2.X

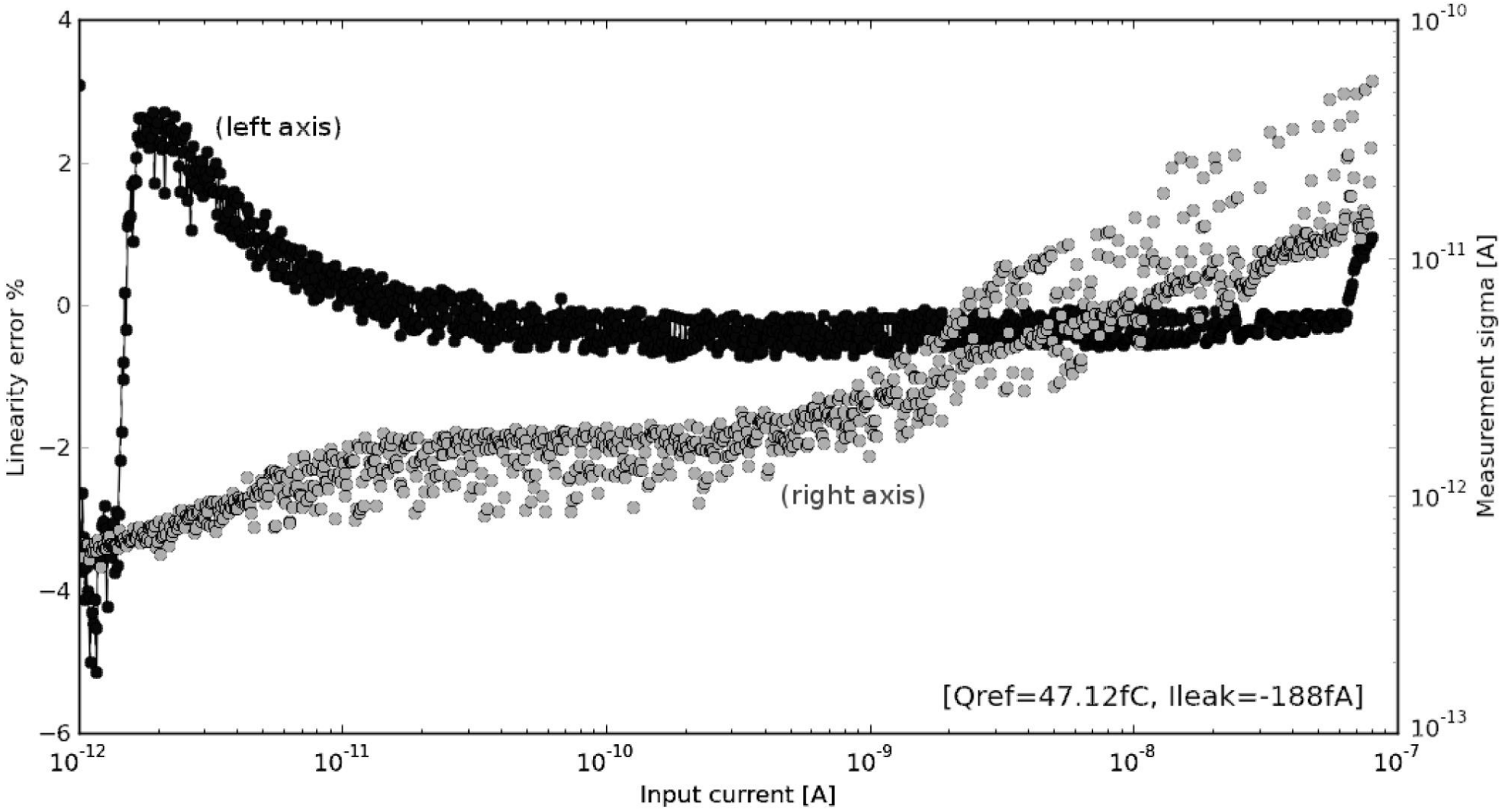


- Dynamic range is divided in 4 sub-ranges
- For each range the logic selects the appropriate values for
  - Feedback capacitor
  - Discharge current
- Fully differential architecture guarantees good noise rejection
- Reinjection of charge when disconnecting a capacitor
- Requires 2 additional bits to be sent to have information on the range
- Digital logic decides when to switch based on the input current

Waveform example - CFC

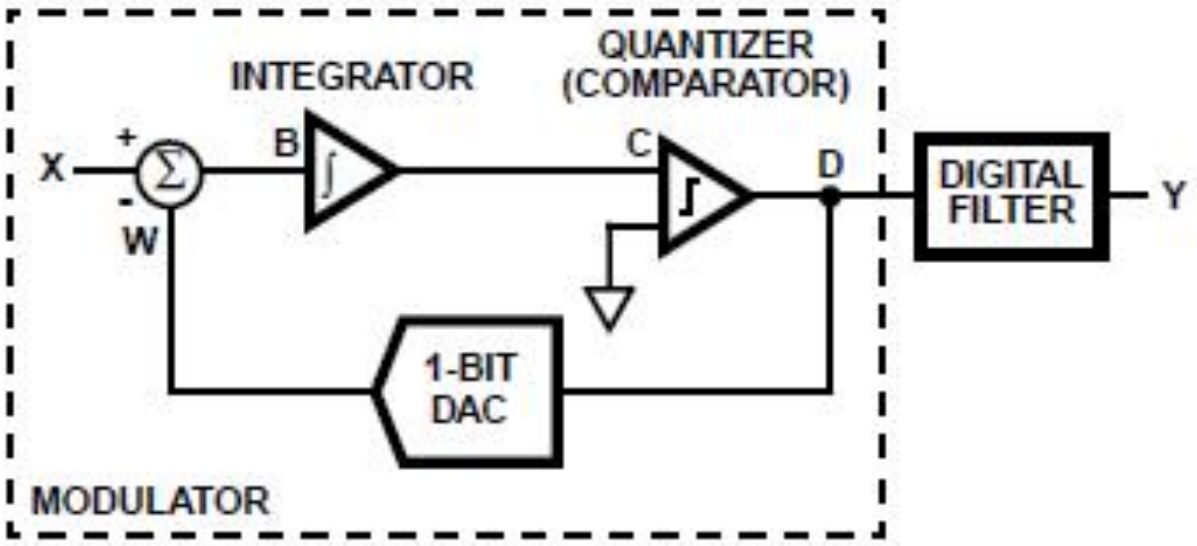


Test results



Ref: G. Venturini et al, A 120 dB dynamic-range radiation-tolerant charge-to-digital converter for radiation monitoring, Microelectronics Journal, vol. 44, Issue 12, 2013 https://doi.org/10.1016/j.mejo.2013.08.020

Architecture 2: Delta-Sigma Converter



- Input current is integrated
- Value of the integrator is compared to threshold (out is 0/1) at each rising edge of the clock
- According to out, the 1-bit DAC subtract a certain amount of charge from the input
- Over time, the “average” of the output follows the input
- The output bitstream is “decimated” by a digital filter, implemented in the FPGA to get the value of the input

Very important concept for DS: oversampling!

Implementation: Multi Bit Delta-Sigma Converter

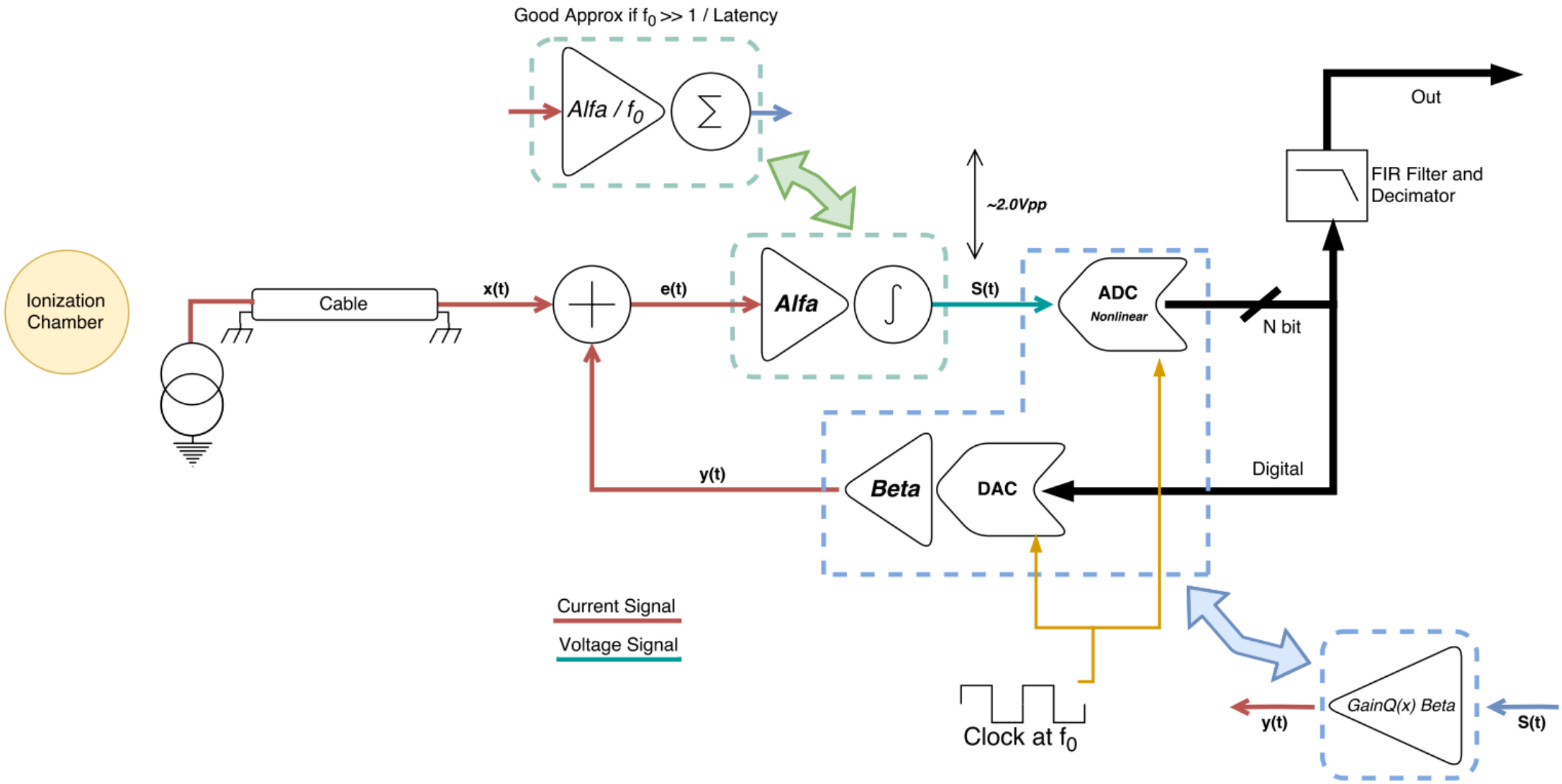
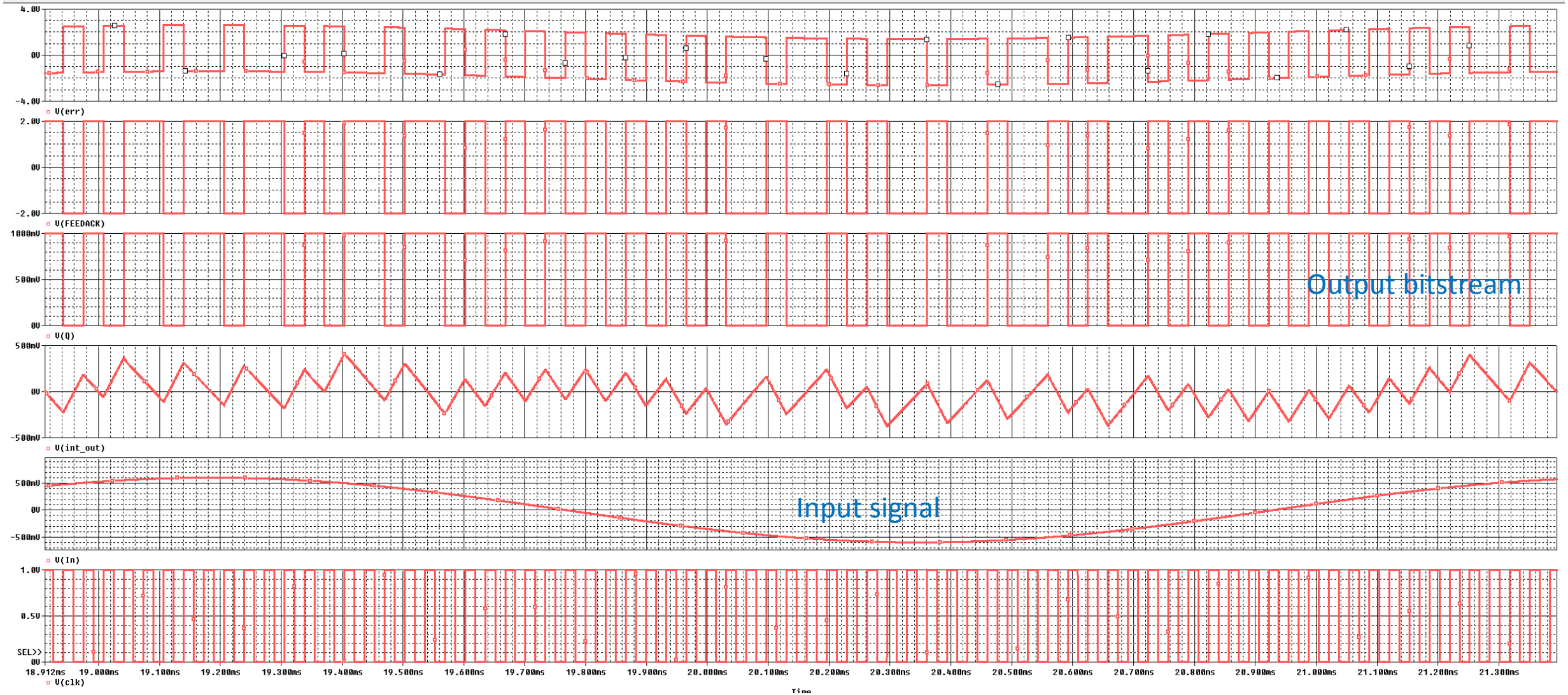


Image courtesy of F. Martina

Waveform example – 1st order DeltaSigma



Simulation results – Numerical simulations

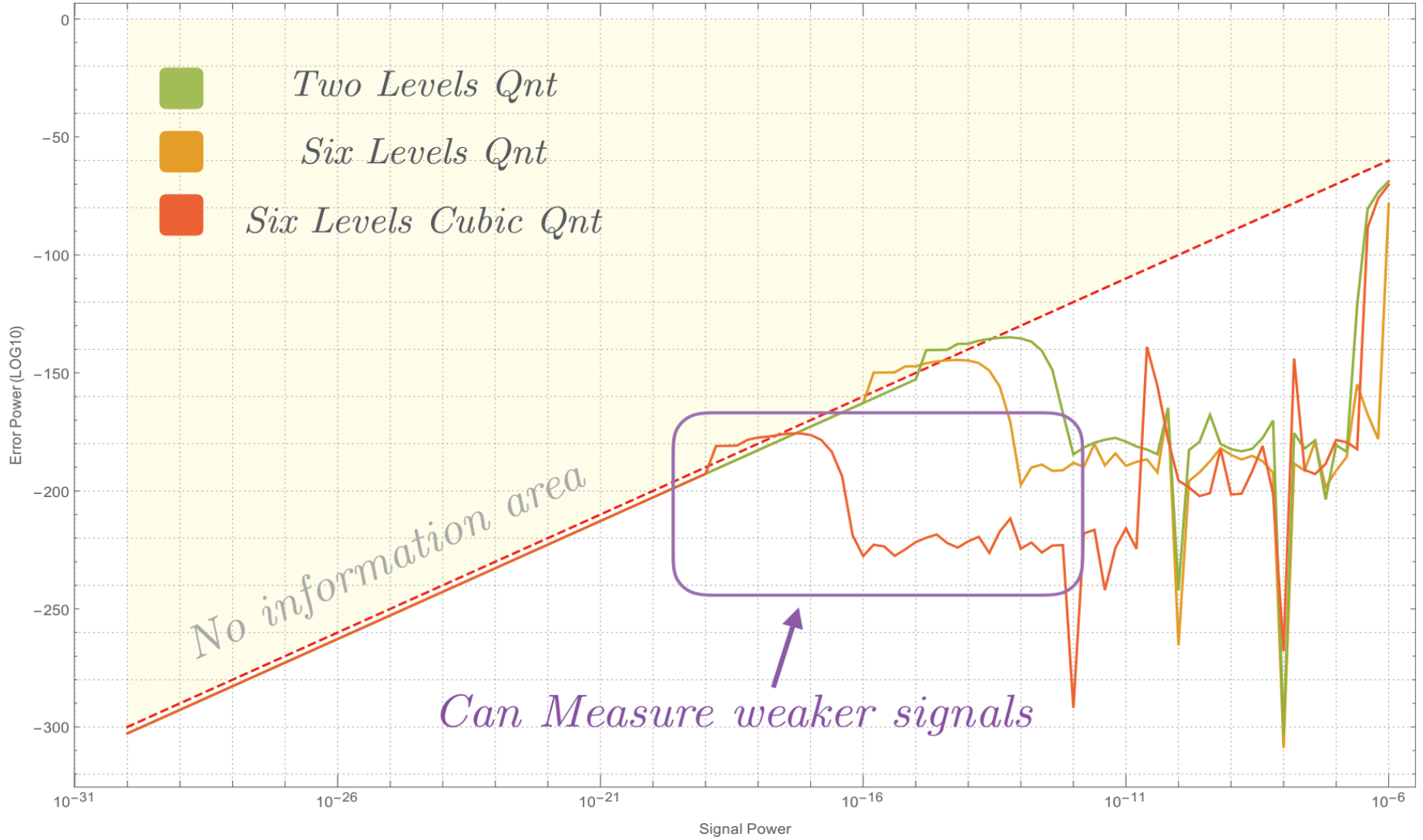


Image courtesy of F. Martina

Architectures comparison

- Bit pattern: similar – but DeltaSigma has higher frequency
- In both cases (CFC with multiple threshold or Multi-bit DeltaSigma) we need to send out of chip additional bits to have the information about the charge subtracted
- CFC requires a Digital State Machine, while DeltaSigma is “self-adjusting”
- Both architectures require radiation hard techniques, but DeltaSigma is less prone to digital problems (SEU)
- There is a bit pattern for DeltaSigma with zero input current (no need to inject a current to trigger the frontend?)
- Charge subtraction in the CFC happens only when the signal is over threshold at the rising edge of the clock while it is “continuous” in the DS.

Planning

Target: submit chip to foundry in 1 year, i.e.: April 2018

April	May	June	July	Aug.	Sept.	Oct.	Nov.	Dec.	Jan.	Feb.	march	April
System level studies		Transistor level design and simulations				Layout and simulations						Signoff

A bit optimistic, but currently on track!

Bonus: implement a discrete-component version of the DeltaSigma architecture.

Cons: might create a delay

Pro: will give insights on the “real world” problems that the final circuit might encounter and we might be able to plan in advance for those issues (plus: proof of principle, which is always good).


THANKS FOR
YOUR ATTENTION
QUESTIONS?
NO?
GREAT BYE

CFC: design values

Range	Min. I (A)	Max I (A)	Feed. C (pC)	Ref. charge	Thr. Volt.
0	$1*10^{-9}$	$256*10^{-9}$	0.32	0.04	0.125
1	$160*10^{-9}$	$4.1*10^{-6}$	2.56	0.64	0.25
2	$2.56*10^{-6}$	$65.5*10^{-6}$	20.5	10.24	0.5
3	$41*10^{-6}$	$1*10^{-3}$	164	163.84	1