Upgrade of the ATLAS Tile Calorimeter for the High Luminosity LHC

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ATLAS Tile Calorimeter System

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Introduction

Motivations for the TileCal LHC phase-II upgrade

- At High Luminosity LHC (HL-LHC, 2026), the instantaneous luminosity will increase by a factor 5-7 (~200 p-p collisions per bunch crossing)
  
  ==> increased particle flux through TileCal (2 to 24 Gy for 4 ab^{-1} integrated luminosity)

- Readout electronics is ageing due to operation time and to radiation.

- Current readout architecture is not compatible with the new fully digital TDAQ system of ATLAS and with the timing requirements for trigger and data flow.

- Detector components (steel absorbers, scintillating tiles, fibres and almost all the PMTs) will not be replaced, but detector optics robustness has to be assessed.

Strategy for the upgrade

- Adopt some general concepts for detector upgrades of the LHC experiments:
  - use electronics parts tolerant to the expected radiation level.
  - readout electronics architecture to sustain the higher trigger rate (> 1MHz) and larger event buffer (>10 μs)
    
    ===> move buffers and pipelines off detector and read out at 40 MHz (LHC crossings)

- Improve reliability through redundancy to limit the impact of component failures.

- Replace optics parts which may have intolerable response loss at HL-LHC, about 800 PMTs of 10,000 in TileCal, reading-out the most exposed detector cells (largest average anode current)
TileCal in the ATLAS experiment

- 2 WLS fibres per tile
- 2 PMTs per cell
- WLS fibres are grouped in bundles to form:
  - readout granularity of 0.1 x 0.1 (η,φ)
  - 3 radial sectors
    1.5, 4.1, 1.8 λ₀ deep
- Resolution:
  \[
  \frac{\sigma}{E} = 50\%/\sqrt{E} \oplus 3\%
  \]
- Coverage:
  0.8 < |η| < 1.7 (EB)
  |η| < 1.0 (LB)
Mechanics: “Drawer” and “Mini-Drawer” concepts

LHC architecture (Long Barrel)

Mechanical structure hosting up to 48 PMTs and the full drawer readout electronics

HL-LHC architecture

4 identical structures (Mini-Drawers MD) hosting 12 PMTs with independent readout electronics and HV and LV distribution

Mini-drawer design purposes:
- Easier maintenance
- Better compliance with ALARA
- Better robustness through modularity
TileCal readout architecture

New HV active dividers will be used in the PMT block
Non-linearity response below 1% up to 100 µA anode current
Front-End boards

• 3 different options proposed, developed and compared in lab tests and at the test beam

1) **New “3-in-1” card** (evolution of the present FE board, U. Chicago):
   - Rad hard discrete components;
   - Shaped pulse and high precision slow integrator
   => accurate luminosity measures in Van der Meer energy scans

2) **“QIE”** (ANL project):
   - ASIC chip
   - gated integrator and ADC

3) **“FATALIC”** (Clermont-F.):
   - ASIC chip
   - Current conveyer and ADC

**Down-selection process completed in 2017 fall, “3-in-1 option selected”**
Main Board (v3)

Version for the “3-in-1” FE card:

• 4 sections, each served by a FPGA

• 3 PMTs served by 1 section with:
  - 6 chs. of 40 Msps 12-bit ADCs (low and high gain)
  - 3 chs. of 50 KHz 16-bit ADCs for the slow integrators.

• Distribute the slow control commands to the FE cards.

• Manage charge injection calibration and remote system configuration

• Physically divided into 2 parts with independent powering from POL regulators receiving +10V from LVPS bricks in “Diode-Or”
Daughterboard (V4)

• Receives TTC signals and slow control commands from the back-end Pre-Processor (PPr) module
• Distributes signals and commands to the Main Board (MB) and to the HV board
• Collects/concentrates ADC data from the MB
• Transmits data over optical links to the PPr (40 Gbps required, 80 Gbps per board in redundancy)
• Divided in 2 sections which can be operated independently, each section serving up to 6 FE channels
• Communication with MB through a 400 pin FMC connector
• Interface with the PPr through redundant QSFP connectors
• System managed by 2 Kintex-7 FPGAs
• 2 GBTx chips used to manage the system clock and FPGA remote configuration

Latest DB version V5 design & prototyping:
• FPGAs: Kintex7 -> Kintex Ultrascale+
• Two QSFPs replaced with four 850 nm multimode SFPs
• First prototypes available
Pre-processor (PPr) and TDAQ interface (TDAQi)

- Design of the full-scale PPr is being finalized (8 SD (Tile modules))
- Each PPr consists of:
  - One customized ATCA carrier
  - Four Compact Processing Modules (CPM)
  - One TDAQi RTM (Rear Transition Module)
  - Optical transceivers with multimode fibres
- 1st prototype (1/8 of the full-scale) extensively tested at the past test beams
- 2nd prototype to be integrated with a FELIX (Front-End LInk eXchange)

CPM main functionalities:
- Communication with the front-end (FE) for control, configuration and monitoring.
- LHC clock recovery and distribution to the FE
- Remote configuration of the FE electronics FPGAs
- High speed data reception from the FE and storage in pipeline memories
- Data calibration and processing (cell energy calculation) in real time every bunch crossing.
- Extraction from pipelines data of triggered events to be sent to the FELIX through the TDAQi
- Transfer data to the Trigger FPGA in the TDAQi

TDAQi main functionalities:
- Synchronous reception of cell energy
- Calculation of trigger objects (trigger towers or group of cells of different eta/phy size)
- Making copies of the trigger objects
- Synchronous transmission of trigger objects data and copies to the different trigger systems
- Sending readout data of triggered events to the FELIX

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High Voltage power supplies

Two options under evaluation, different location of the distribution and monitoring electronics

“Remote” option (baseline)

- HV bulk power supplies and regulators installed in the Atlas service cavern (USA15)
- Requires 100 m long HV wires for each individual PMT.
- Advantages: easy maintenance, no radiation hardness issues
- A 12 channel prototype used at the test beams
- HV cables with higher density wire bundles from different companies under test → Challenge is fitting and routing large volume cables with big HV connectors

“Internal” option (back-up)

- HV bulk power supplies in the underground service cavern, but regulators on-detector
- Individual channel control through the DaughterBoard
- Advantage: reduced number of HV cables (only one HV cable per module (SD))
- Operational and used at the test beams
Low Voltage power supplies

A three stage power system based on the current LVPS design

Improvements:
• Better reliability, lower noise
• Improved radiation tolerance
• Lower number of connections
  - One DC level (+10V) and POL regulators for the voltages needed by the local circuits
• Redundant power distribution
  - 2 individual “bricks” per mini-drawer
  - Redundancy control with diode “OR” in the mainboard

Voltage adjust and controls through the new ATLAS slow control system (ELMB++ or ELMB2)
-- Each individual brick requires remote on/off control

8 bricks (1 SD) assembled in a box located in the Tile drawer extension (“finger”)

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Test beam campaigns

• Test beam campaigns very useful to test and to integrate the different components of the demonstrator.

• Five campaigns of 2 weeks between 2015 and 2017 with three detector modules equipped with different readout systems:
  - 1 Long Barrel and 1 Extended Barrel modules with legacy readout electronics
  - ½ Long Barrel module with the new “3-in-1” FE option for the upgrade (Demonstrator)
  - ½ Long Barrel Module with the other FE ASIC options (“FATALIC” and “QIE”)

• Results shown in next talk (A. Rodriguez Perez).

• Demonstrator readout with the ATLAS TDAQ SW allowing for:
  - Front-End configuration
  - Physics and calibration (Caesium source and laser) runs

• Two more test beams scheduled during 2018 (May and November) with the following program:
  - Integration of the real ATLAS FELIX in the TDAQ software
  - Test of the last Daughterboard version (V5)
  - Test of the full-size PPr prototype
  - Test of the “remote” HV option with cables with higher density wires
  - Test of the mechanics option (micro-drawers μD) for the extended barrel
    --> increased modularity only for the mechanical structure (1 SD = 3 MD + 2 μD)
Test beam set-up (2017)

H8 beam facility in the CERN North Area

Tested modules mounted on a movable platform

- The super-drawer (Demonstrator) of the long barrel LBC 65 equipped with the 3-in-1 FE upgrade option.
- The Demonstrator provides all the upgrade functionalities compared to previous electronics (Legacy Super-Drawer (SD)).
- The ASIC alternatives (FATALIC/QIE) mounted in the super-drawer LBA 65.
- The super-drawers M0 C and EBC 65 were equipped with the Legacy SD system.
- Multi-Anode PMTs (MA) on M0 A, for special tests of light collection.

“3-in-1” FE cards for the Upgrade

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Test beam 2018 readout architecture

- Kept compatibility with the present (legacy) TDAQ architecture in the “Demonstrator”

- Added a full upgraded readout system to an Extended Barrel module

- Link bandwidths:
  - From Mainboard to Daughterboard: 560 Mbps for each channel and gain
  - Daughterboard to PPr (including redundancy for each mini-drawer):
    - Uplink (DB—>PPr) : 8 links @ 9,6 Gbps
    - Downlink(PPr—>DB): 4 links @ 4,8 Gbps
  - PPr to ROD (legacy readout) :
    - 1 link @ 640 Mbps
  - PPr to FELIX: 1 link@ 4,8 Gbps

With DB_v5 the data links between PPr and DB will be reduced by a factor of 2 ( 4 uplinks, 2 downlinks)
• Full replacement of the readout PMTs of TileCal not foreseen.
• Time evolution of the response studied for the most exposed and special cells of the detector.
• Observed a down drift of the PMT response during p-p collision periods, with a partial recovery during shut-downs.
• Made a two-exponential model for the PMT response loss as a function of the anode integrated charge.
• Only a small fraction of the PMTs (8% of 10,000) for cells in the inner layer A will lose more than 30%. They will be replaced with last and improved version of the same PMT type.

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## TileCal phase-II upgrade: medium term program

<table>
<thead>
<tr>
<th>Year</th>
<th>Quarter</th>
<th>Event</th>
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<tbody>
<tr>
<td>2017</td>
<td>Q1</td>
<td>IDR</td>
</tr>
<tr>
<td>2017</td>
<td>Q2</td>
<td>FEB choice</td>
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<td>2017</td>
<td>Q3</td>
<td>TDR submitted</td>
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<tr>
<td>2017</td>
<td>Q4</td>
<td>DB V5</td>
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<tr>
<td>2018</td>
<td>Q2</td>
<td>Test beam</td>
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<tr>
<td>2018</td>
<td>Q3</td>
<td>Full-size PPr</td>
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<td>2018</td>
<td>Q4</td>
<td>Final Design Reviews during 2019</td>
</tr>
<tr>
<td>2019</td>
<td>Q1</td>
<td>Demonstrator insertion in TileCal?</td>
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#### LHC Timeline

- **Run 1**: 2011-2014
  - LS1: Splice consolidation, button collimators, RSE project
- **Run 2**: 2015-2018
  - LS2: Injector upgrade, cryo Point 4, DS collimation, P2-P7, T1 T dip., Civil Eng., P1-PS
  - LS3: HL-LHC installation
- **Run 3**: 2019-2023
  - LS1: Experiment beam pipes, nominal luminosity
  - LS2: Experiment upgrade phase 1
  - LS3: HL-LHC installation
  - Run 4-5...
  - LS3: 5 to 7 x nominal luminosity
  - LS3: Experiment upgrade phase 2
  - 3000 fb^-1 integrated luminosity
- **Run 4-5...**
  - 3000 fb^-1 integrated luminosity

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Summary

- A wide R&D program for the new TileCal readout electronics for HL-LHC is progressing well
  - Prototypes of all elements of the full readout chain intensively tested
  - Continuous tuning of the new versions of each component prototype of the FE and BE electronics.
  - Full-size PPr and TDAQi (interface to the future ATLAS TDAQ) prototypes ready this summer
  - LVPS ready for pre-production
  - Evaluating 2 HV distribution architectures (HV “remote” option is the baseline)
  - Radiation hardness tests for all elements of the system on-going or ready to start
- New super-drawer mechanics design completed, prototypes available including the micro-drawer option for the Extended Barrel and the new drawer extraction system.
- Studies on PMT lifetime and robustness in progress, made projections to the HL-LHC era.
- In general, high reliability of the upgraded system will be achieved through redundancy, modularity, and robustness.
- Five test beam campaigns from 2015 to 2017 and two more in 2018.
- Steps of the TileCal upgrade roadmap to HL-LHC on the time schedule.
Back-up
TileCal cell geometry

Istantaneous Luminosity to PMT anode current conversion coefficients

ATLAS Preliminary
Tile Calorimeter
Data 2016

ATLAS Preliminary
Tile Calorimeter
Data 2017

$\eta_{\text{cell}}$

$\eta_{\text{cell}}$
Mechanics for the new module drawers

- New mechanics and extraction tools
  - Simplify the handling during maintenance
  - Allow access in reduced detector standard opening
- Each module hosts 4 mini-drawers:
  - 12 PMTs + 12 Front-End cards (3-in-1 cards)
  - 1 MainBoard + 1 DaughterBoard
  - 1 HV regulation board: Internal or Remote option
  - 1 adder base board + 3 adder cards (only for the Demonstrator)
- 1 LVPS: low power distribution for readout electronics
- Mini Mini-Drawer proposal for Extended modules under study
  - Only 32 PMTs in Extended modules
    (10 PMTs in MD3 and MD4)
  - Proposal: 3 MD + 2 MMD using 3 sets of electronics boards
New HV active dividers in the PMT block

Deviation from response linearity (%)

Passive dividers

New active dividers

Feedback transistors inserted in the last amplification stages
“QIE” ASIC based option for the FE cards

- The core is QIE 12 ASIC, some of COTS devices in advanced technology used for slow control and calibration purpose

  → LVDS/LVCMOS buffers, DACs, SAR ADCs, OPAMPS, and Mux

- The QIE splits the PMT output current in 4 ranges, each has a corresponding gated integrator and 7-bit ADC. Combining the 4 ranges, QIE presents 17-bit dynamic range with non-linear transfer function
The FATALIC ASIC design has a current conveyor with outputs with a gains ratio of 64:8:1, each followed by an RC shaper to handle the PMT signals.

- Three 12-bit ADCs in parallel to digitize the outputs from current conveyor.
- Combined dynamic range is 17-bits.
- Auto-selection data readout with medium gain + (Low or High gain).
- ASIC built in 130 nm CMOS technology operates in 1.6V, consuming 205 mW.
Daughter board version 5 architecture
Pre-processor (PPr) prototypes

Prototypes (1/8 of the full-size PPr, 1 Super-Drawer)

- 1st prototype extensively tested at the past test beams
- 2nd prototype to be integrated with a FELIX emulator
- Two FPGAs:
  - Virtex 7 + 4 QSFPs for data readout (TTC/DCS distribution to the FE, interface to FELIX, energy and time reconstruction)
  - Kintex 7 + Avago MiniPOD TX for trigger (data to L0/L1Calo, pre-trigger algorithms)
Full-size Pre-Processor

- **ATCA carrier with 4 AMC positions**
  - Modular strategy to reduce the complexity of the PCB layout → saving costs
  - Xilinx Zynq controller module
    - SODIMM form factor
    - Diagnostics, monitoring, remote programming
  - GbE Ethernet switch module
    - SODIMM form factor
    - 16 GbE ports, 1 per AMC, Zone 2, TDAQi
  - CERN IPMC mezzanine card
    - DIMM form factor
    - AMC/Blade management, sensor reading

- **Compact Processor Modules**
  - Readout and operate 2 TileCal modules
  - Single AMC form factor
  - Xilinx Kintex UltraScale FPGA
  - 8 Samtec firefly modules (up to 32 links)
  - Artix FPGA for diagnostics, clock phase monitoring

- **First prototypes expected for summer 2018**
TDAQi prototype

- Trigger and DAQ interface (TDAQi)
  - Receives calibrated cell energy from the PPr and interfaces with the trigger systems
  - Interfaces the PPr with the FELIX
- TDAQi prototype: reduced version
  - Kintex UltraScale FPGA
    - 2 SFPs, 2 Samtec Firefly, SMA connectors
  - 1 QSFP connected directly to zone 3 (signal integrity studies)
  - Rear Transition Module form factor
  - No major issues found
    - Voltages, dimensions, JTAG chain verified
  - More tests ongoing: Link qualification with Xilinx IBERT IP core