The Phase-1 Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeter

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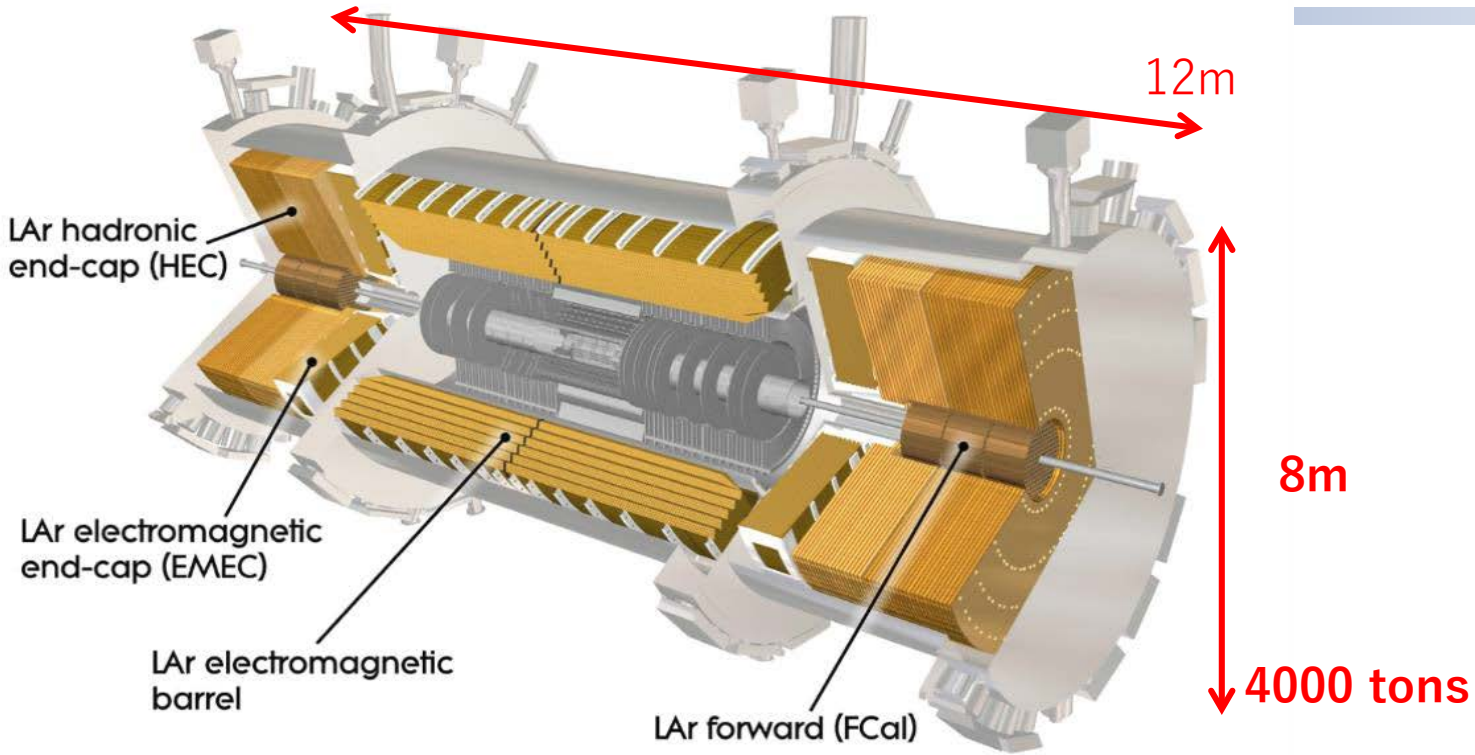
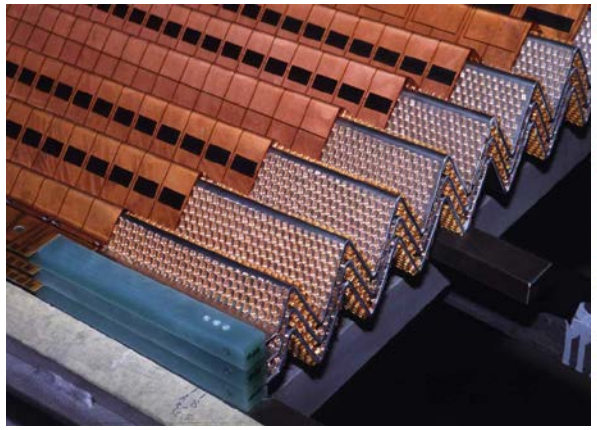
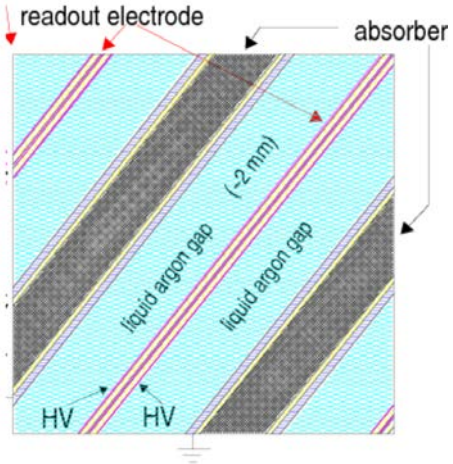
On behalf of ATLAS LAr group

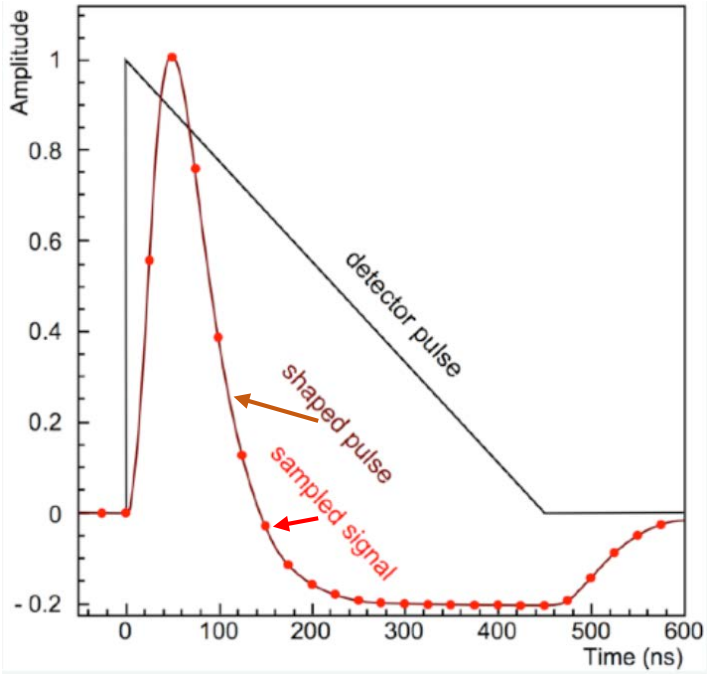
CALOR 2018, Eugine, Oregon, US 2018 May 23rd

ATLAS Liquid Argon Calorimeter









- Pb-LAr EM sampling calorimeter
  - $\sigma/E \sim 10\%/\sqrt{E} \oplus 0.7\%$
  - fine granularity: $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ (middle layer)
  - Total 22 X_0
  - 4 layers, total 180 x 10^3 channels
- e/γ trigger, ID, transverse energy

→ Essential for precise measurements, esp. Higgs physics

LHC upgrade schedule

2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2035

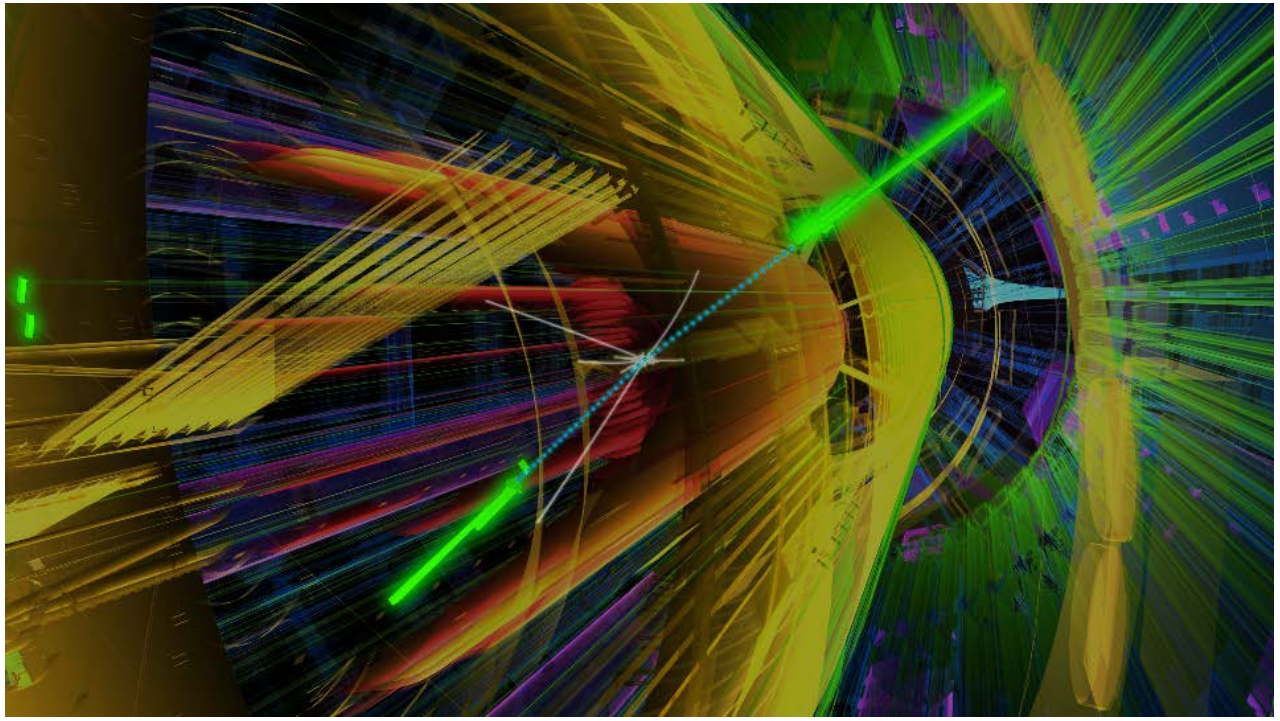
LS1	Run-2	LS2	Run-3	LS3	Hi-Lumi

$\sqrt{s} = 13$ TeV
$L = 1.7 \times 10^{34}$ cm^{-2}s^{-1}
$\int L dt = 150$ fb^{-1}
$\mu \sim 50$

$\sqrt{s} = 14$ TeV
$L = 3 \times 10^{34}$ cm^{-2}s^{-1}
$\int L dt = 300$ fb^{-1}
$\mu \sim 80$-100

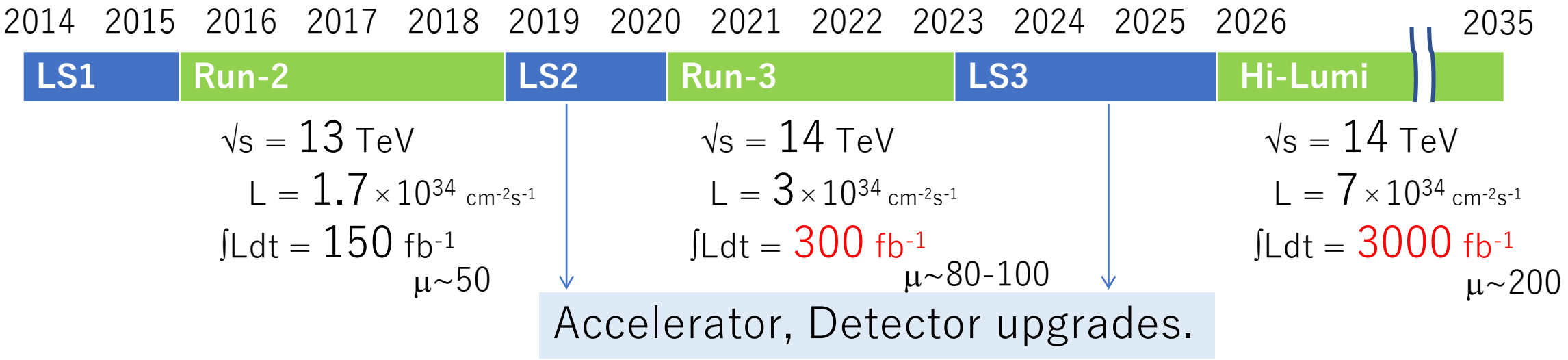
$\sqrt{s} = 14$ TeV
$L = 5\sim7 \times 10^{34}$ cm^{-2}s^{-1}
$\int L dt = 3000$ fb^{-1}
$\mu \sim 200$

Accelerator, Detector upgrades.



Event with
two photons.
(Recorded in 2014)
Aiming such clean
condition at high
luminosity runs.

LHC upgrade and ATLAS Calorimeter



ATLAS LAr Calorimeter upgrade:

LS2: Phase-1 upgrade

- **Trigger readout** upgrade
- Level-1 trigger
  100 kHz ~ latency 3 μs
- data recording rate:1 kHz.

LS3: Phase-2 upgrade

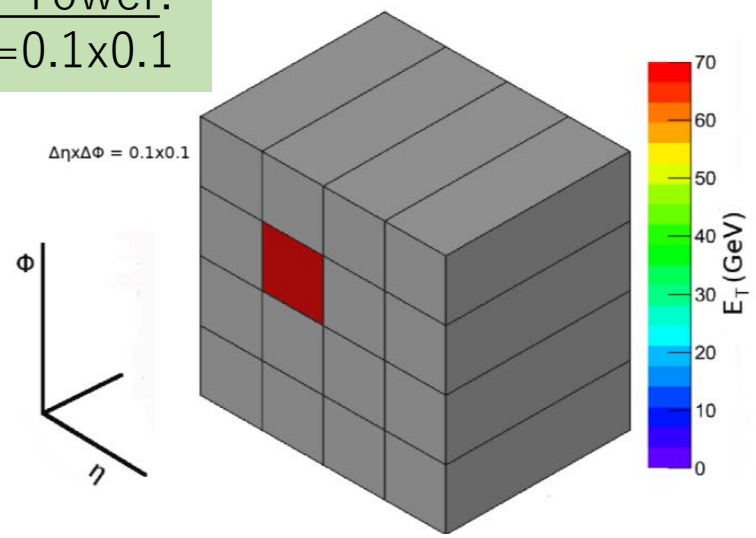
- Main readout upgrade
- Forward part detector upgrade
- Level-1 trigger
  1 MHz ~ latency 10-20 μs
- data recording rate: 5~10 kHz.

ATLAS LAr Phase-1 upgrade project

- Upgrade for Calorimeter trigger in LS2(2019-2020)

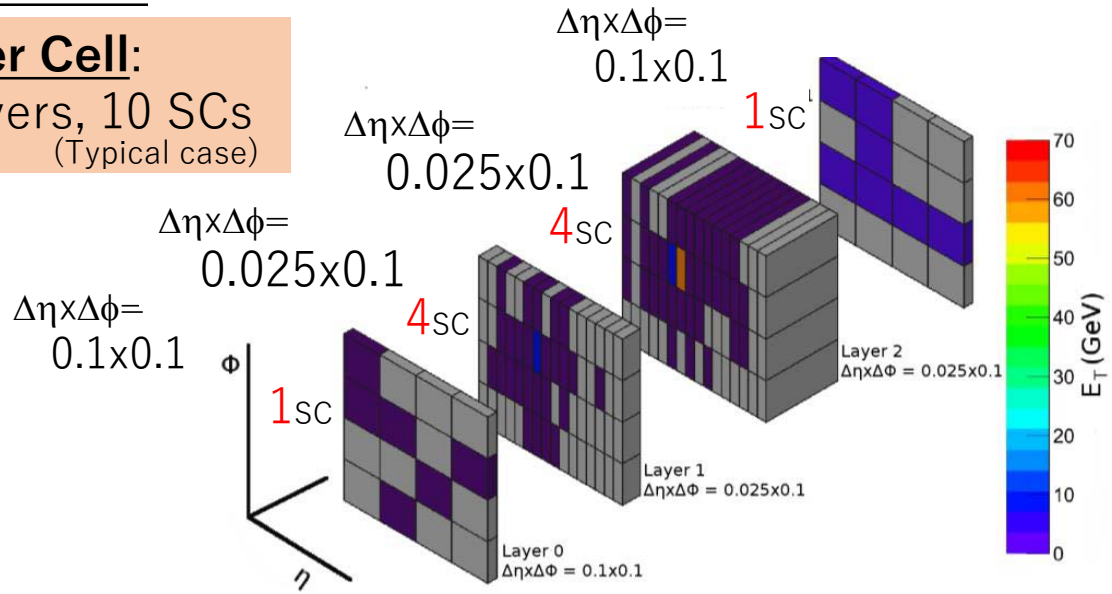
Current readout:

Trigger Tower:
ΔηxΔϕ=0.1x0.1



NEW readout:

Super Cell:
4 layers, 10 SCs
(Typical case)

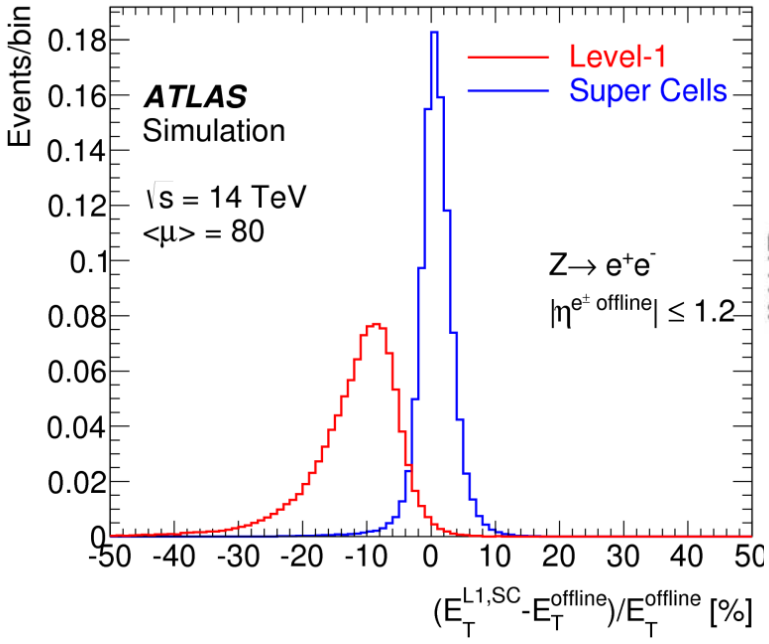


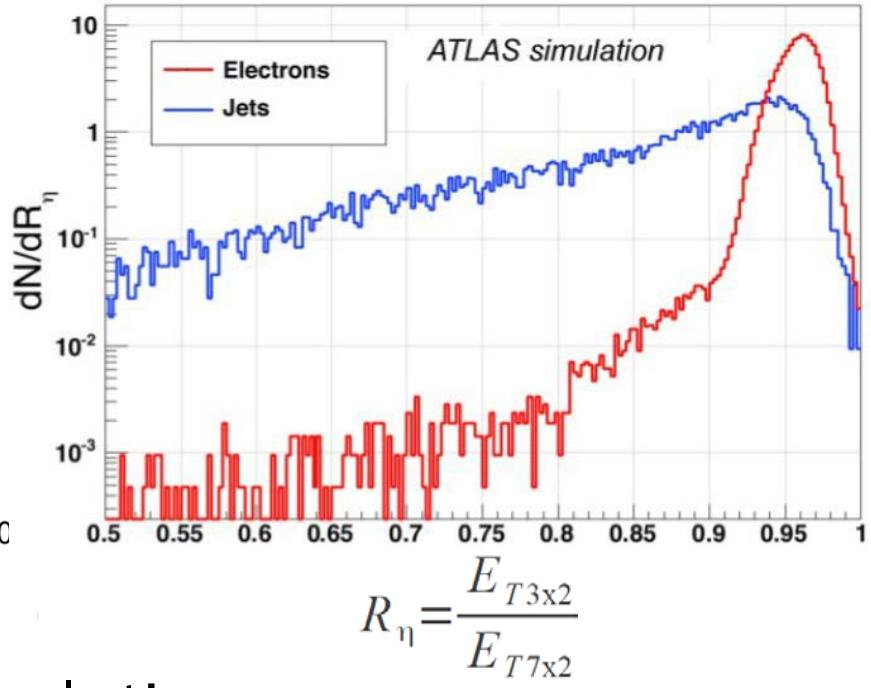
Electron with 70 GeV
Size of Moliere radius in η is ~ 0.08

- Digitize at Frontend(on-detector),
  Realtime processing at Backend (off-detector).
  → High density, high speed data transmission
  → Digital filtering on FPGA

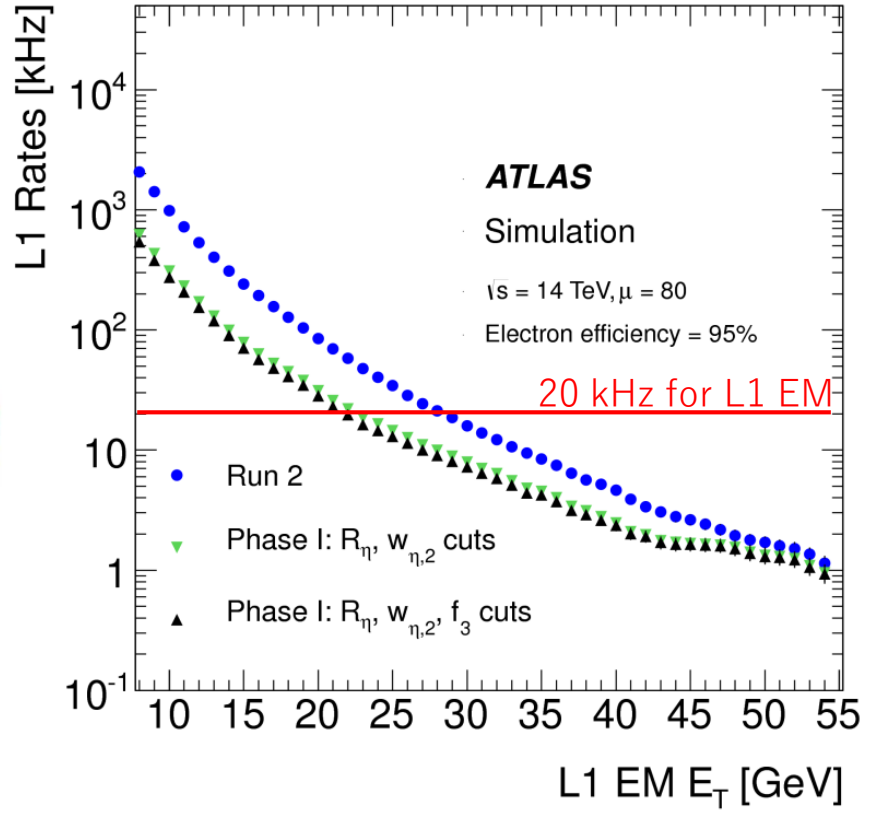
Ten times finer granularity
+
Better energy resolution
→ Higher BG rejection

Expected performance



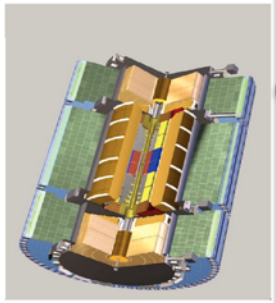


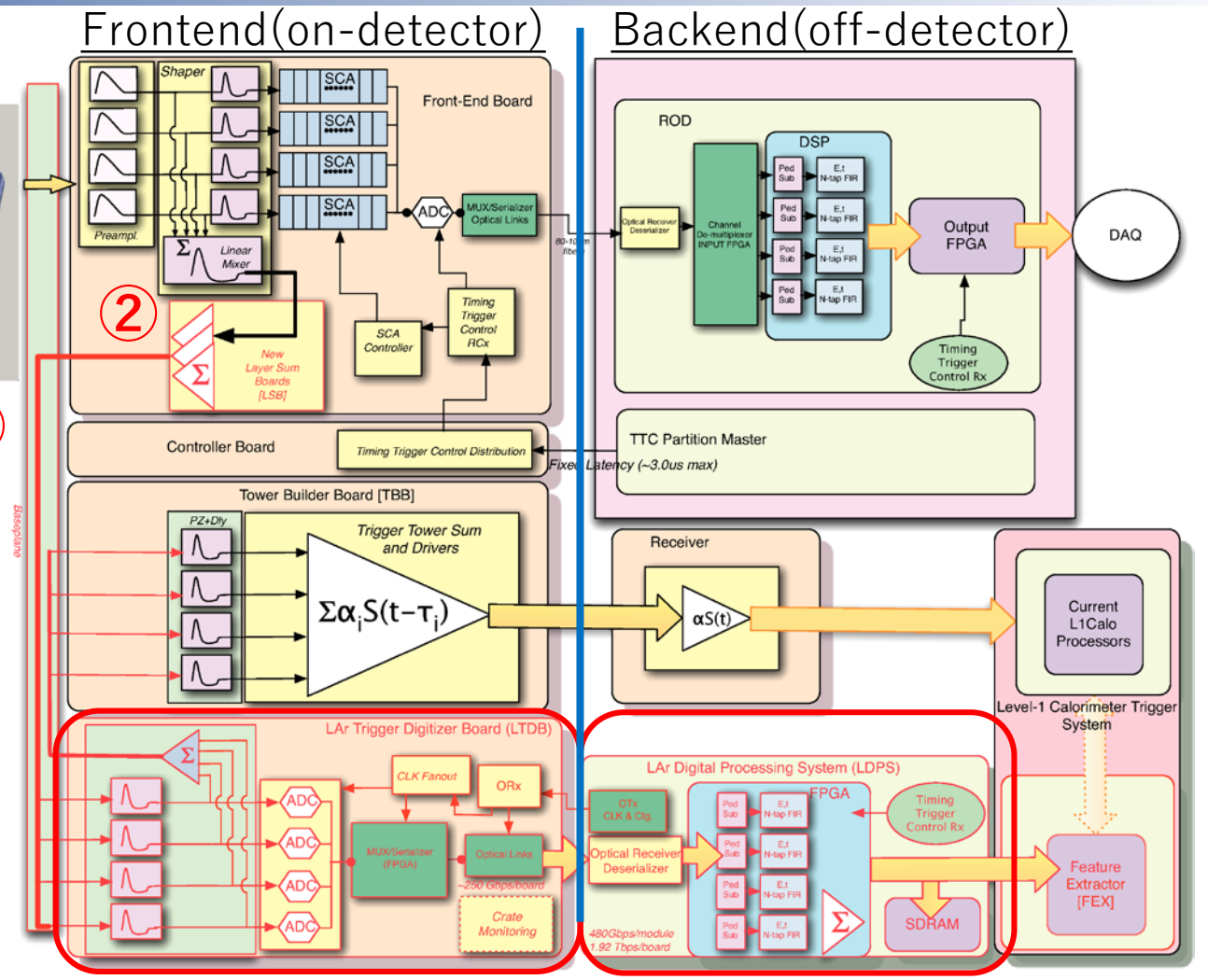
$$R_\eta = \frac{E_{T3\times2}}{E_{T7\times2}}$$



- Better energy resolution
- Better signal(EM object) to background (Jets) separation
  - Keep lower threshold within given Level-1 rate budget (20 kHz for Single EM)
- Very important for the ATLAS physics program!
  - For W→eν, Z→ee, H→γγ: Trigger on EM objects with 20-30 GeV.

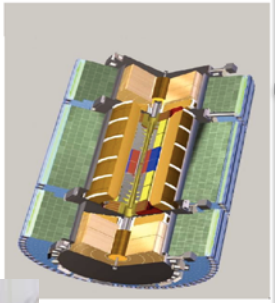
New Hardware

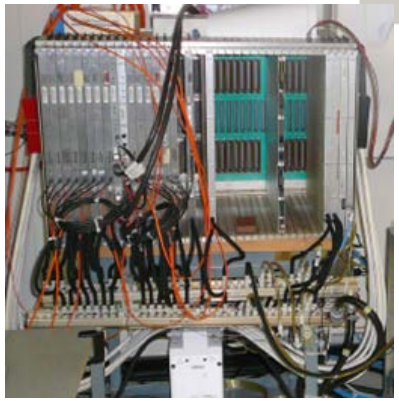


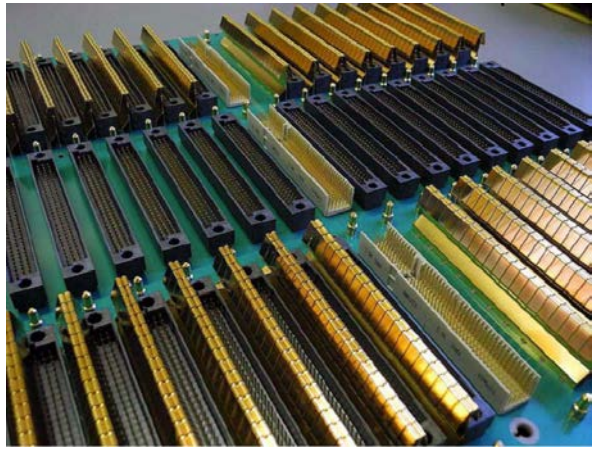


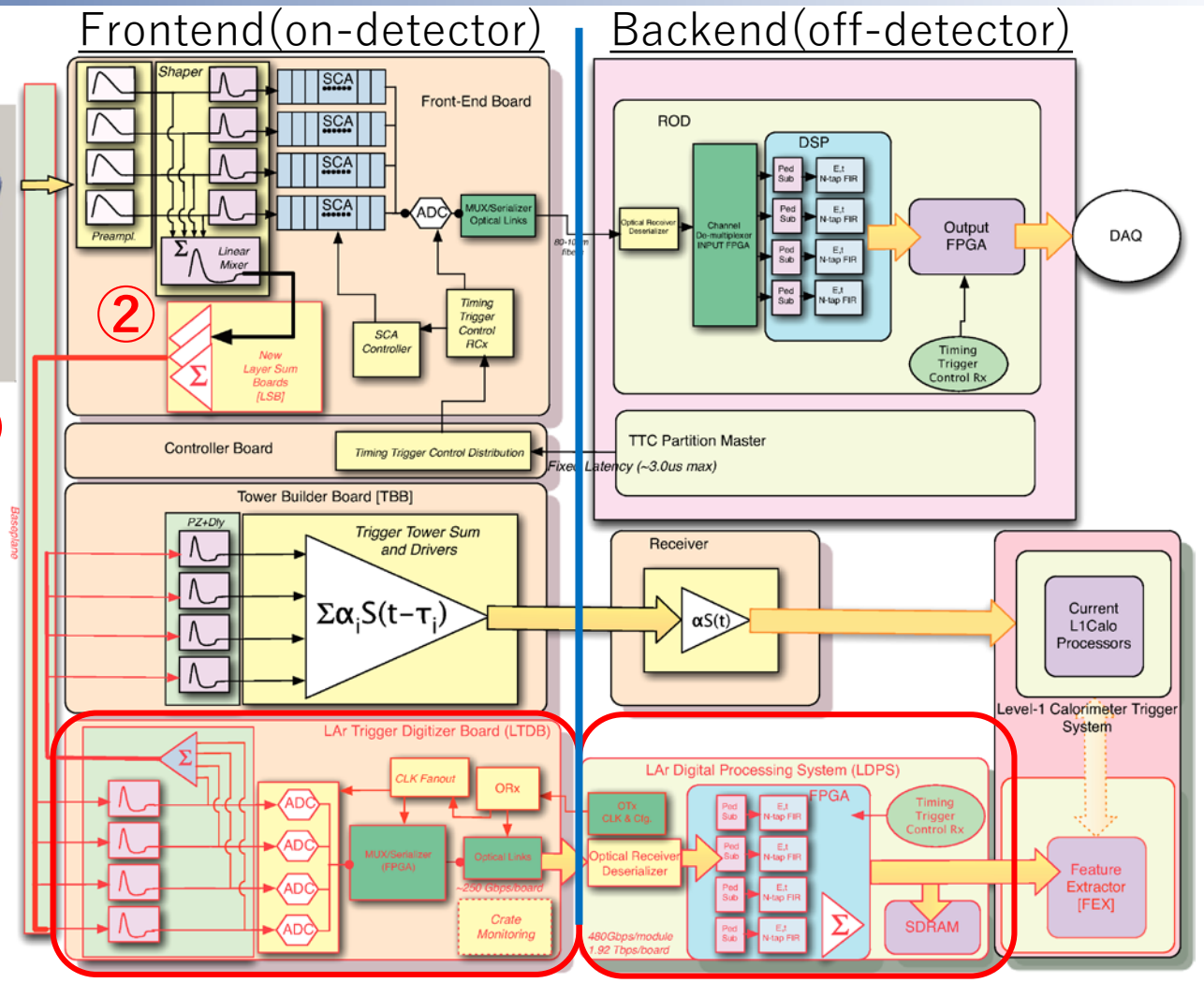
New Hardware

1. Baseplane









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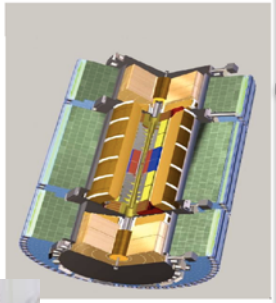
③ **LTDB** digitizer board

④ **LDPB** digitizer processing

New Hardware



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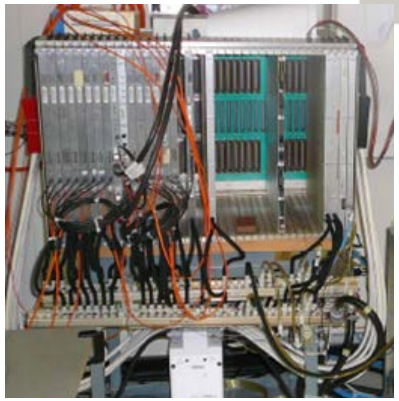
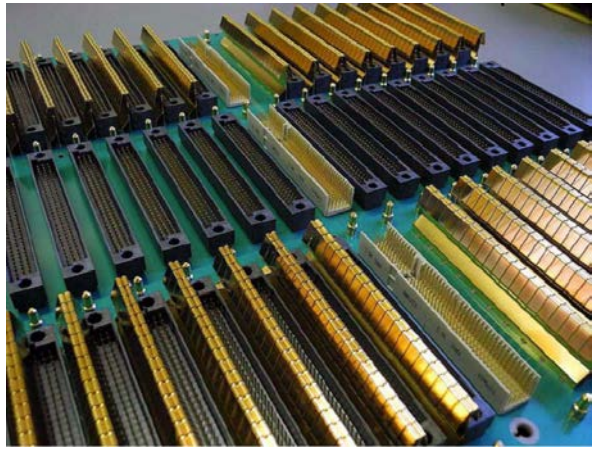
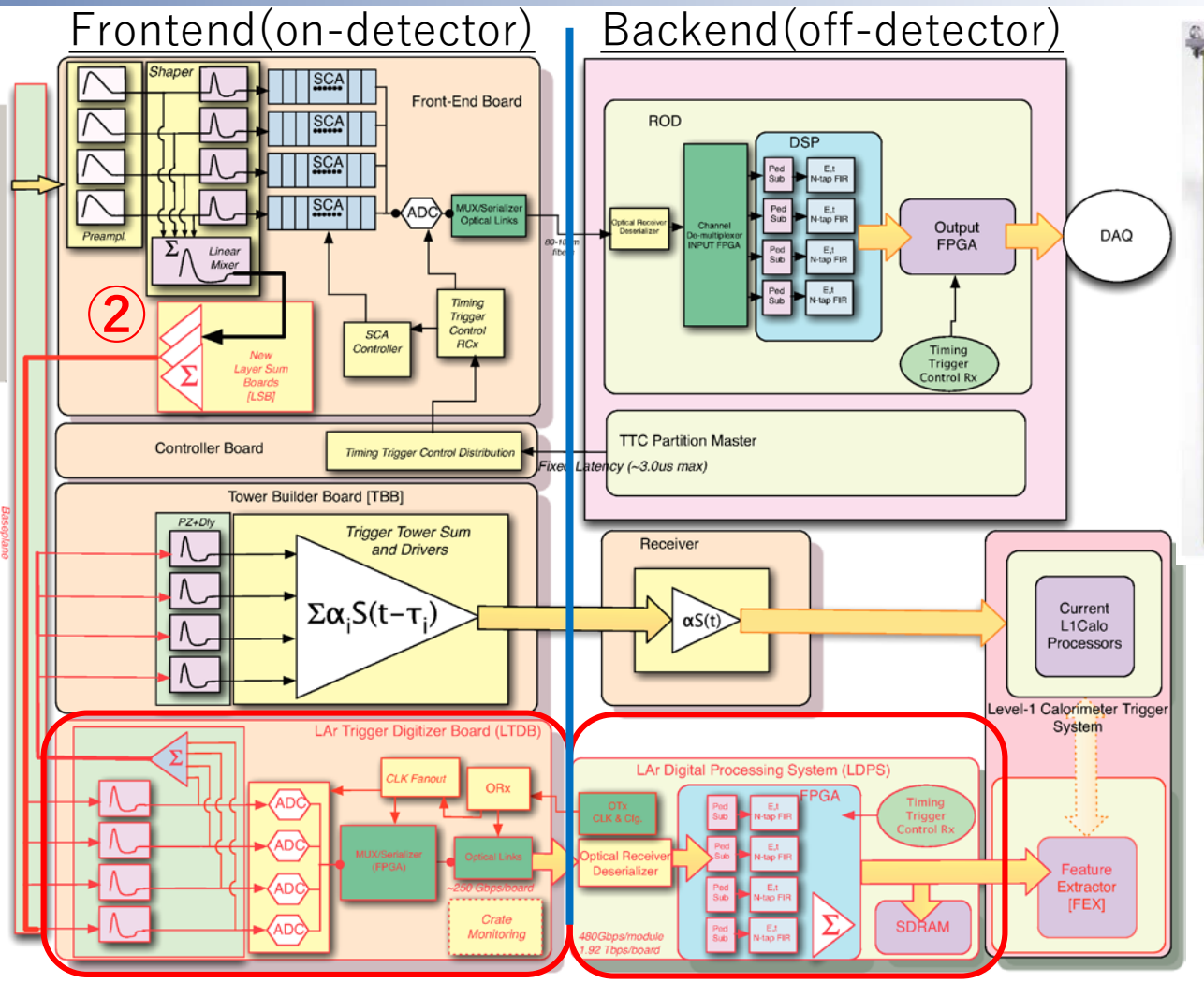
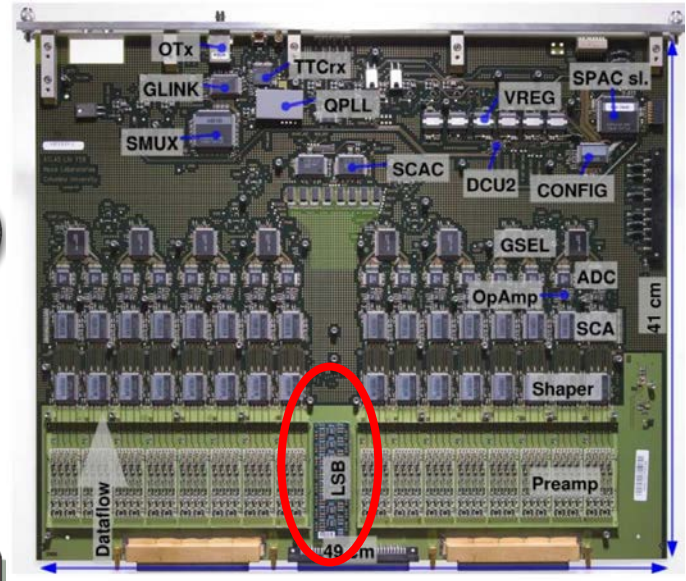


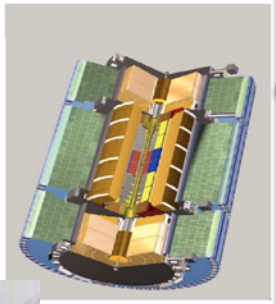






2. LSB(mezzanine)

New Hardware



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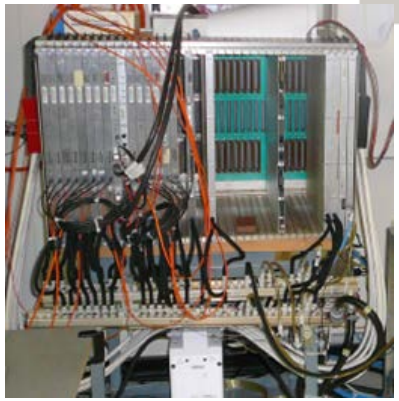

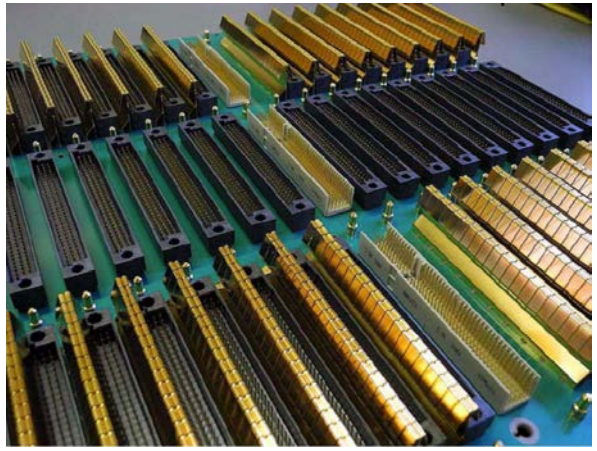

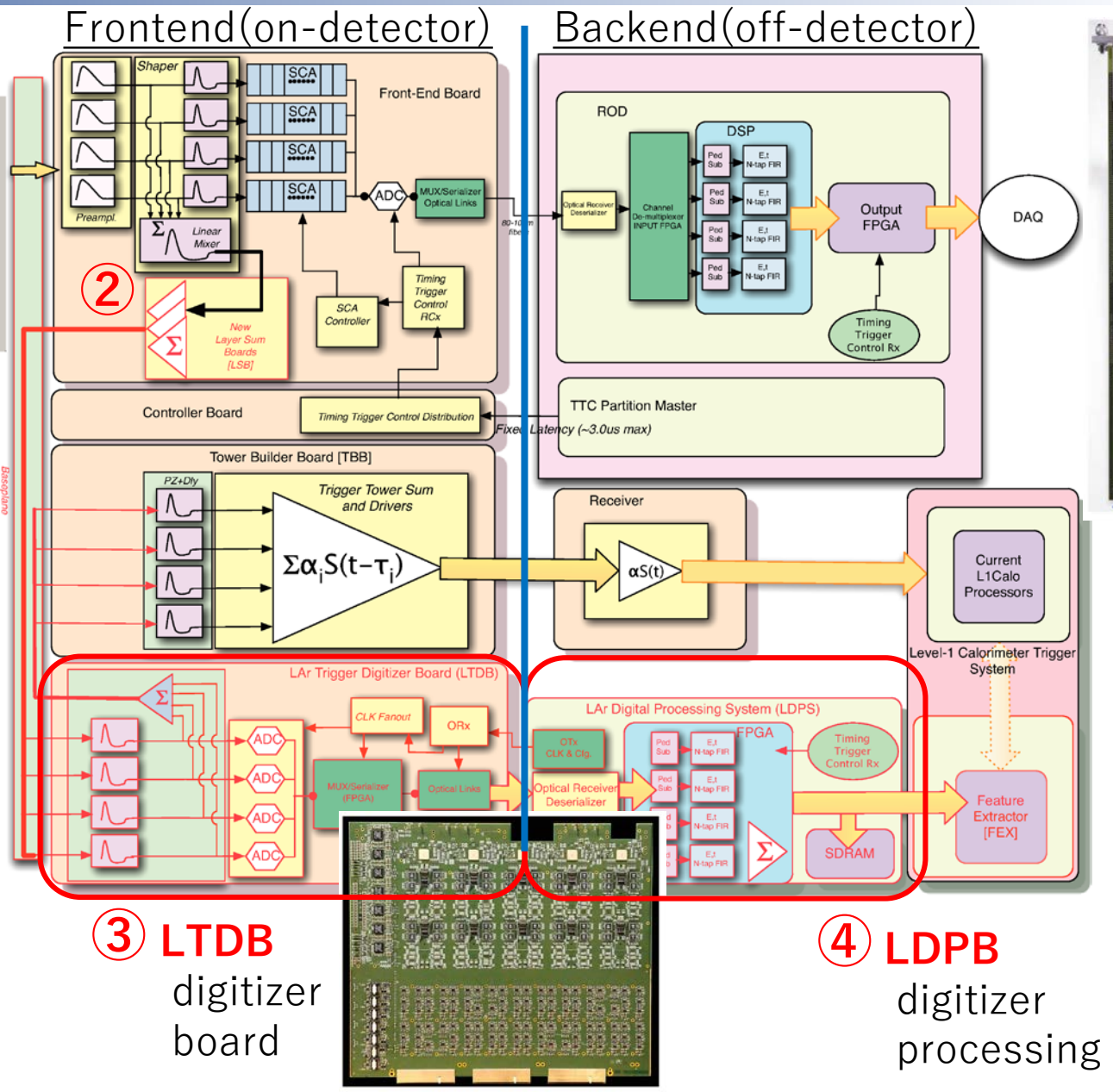

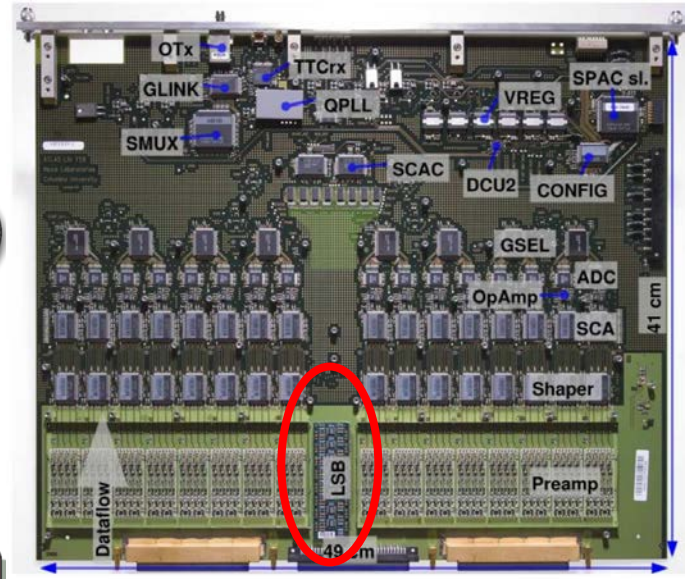

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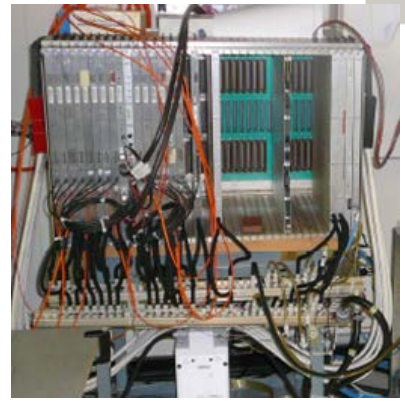

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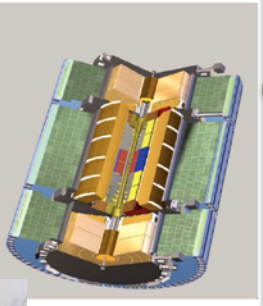

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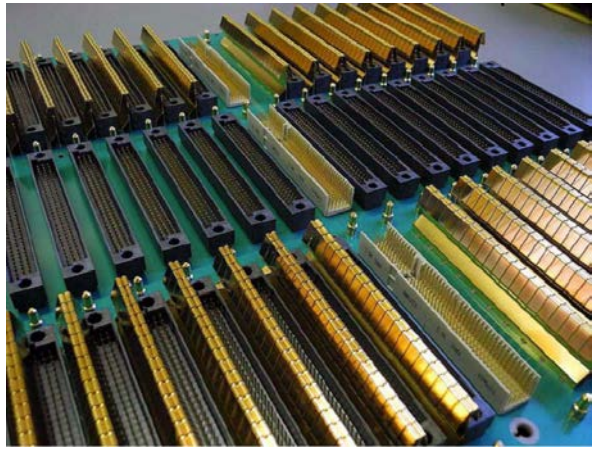
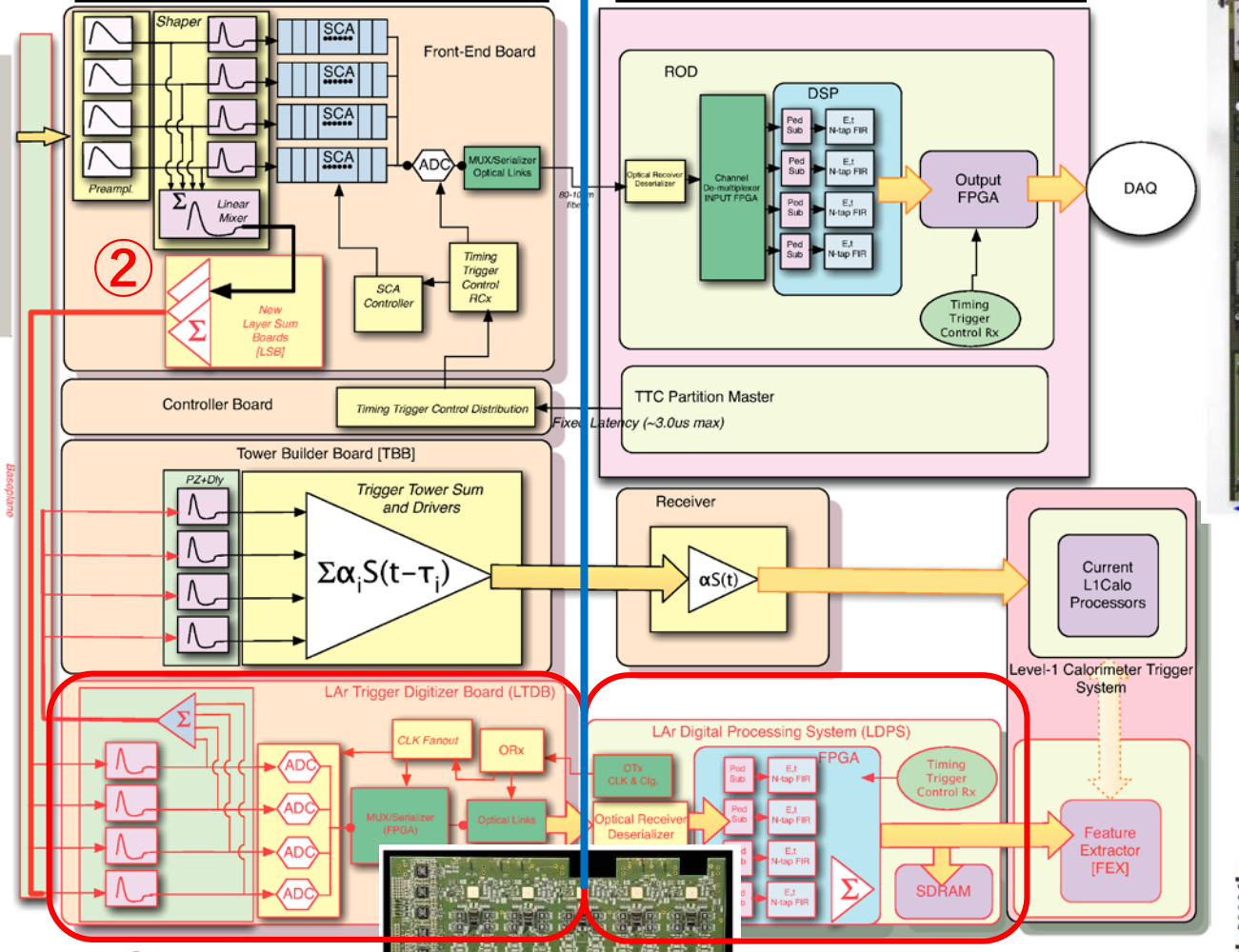
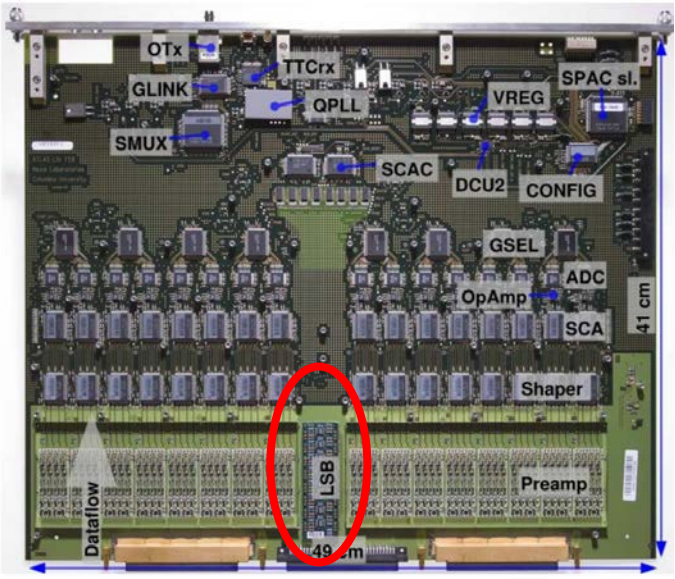


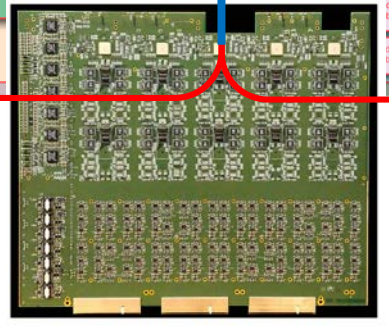
Frontend(on-detector)

Backend(off-detector)

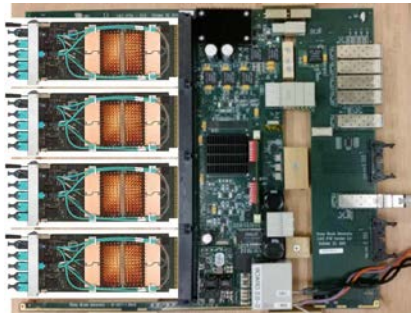




2. LSB(mezzanine)

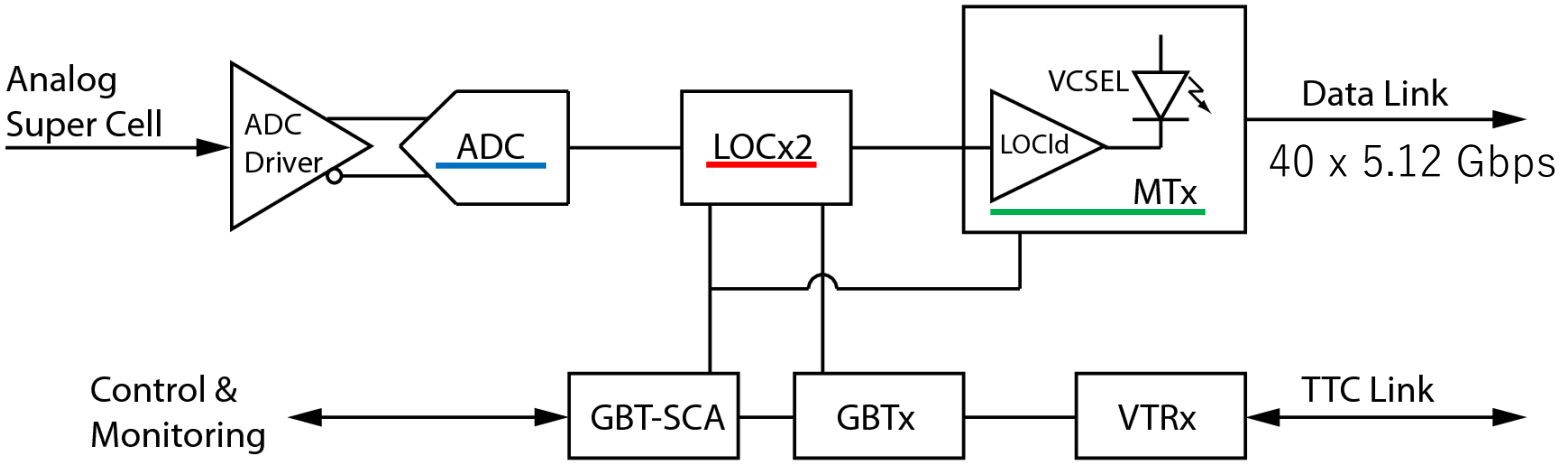


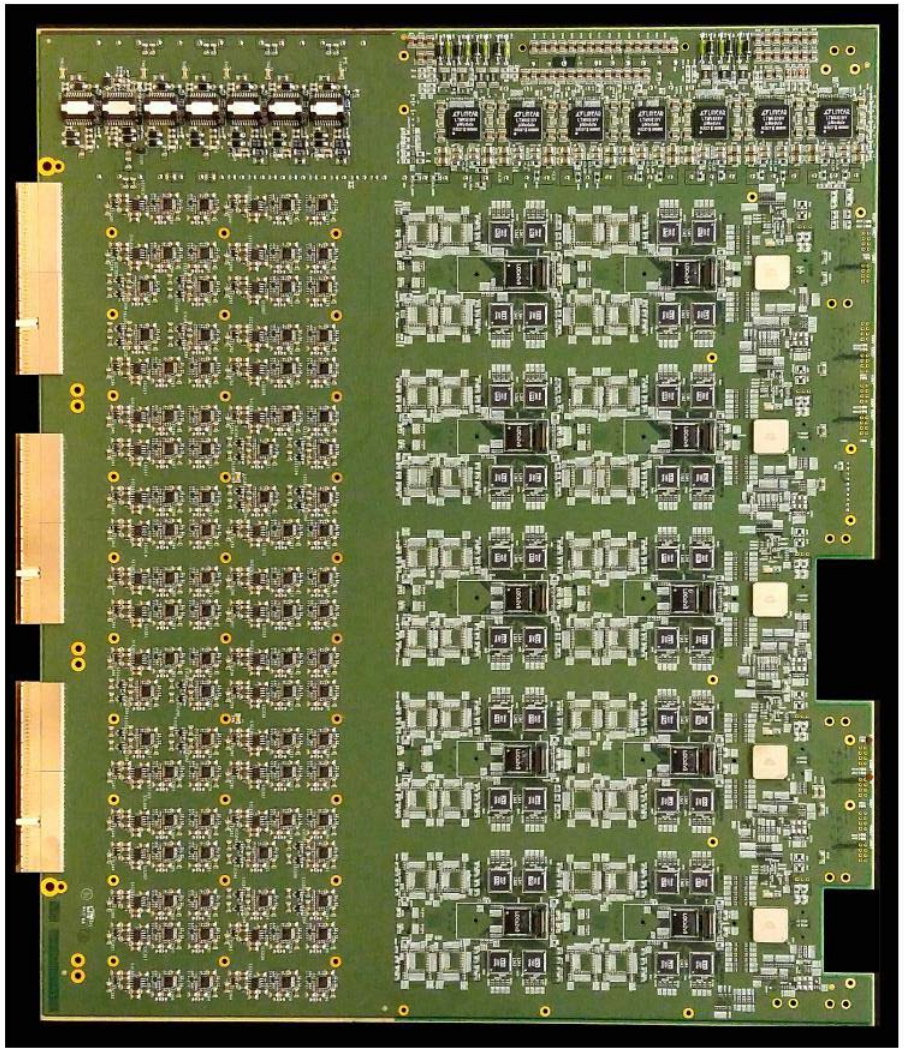
③ **LTDB** digitizer board



④ **LDPB** digitizer processing

Frontend: LTDB LAr Trigger Digitizer Board





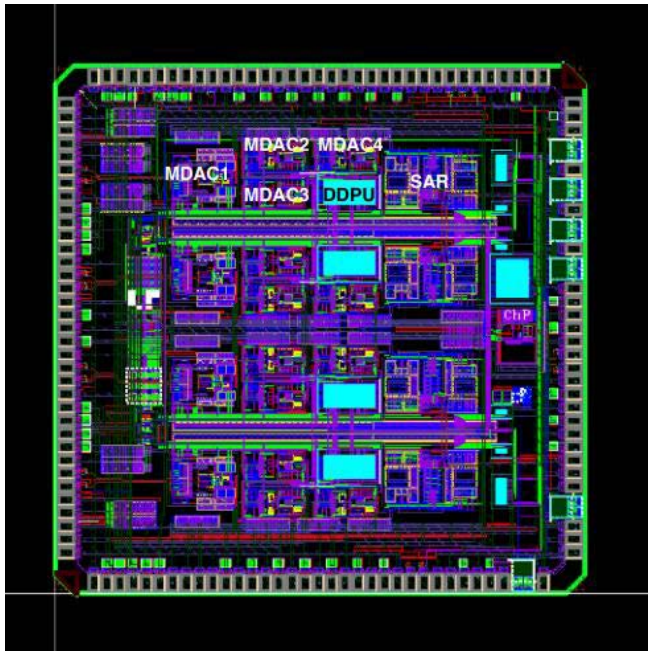
- Functionalities:

  Digitize Analog signal, **serialize** and **transmit**
  - Custom radiation tolerant **ASICs**(ADC, serializer)
  - **320 Super Cells** per board
  - 24 layers PCB with 2.23 mm thickness
  - **Latency < 275 ns**
  - GBT links used for LHC clock and Trigger information (Timing, Trigger and Control)

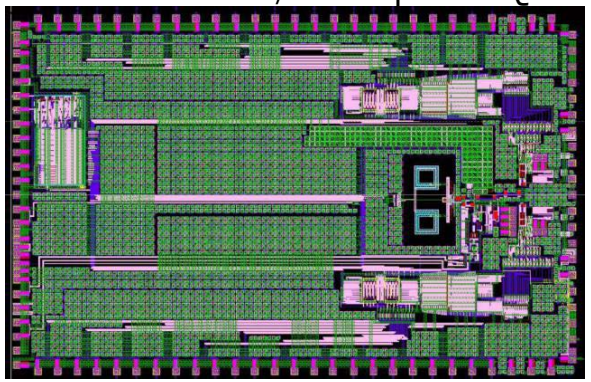
Custom made ASICs

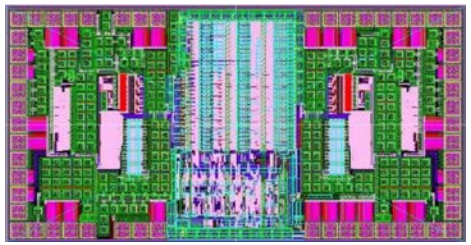
- Quad channel ADC: Nevis-15
  - 40 MS 12 bits pipeline ADC
  - IBM8RF 130 nm CMOS
  - ENOB 11 bits, Dynamic range: 11.7 Bits
  - 50 mW / channel
  - Latency ~ 100 ns
- Serializer: LOCx2
  - Dual channel 8x14 bits
  - 5.12 Gbs transmission
  - 250 nm Silicon-on-Sapphire
  - Fixed latency < 75 ns
- Laser driver: LOCld
  - Dual channel VCSEL driver

Navis-15 ADC :3.6 x 3.6 mm, 72 pins QFN



LOCx2: 6.036x3.68mm, 100 pins QFN

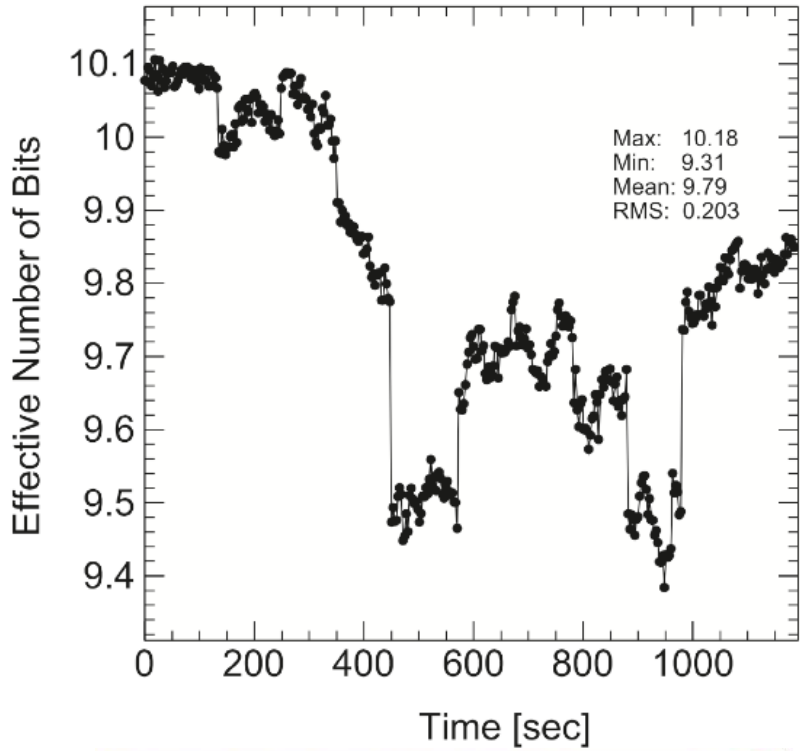


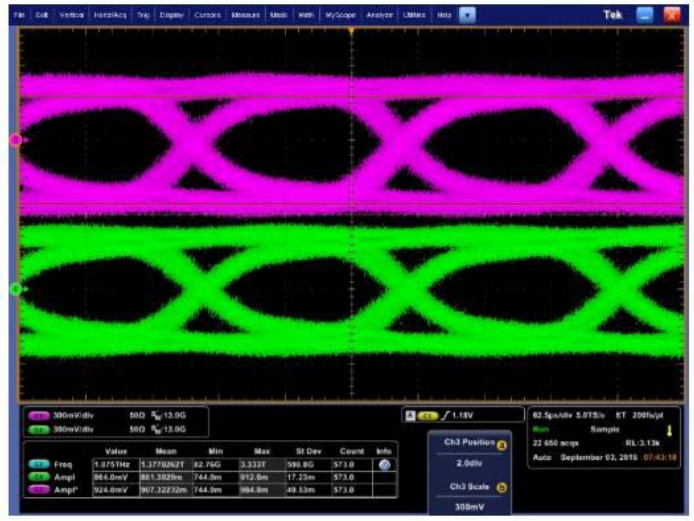


LOCld:
2.114 x 1.090 mm 40 pins QFN

Radiation tolerance on ASICs

- HL-LHC requirement
  - 100 kRad of total dose and SEE tests with total fluency of 3.8 x 10^{12} h/cm^2.
- Quad channel ADC: Nevis-15
  - Radiation tolerance established up to 10 MRad
  - See cross section as 10^{-12} cm^2 per channel
- Serializer(LOCx2) and Laser driver(LOCld)
  - No change in the output eye diagram has been observed after ~ 200 kRad TID.





Towards LTDB production

- ASIC production

  Serializer: LOCx2
  - No issue observed in wafer production
  - Working on packaging
    - Reasonable yields, long term stability
  - QA tests on-going.

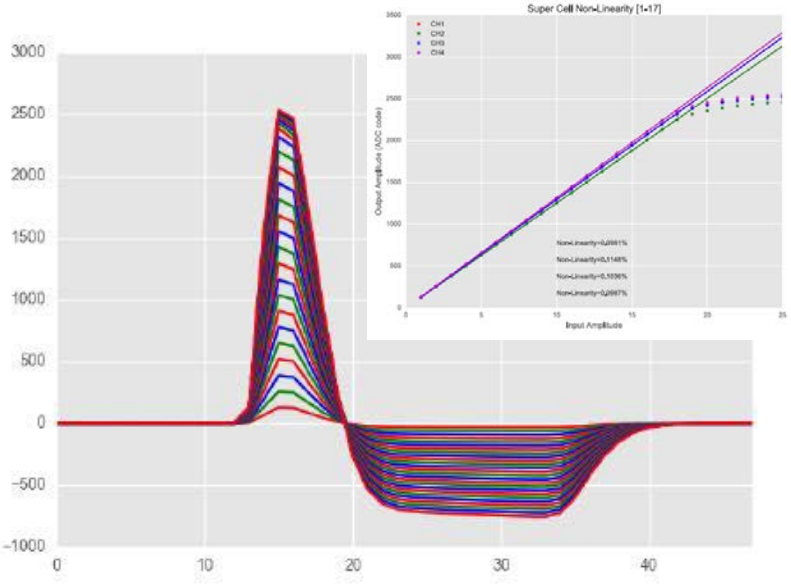
  ADC: Nevis-15
  - Established 80% yield, including dicing and packaging

    Performed QC test on 186 chips
  - Wafer production finished this month
  - Established QA procedure
    - ~ 2100 chips / week.

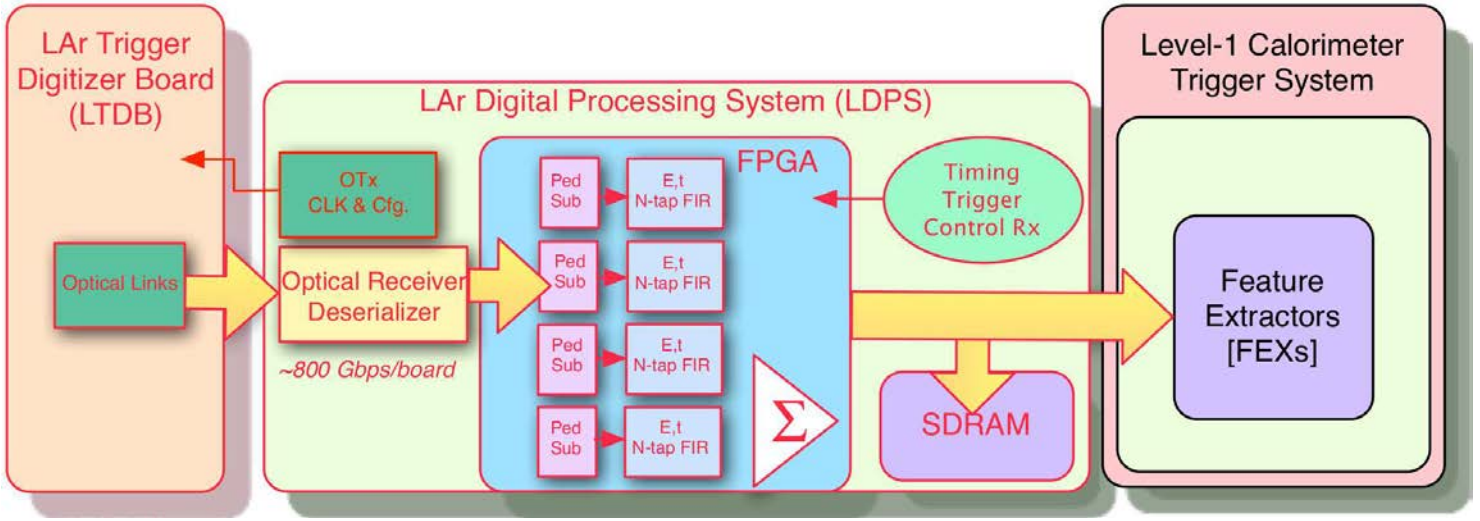
    → Expect all 13k chips available in Aug.

- LTDB board
  - Pre-production board
    - Design is almost final.

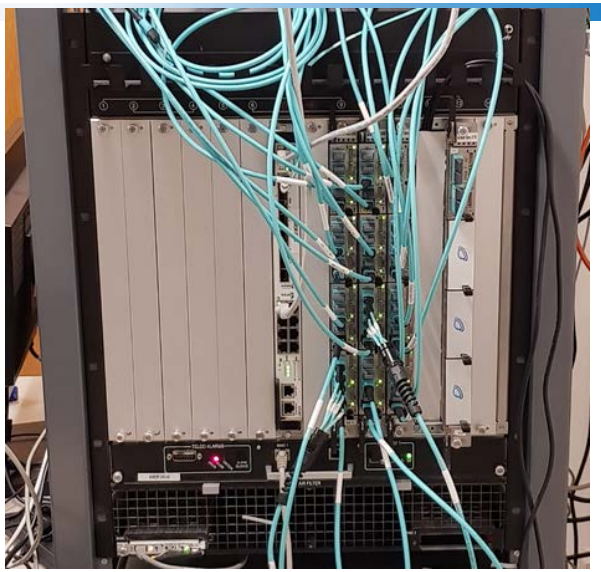
    After extensive test, two boards installed in ATLAS
    - Replaced two demonstrators installed in 2014.
    - Verified Super Cell connectivity.
  - Last updates on fiber routing is ongoing.
  - QA test stand is under preparation.



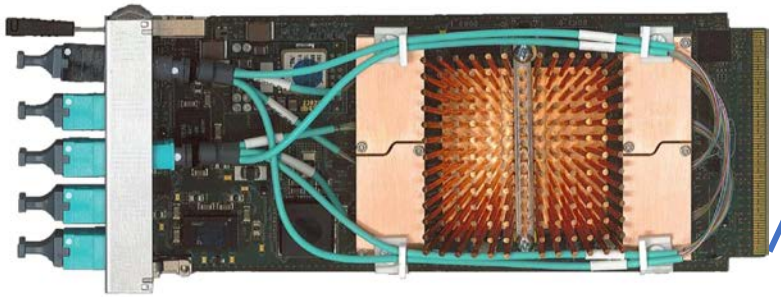
Backend: LDPB LAr Digital Processing Board



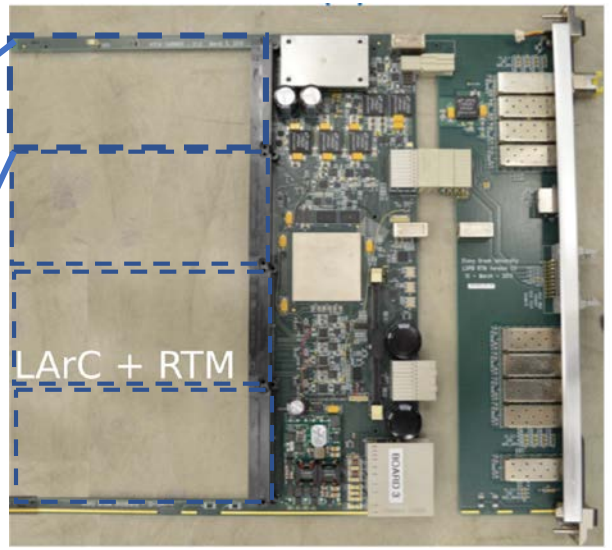
ATCA



- Main data transfer rate
  - 25.2 Tbps from frontend
  - 41.1 Tbps to L1 system
- Functionalities:
  - Transverse Energy computation
  - Energy sum
  - Monitoring

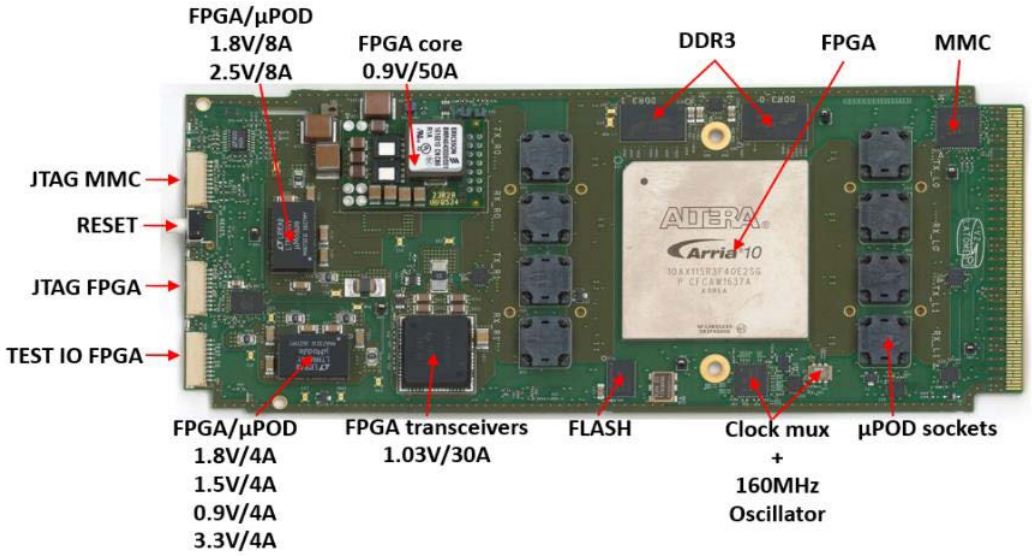


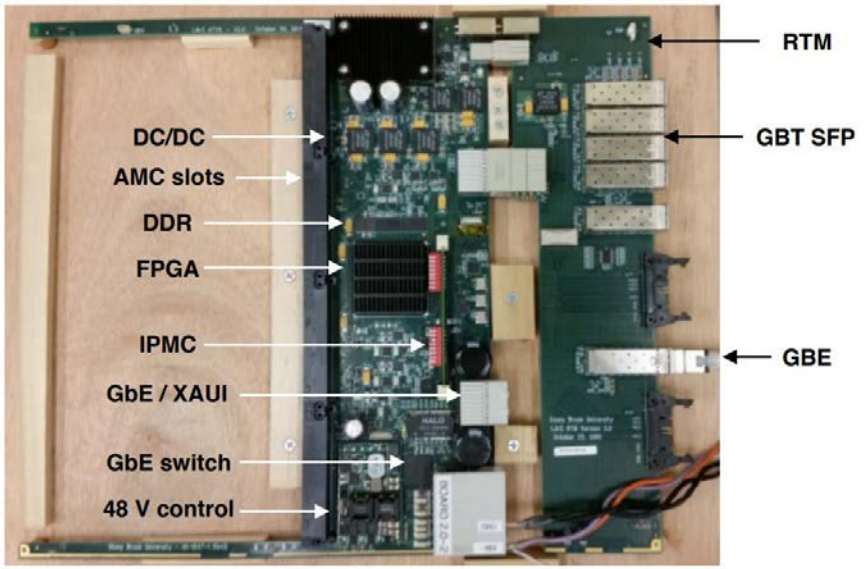
Advanced Mezzanine Card (LATOME)
→ Total 124 LATOMEs



ATCA carrier blade and RTM
→ Total 32 blades.

LATOME LAr Trigger prOcessing Mezzaine & LArC LAr Carrier card

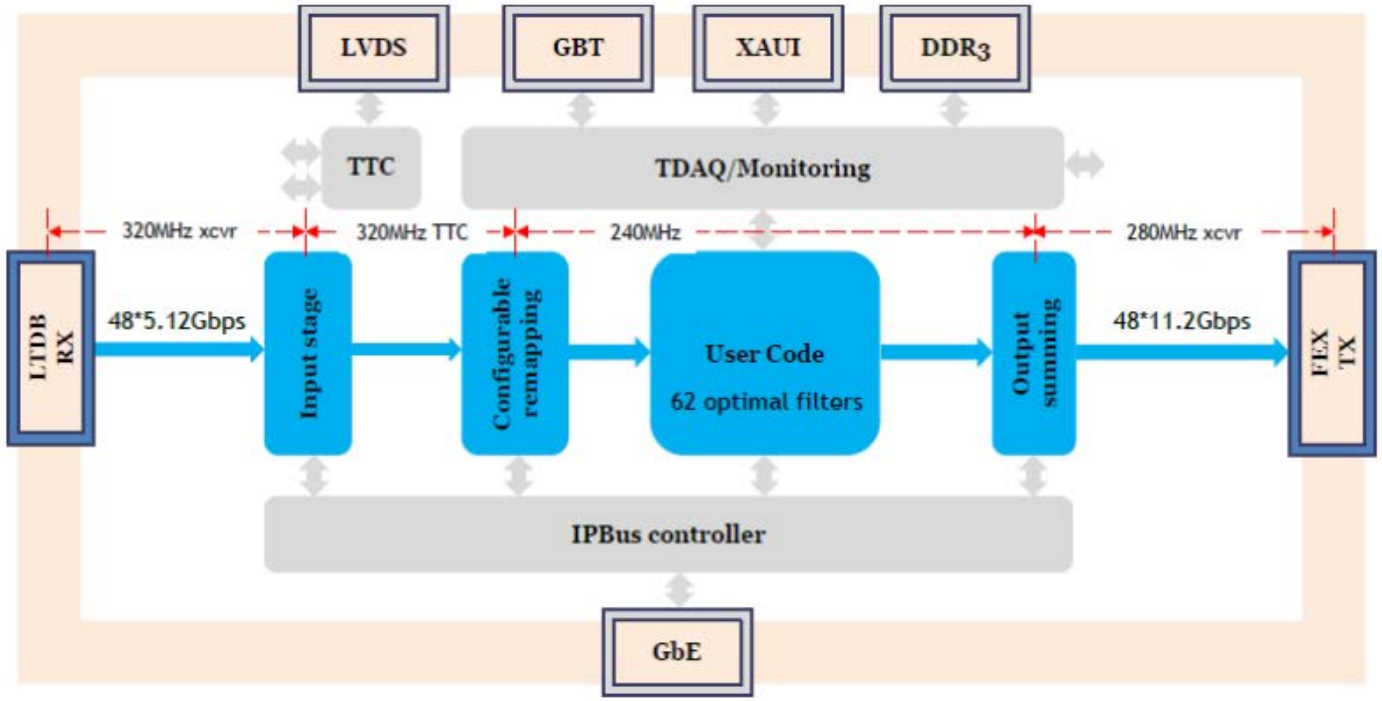




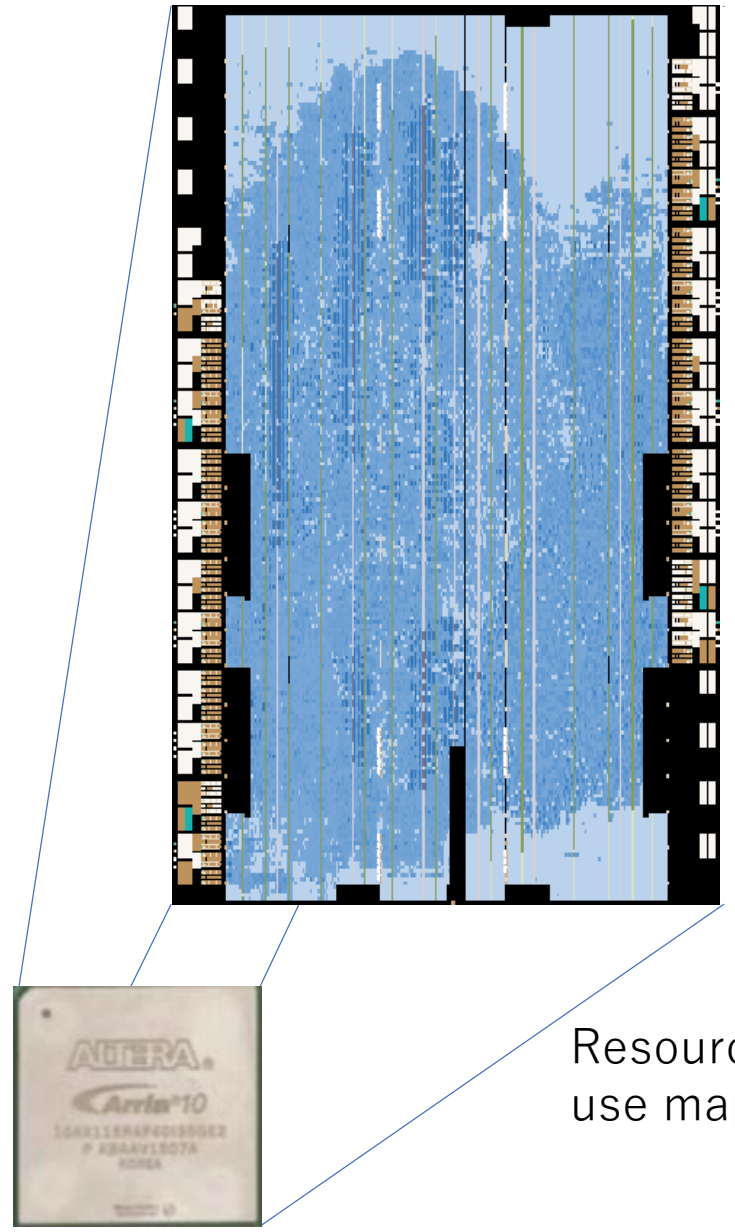
- LATOME (ATCA AMC)
  - 16 layer PCB with 1.6 mm thickness
  - Power consumption: up to 80 W
  - Intel **Arria-10 FPGA**
- Data Transmission
  - Input: **48 fibers (5.12 Gbps)**
  - Output: **48 output fibers (11.2 Gbps)**
    - Eight MicroPODs
  - 1 GBT links

- LArC: (ATCA Carrier blade with RTM)
  - 22 layer PCB with 2.4 mm thickness
  - Power consumption: ~280 W
    (designed up to 400 W)
  - Xilinx **Vertex-7 FPGA**
  - ATCA IMPC
- Data Transmission
  - 10 Gbps link via ATCA fabric
  - 5 GBT links via RTM
  - 1 Gbps links via RTM (slow control)

LATOME firmware



- Tasks on LATOME(per card)
  1. Receive 48 data stream (fiber @ 5.12 Gbps)
  2. Remap channel
  3. ET and BC assignment (Filtering)
     - Accurate Energy at proper bunch crossing
  4. Energy Summing ($\Delta\eta \times \Delta\phi$ =0.1x0.1 and 0.2x0.2)
  5. Transmit 48 data stream (fiber @ 11.2 Gbps)



Resource use map

Intel-Altera Arria-10 FPGA

Energy reconstruction

- Calculate the energy at fixed Latency
  - The energy is proportional to peak value of pulse.
    - The peak is around 3rd point
  - FIR calculation(optimal filtering)
    - a_i , b_i are set to minimize noise by using calibration and physics data.

$$E_T = \sum_{i=1}^{4} a_i S_i$$

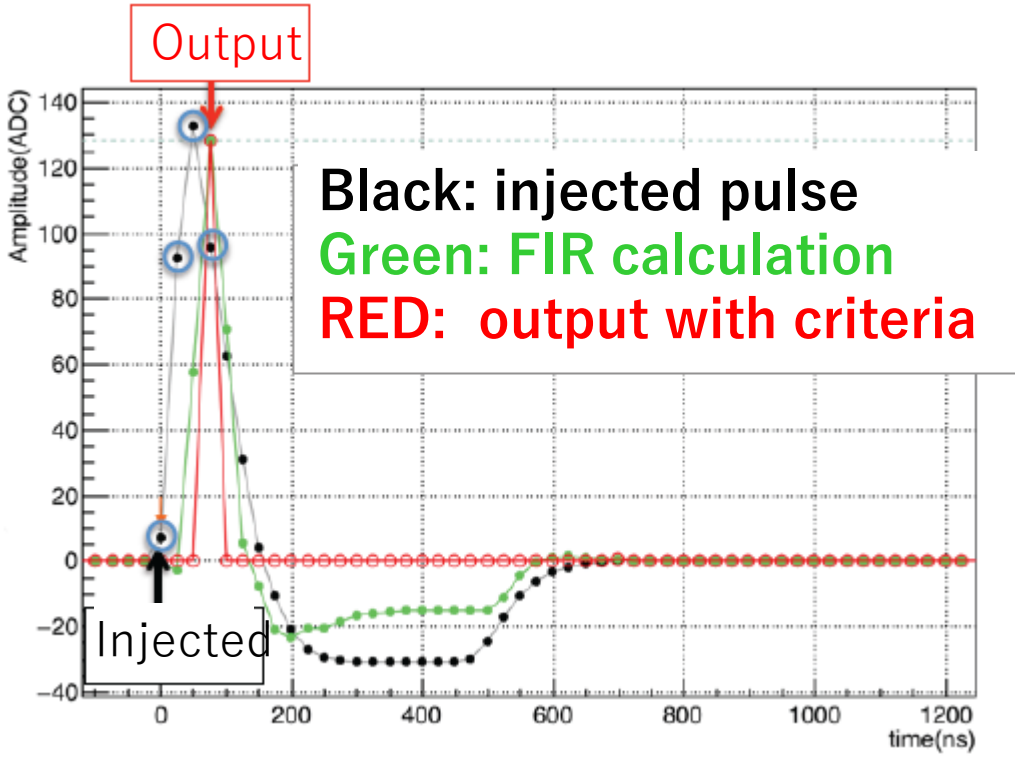
$$E_T\tau = \sum_{i=1}^{4} b_i S_i$$

Criteria

$E_T > 0$ & $|\tau| < 12.5$ ns

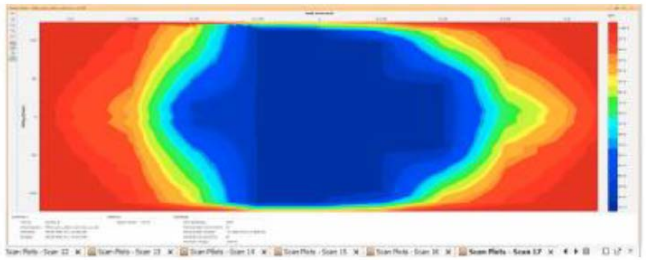
An energy with fulfilling the criteria is the energy at the right BC.

Options for alternative filter:
Wiener filter, Extended Optimal filter

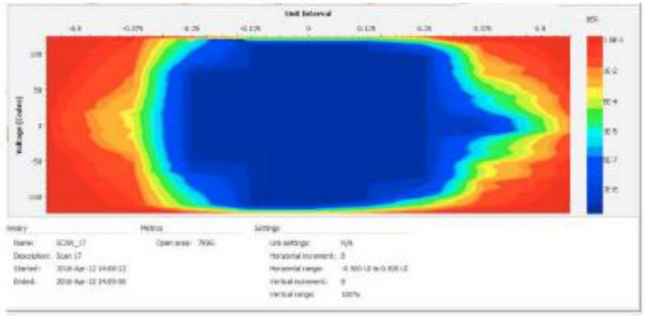


Performance test towards production

Data transmission



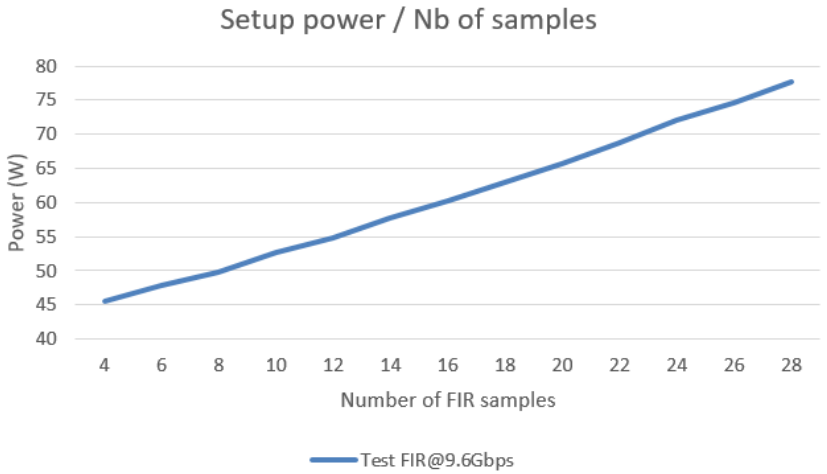
To gFEX

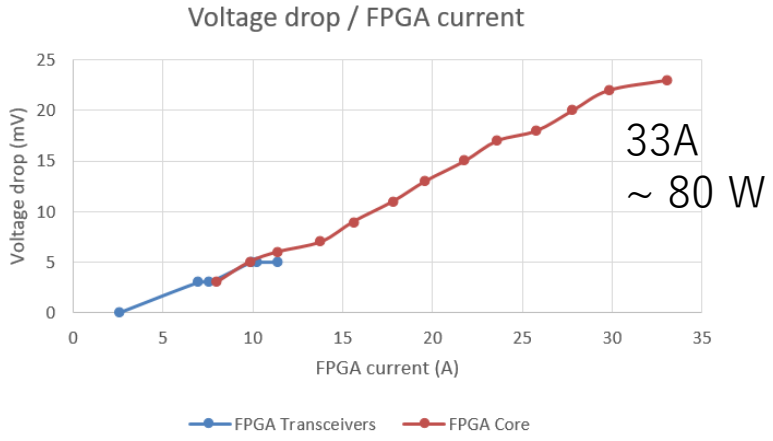


To eFEX

All 48 Rx/Tx: BER (<10^{-14})@11.2 Gbps

Power consumption





Verified LATOME operation with full load on FPGA.

Latency

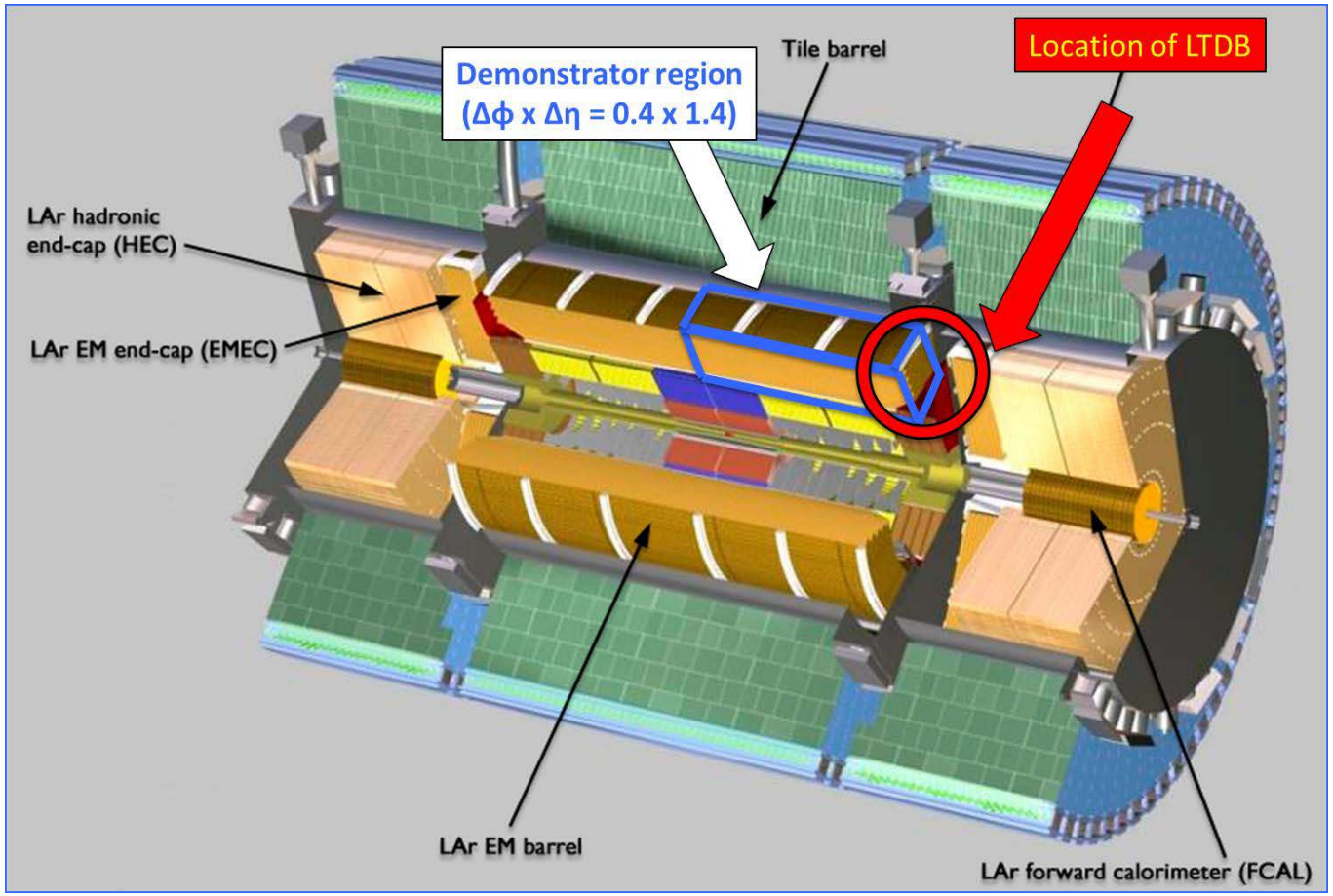
Block	Spec	Meas
Interface	2	2
Input stage	3	2.63
Remapping	1.5	1.75
ET calc	5	4.5
Summing	1.5	2.5
Interface	2	2
Total	**15**	**15.38**

Unit: BC=25 ns

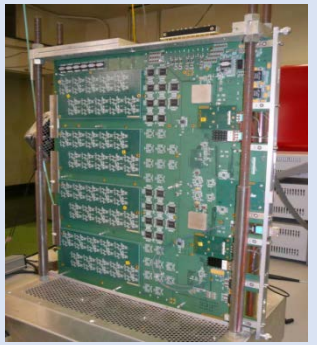
Verify a fixed latency on various resets.

All requirements fulfilled.
Production has been started!

LAr Phase-1 Demonstrators



Frontend


70m

x100

Backend

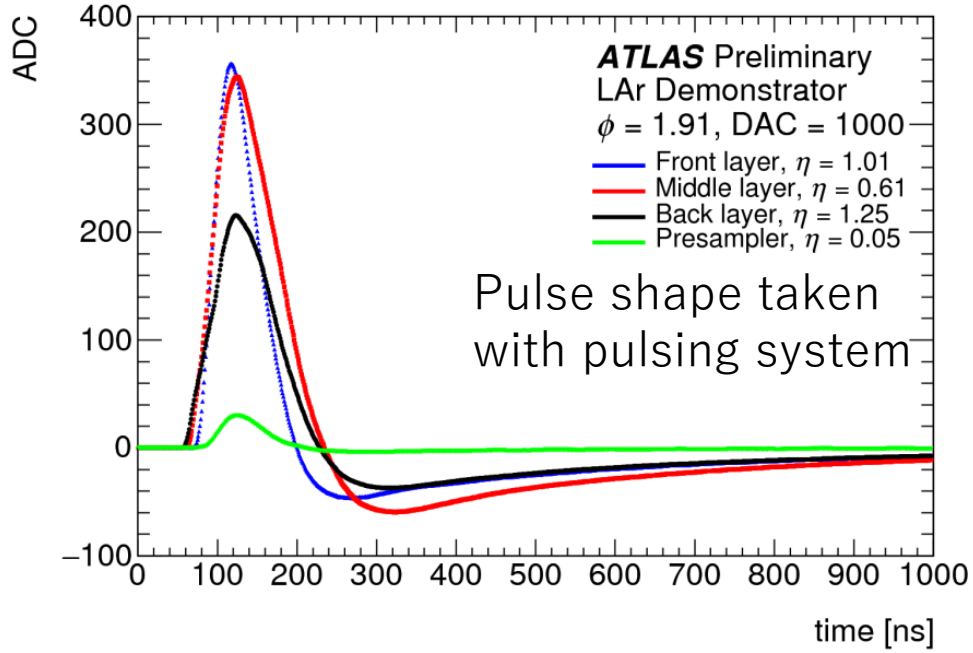


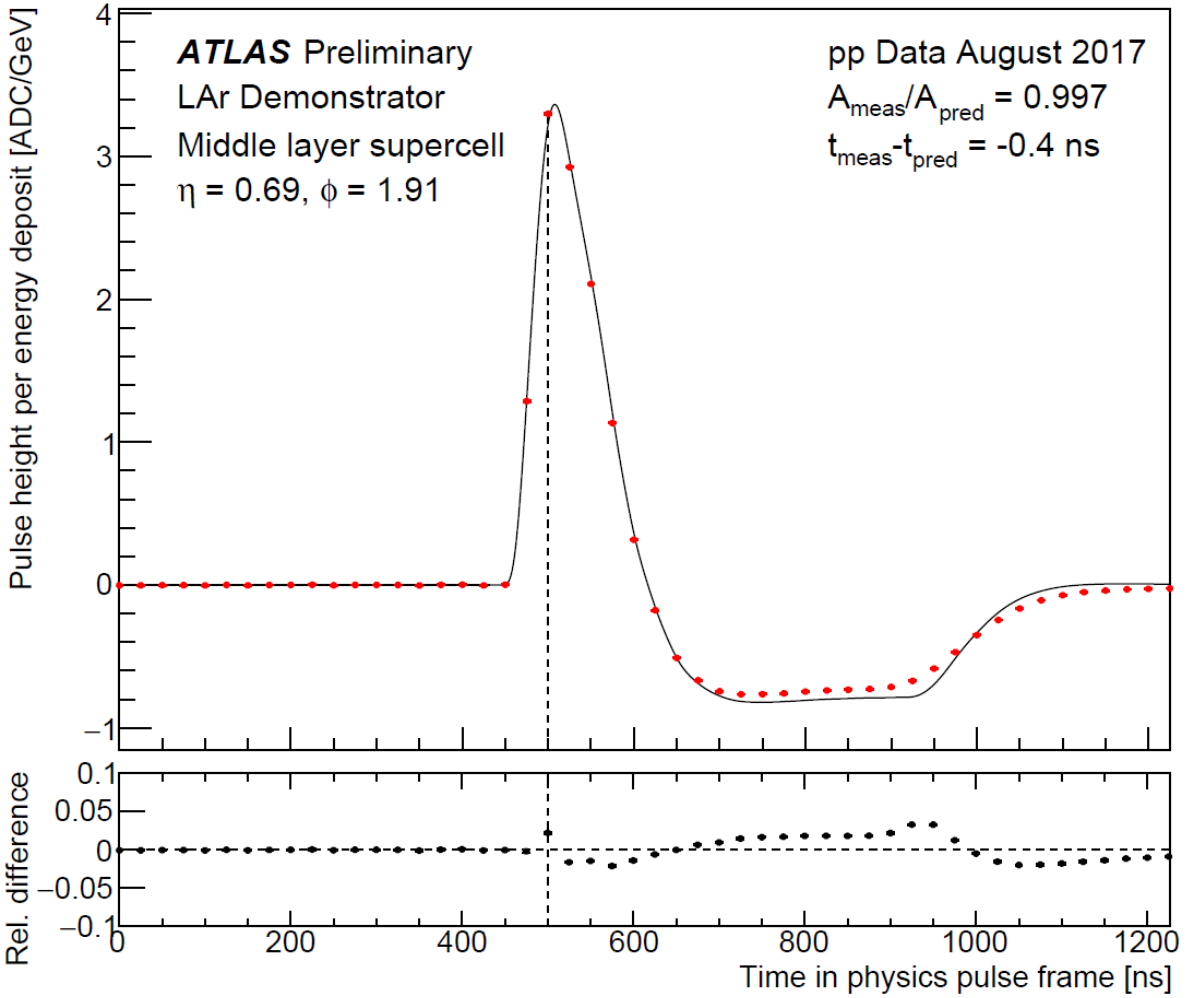
In 2018, replaced with pre-production boards.

- Demonstrators are in ATLAS since 2014.
- Collecting collision data in LHC Run2
- Check installation procedure, system feasibility and stability

Demonstrator calibrations

- It is important to understand the pulse shape of Super Cell output to reconstruct the transverse energy.
- Established calibration method for Super Cell.



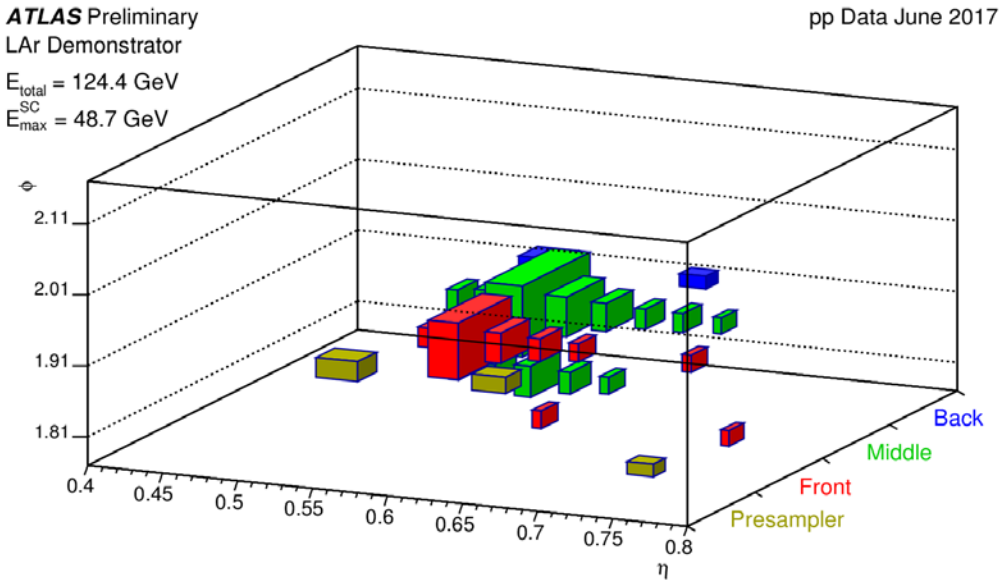


Expected pulse from calibration run(black). Compared to collision data(red). Good match!

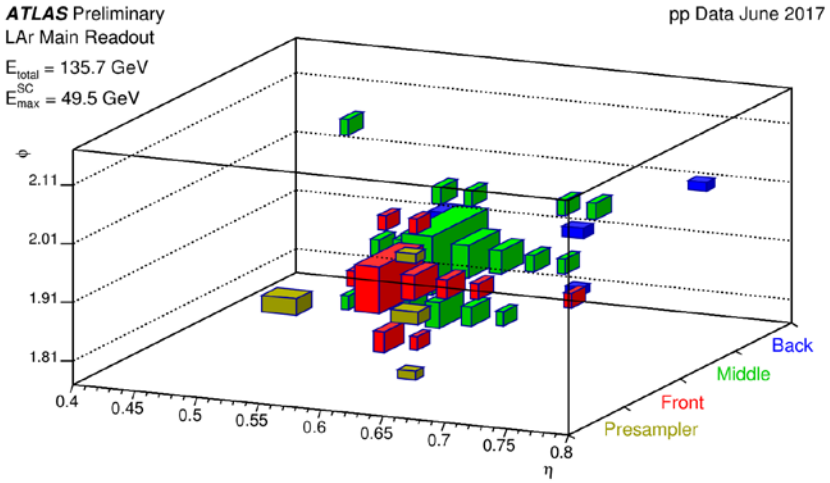
Collision data with demonstrator

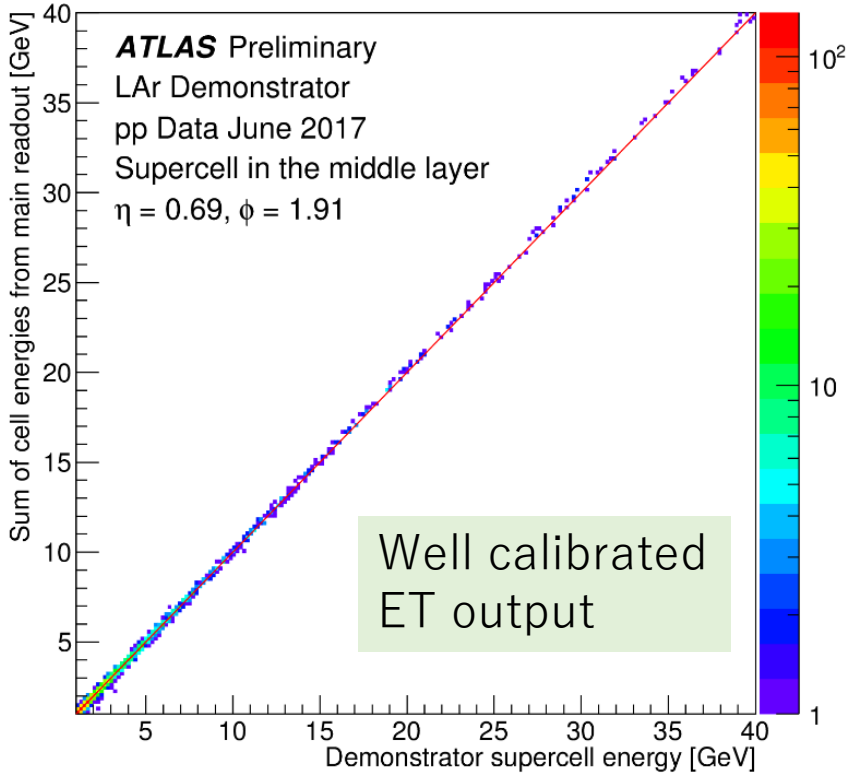
- Comparison with Main readout on cluster

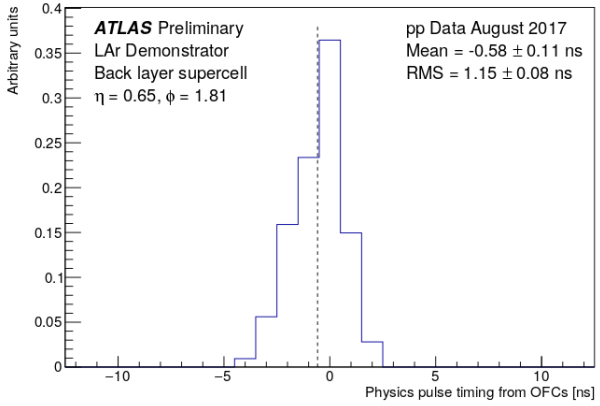
Demonstrator



Main readout







Time phase
Well distributed within same BC.
(1 BC=25 ns)

Summary

- ATLAS LAr Calorimeter Phase-1 upgrade (2018 Dec-2021 Mar)
  - Upgrade the trigger readout, will be used for HL-LHC (upto ~2035).
- Frontend: design is almost finalized.
  - ASIC packaging and update analog mapping to ease fiber routing
- Backend: going well
  - Production will be started soon
  - Next: assembling and QA tests
- Demonstrator
  - Installed in 2014 August, data taking since beginning of Run-2.
    - Established calibration machinery
    - compatibility test with Main readout.
  - 2018 Jan, replaced with Pre-production board.
    - Overall latency, stabilities will be verified.
    - Collect more data for filtering studies.