The Phase-1 Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeter

Yuji Enari, ICEPP, the University of Tokyo
On behalf of ATLAS LAr group

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ATLAS Liquid Argon Calorimeter

- Pb-LAr EM sampling calorimeter
  - $\sigma/E \sim 10%/\sqrt{E} \pm 0.7$
  - fine granularity: $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ (middle layer)
  - Total 22 $X_0$
  - 4 layers, total $180 \times 10^3$ channels
- $e/\gamma$ trigger, ID, transverse energy
  - Essential for precise measurements, esp. Higgs physics
LHC upgrade schedule

<table>
<thead>
<tr>
<th>Year</th>
<th>Run-2</th>
<th>Run-3</th>
<th>Hi-Lumi</th>
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√s = 13 TeV
L = 1.7 × 10^{34} cm^{-2}s^{-1}
∫Ldt = 150 fb^{-1}
μ~50

√s = 14 TeV
L = 3 × 10^{34} cm^{-2}s^{-1}
∫Ldt = 300 fb^{-1}
μ~80-100

√s = 14 TeV
L = 5~7 × 10^{34} cm^{-2}s^{-1}
∫Ldt = 3000 fb^{-1}
μ~200

Accelerator, Detector upgrades.

Event with two photons. (Recorded in 2014)
Aiming such clean condition at high luminosity runs.
ATLAS LAr Calorimeter upgrade:

**LS2: Phase-1 upgrade**
- **Trigger readout** upgrade
- Level-1 trigger
  - 100 kHz ~ latency 3 $\mu$s
- data recording rate: 1 kHz.

**LS3: Phase-2 upgrade**
- **Main readout** upgrade
- Forward part detector upgrade
- Level-1 trigger
  - 1 MHz ~ latency 10-20 $\mu$s
- data recording rate: 5-10 kHz.
ATLAS LAr Phase-1 upgrade project

- Upgrade for Calorimeter trigger in LS2 (2019-2020)

Current readout:

Trigger Tower: 
\( \Delta \eta \times \Delta \phi = 0.1 \times 0.1 \)

NEW readout:

Super Cell:
4 layers, 10 SCs
(Typical case)

- Digitize at Frontend (on-detector),
- Realtime processing at Backend (off-detector).
  - High density, high speed data transmission
  - Digital filtering on FPGA

Electron with 70 GeV
Size of Moliere radius in \( \eta \) is \( \sim 0.08 \)

Ten times finer granularity
+ Better energy resolution
  \( \rightarrow \) Higher BG rejection
Expected performance

- Better energy resolution
- Better signal (EM object) to background (Jets) separation
  - Keep lower threshold within given Level-1 rate budget (20 kHz for Single EM)
- Very important for the ATLAS physics program!
  - For $W \rightarrow e\nu$, $Z \rightarrow ee$, $H \rightarrow \gamma\gamma$: Trigger on EM objects with 20-30 GeV.
New Hardware

1. Frontend (on-detector)
2. Backend (off-detector)
3. LTDB digitizer board
4. LDPB digitizer processing
New Hardware

1. Baseplane

2. LTDB digitizer board

3. LDPB digitizer processing
New Hardware

1. Baseplane

2. LSB (mezzanine)

3. LTDB digitizer board

4. LDPB digitizer processing
New Hardware

1. Baseplane

2. LSB (mezzanine)

3. LTDB digitizer board

4. LDPB digitizer processing
New Hardware

1. Baseplane

2. LSB (mezzanine)

3. LTDB digitizer board

4. LDPB digitizer processing
Frontend: LTDB  
LAr Trigger Digitizer Board

- **Functionalities:**
  - **Digitize** Analog signal, **serialize** and **transmit**
    - Custom radiation tolerant **ASICs** (ADC, serializer)
    - **320 Super Cells** per board
    - 24 layers PCB with 2.23 mm thickness
    - **Latency < 275 ns**
    - GBT links used for LHC clock and Trigger information (Timing, Trigger and Control)
Custom made ASICs

- **Quad channel ADC**: Nevis-15
  - 40 MS 12 bits pipeline ADC
  - IBM8RF 130 nm CMOS
  - ENOB 11 bits, Dynamic range: 11.7 Bits
  - 50 mW / channel
  - Latency ~ 100 ns

- **Serializer**: LOCx2
  - Dual channel 8x14 bits
  - 5.12 Gbs transmission
  - 250 nm Silicon-on-Sapphire
  - Fixed latency < 75 ns

- **Laser driver**: LOCld
  - Dual channel VCSEL driver
Radiation tolerance on ASICs

• HL-LHC requirement
  • 100 kRad of total dose and SEE tests with total fluency of $3.8 \times 10^{12} \text{ h/cm}^2$.

• Quad channel ADC: Nevis-15
  • Radiation tolerance established up to 10 MRad
  • See cross section as $10^{-12} \text{ cm}^2$ per channel

• Serializer (LOCx2) and Laser driver (LOCId)
  • No change in the output eye diagram has been observed after ~ 200 kRad TID.
Towards LTDB production

• ASIC production
  Serializer: LOCx2
  • No issue observed in wafer production
  • Working on packaging
    • Reasonable yields, long term stability
  • QA tests on-going.

  ADC: Nevis-15
  • Established 80% yield, including dicing and packaging
  • Performed QC test on 186 chips
  • Wafer production finished this month
  • Established QA procedure
    • ~ 2100 chips / week.
  → Expect all 13k chips available in Aug.

• LTDB board
  • Pre-production board
    • Design is almost final.
  After extensive test, two boards installed in ATLAS
    • Replaced two demonstrators installed in 2014.
    • Verified Super Cell connectivity.
  • Last updates on fiber routing is ongoing.
  • QA test stand is under preparation.
Main data transfer rate:
- **25.2 Tbps** from frontend
- **41.1 Tbps** to L1 system

Functionalities:
- Transverse Energy computation
- Energy sum
- Monitoring

Advanced Mezzanine Card (LATOME) ➔ **Total 124 LATOMEs**

ATCA carrier blade and RTM ➔ **Total 32 blades.**
LATOME (ATCA AMC)
- 16 layer PCB with 1.6 mm thickness
- Power consumption: up to 80 W
- Intel Arria-10 FPGA

Data Transmission
- Input: **48 fibers (5.12 Gbps)**
- Output: **48 output fibers (11.2 Gbps)**
  - Eight MicroPODs
  - 1 GBT links

LArC: (ATCA Carrier blade with RTM)
- 22 layer PCB with 2.4 mm thickness
- Power consumption: ~280 W
  (designed up to 400 W)
- Xilinx Vertex-7 FPGA
- ATCA IMPC

Data Transmission
- 10 Gbps link via ATCA fabric
- 5 GBT links via RTM
- 1 Gbps links via RTM (slow control)
LATOME firmware

- Tasks on LATOME (per card)
  1. Receive 48 data stream (fiber @ 5.12 Gbps)
  2. Remap channel
  3. ET and BC assignment (Filtering)
     - Accurate Energy at proper bunch crossing
  4. Energy Summing ($\Delta \eta \times \Delta \phi = 0.1 \times 0.1$ and $0.2 \times 0.2$)
  5. Transmit 48 data stream (fiber @ 11.2 Gbps)
Energy reconstruction

- Calculate the energy at fixed Latency
  - The energy is proportional to peak value of pulse.
    - The peak is around 3rd point
  - FIR calculation (optimal filtering)
    - $a_i, b_i$ are set to minimize noise by using calibration and physics data.

Criteria

$E_T > 0$ & $|\tau| < 12.5$ ns

An energy with fulfilling the criteria is the energy at the right BC.

Options for alternative filter:
Wiener filter, Extended Optimal filter
Performance test towards production

**Data transmission**

All 48 Rx/Tx: BER (<10^{-14})@11.2 Gbps

**Power consumption**

- Setup power / Nb of samples
- Voltage drop / FPGA current

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<th>Block</th>
<th>Spec</th>
<th>Meas</th>
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<tr>
<td>Total</td>
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<td>15.38</td>
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</table>

Unit: BC=25 ns

Verify a fixed latency on various resets.

**Latency**

All requirements fulfilled. Production has been started!
LAr Phase-1 Demonstrators

- Demonstrators are in ATLAS since 2014.
- Collecting collision data in LHC Run2
- Check installation procedure, system feasibility and stability
Demonstrator calibrations

- It is important to understand the pulse shape of Super Cell output to reconstruct the transverse energy.
- Established calibration method for Super Cell.

![Pulse shape taken with pulsing system](image1)

**Expected pulse from calibration run (black). Compared to collision data (red). Good match!**
Collision data with demonstrator

- Comparison with Main readout on cluster

**Demonstrator**

**Main readout**

Well calibrated ET output

**Time phase**
Well distributed within same BC.
(1 BC=25 ns)
Summary

• ATLAS LAr Calorimeter Phase-1 upgrade (2018 Dec-2021 Mar)
  • Upgrade the trigger readout, will be used for HL-LHC (upto ~2035).
• Frontend: design is almost finalized.
  • ASIC packaging and update analog mapping to ease fiber routing
• Backend: going well
  • Production will be started soon
  • Next: assembling and QA tests

• Demonstrator
  • Installed in 2014 August, data taking since beginning of Run-2.
    • Established calibration machinery
    • compatibility test with Main readout.
  • 2018 Jan, replaced with Pre-production board.
    • Overall latency, stabilities will be verified.
    • Collect more data for filtering studies.