

# ATLAS LAr Calorimeter

HL-LHC Electronics Upgrade

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On behalf of the  
ATLAS LAr Calorimeter Project

CALOR 2018

University of Oregon, May 2018

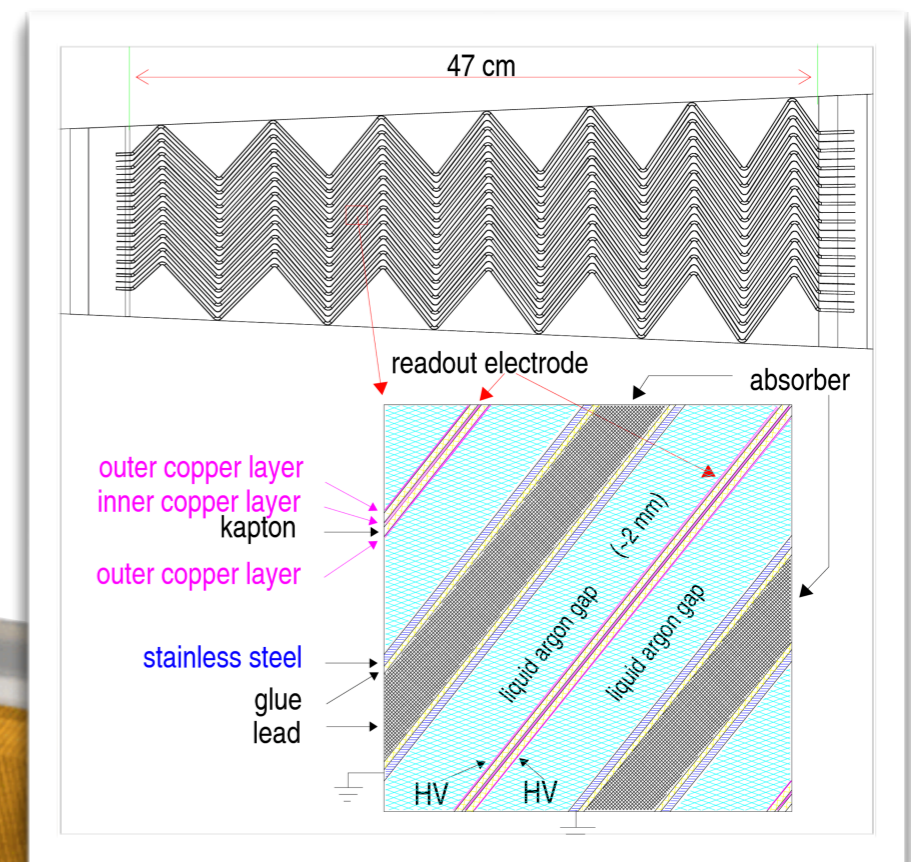
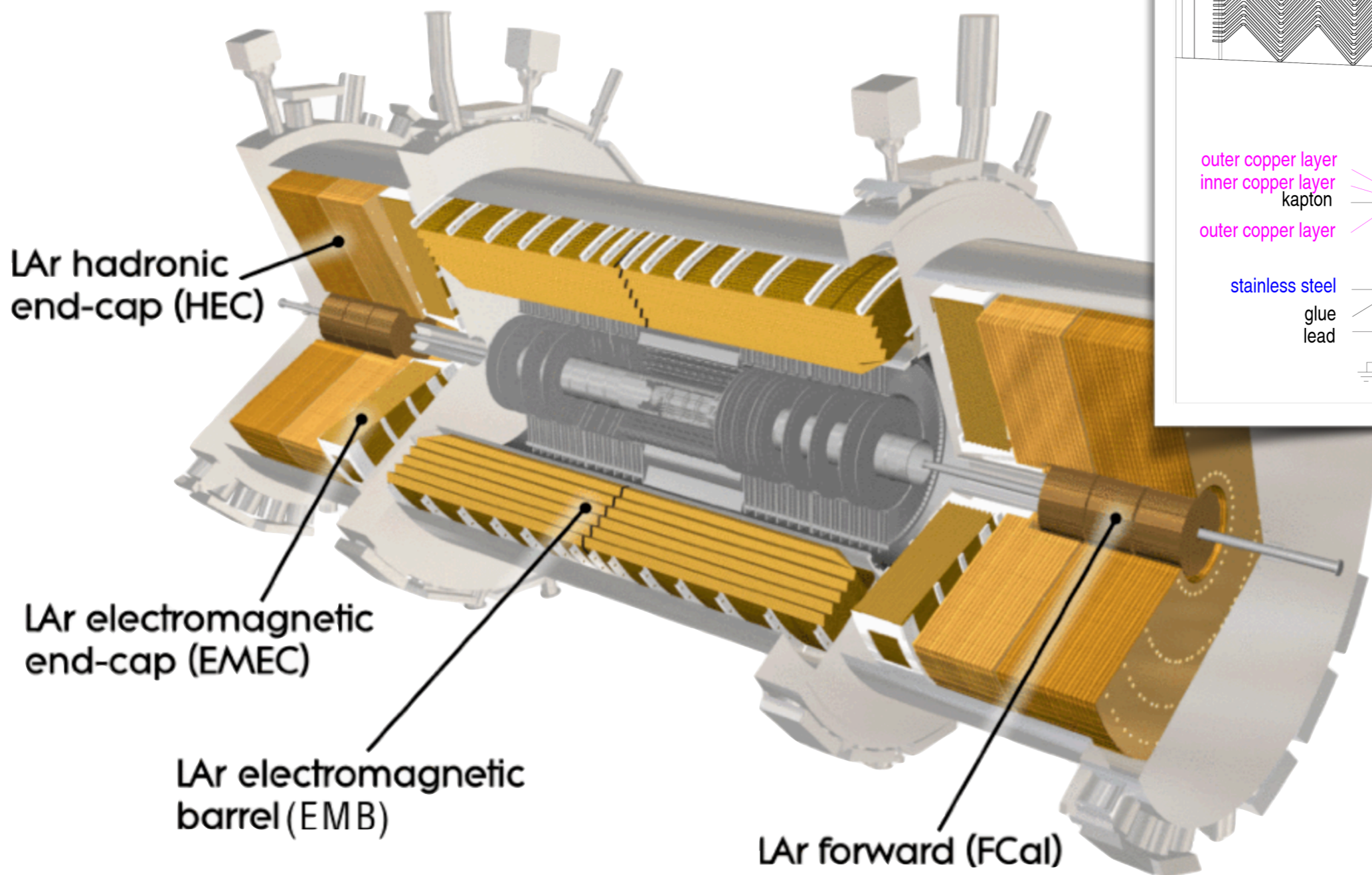


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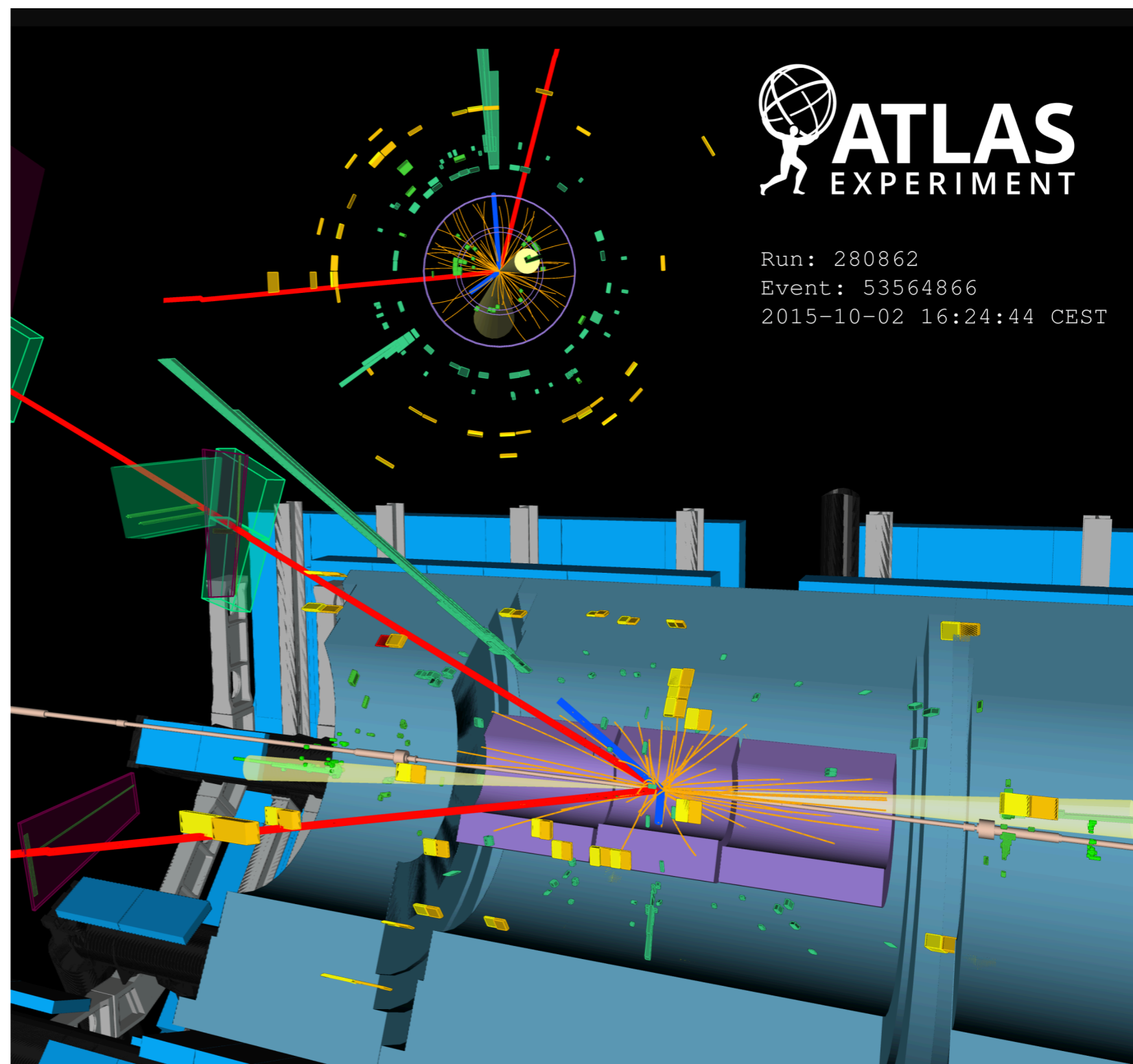
# LAr Calorimeter at the HL-LHC

- LAr Calorimeters will maintain performance  
→ will not be replaced.  
→ Upgrade focuses on electronics

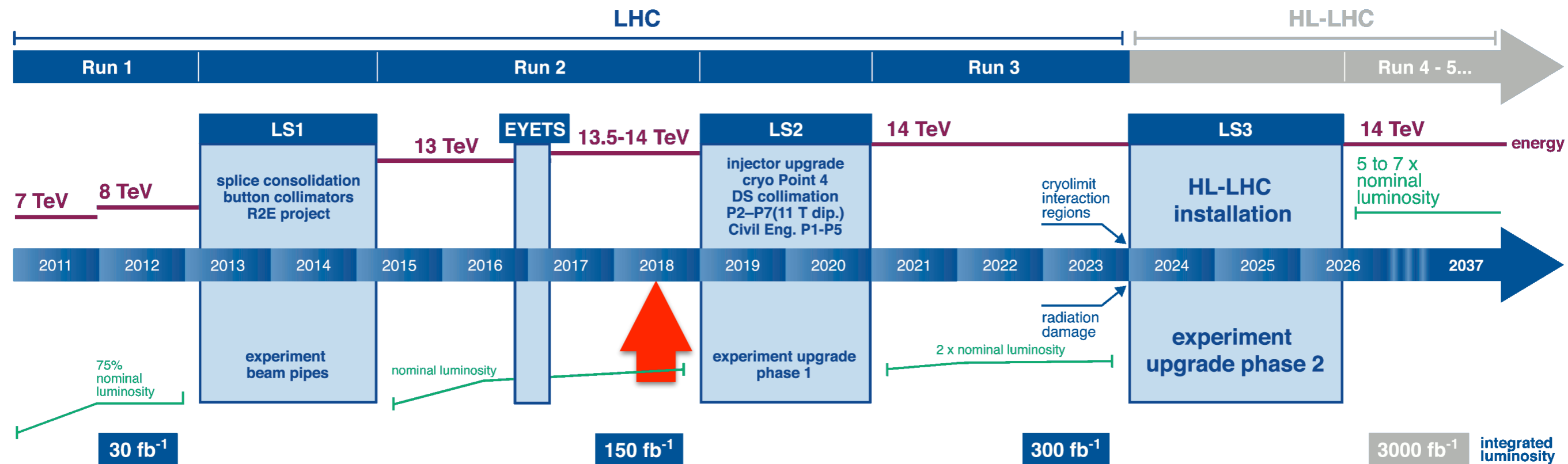


# LAr Calorimeter Upgrade Motivation

- **Critical sub-detector for most signatures of HL-LHC physics.**
  - ✓ electrons
  - ✓ photons
  - ✓ jets
  - ✓ missing  $E_T$
- Current electronics and power supplies will not survive HL-LHC radiation.
- Without upgrade must raise trigger thresholds, losing physics
- Instead, we provide more/better info at earlier trigger levels.
  - ➔ Intermediate step in **Phase 1**: use Super Cells to provide finer granularity to trigger
  - ➔ HL-LHC upgrade builds on Phase 1, **provides full granularity and full precision readout at 40 MHz** (bunch crossing frequency)



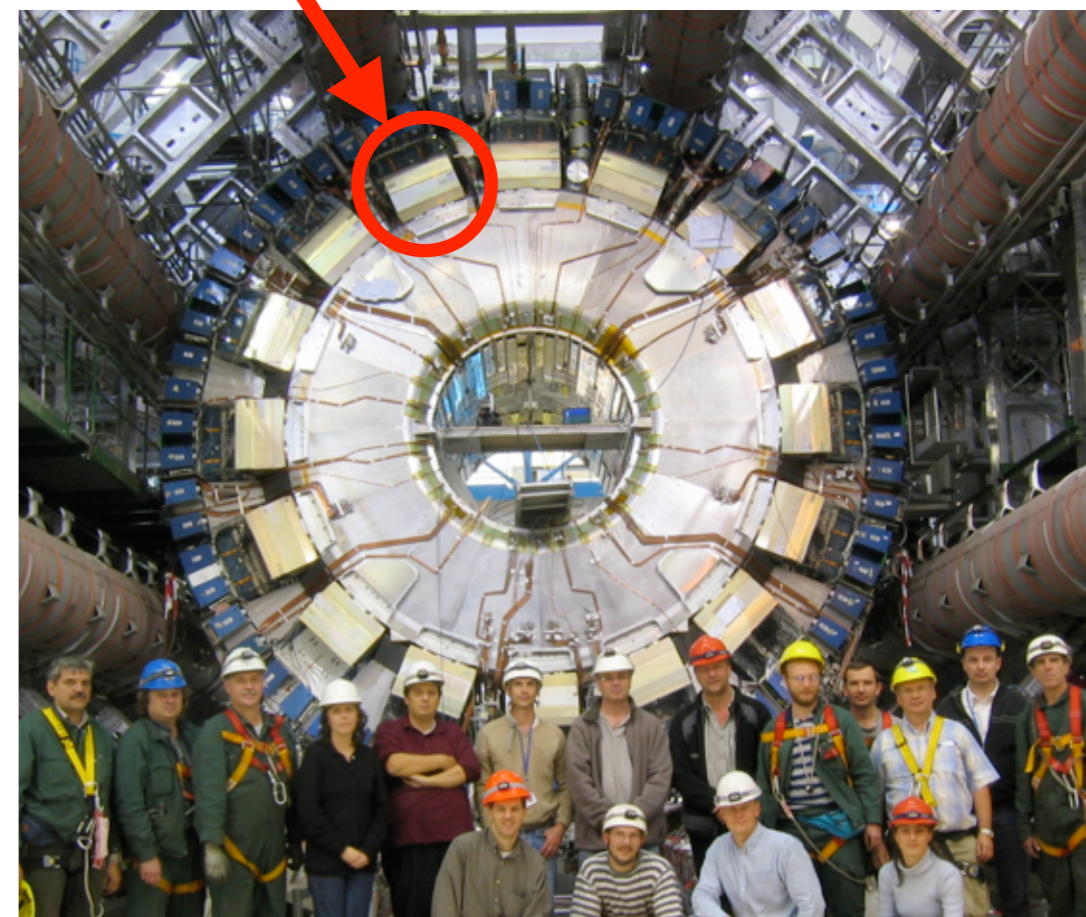
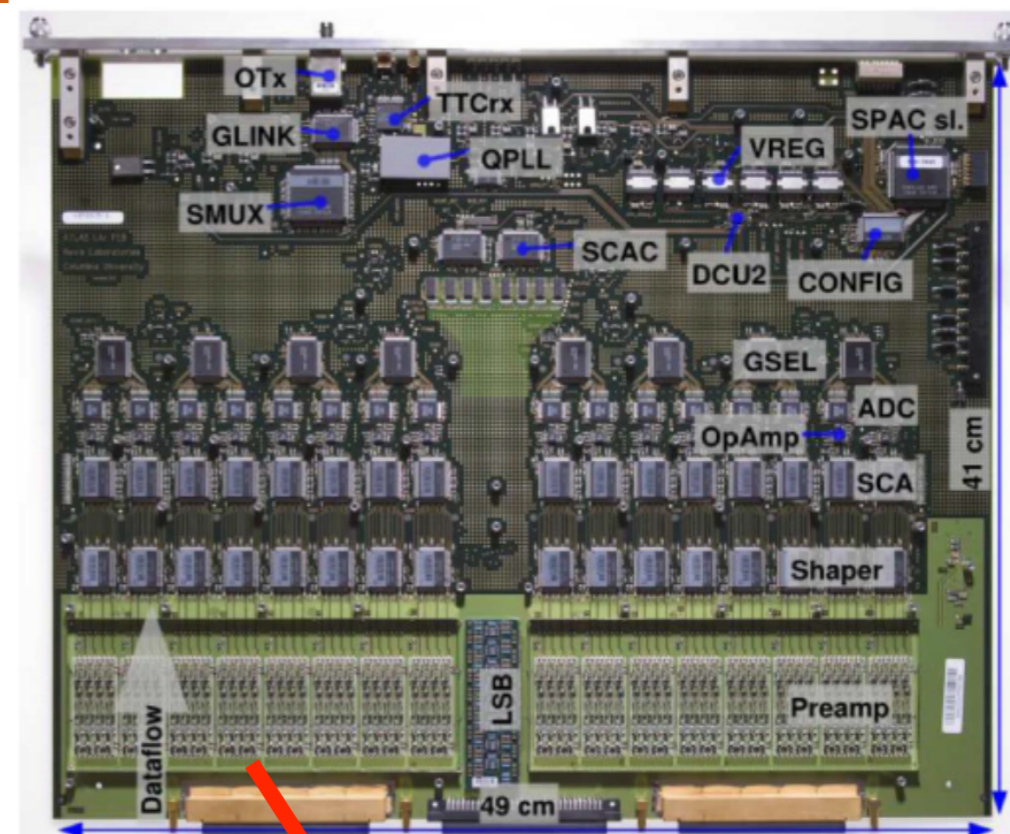
# Path to HL-LHC



- Greater instantaneous luminosity, harder to trigger on signal events.
  - Significant backgrounds from both in-time and out-of-time pileup

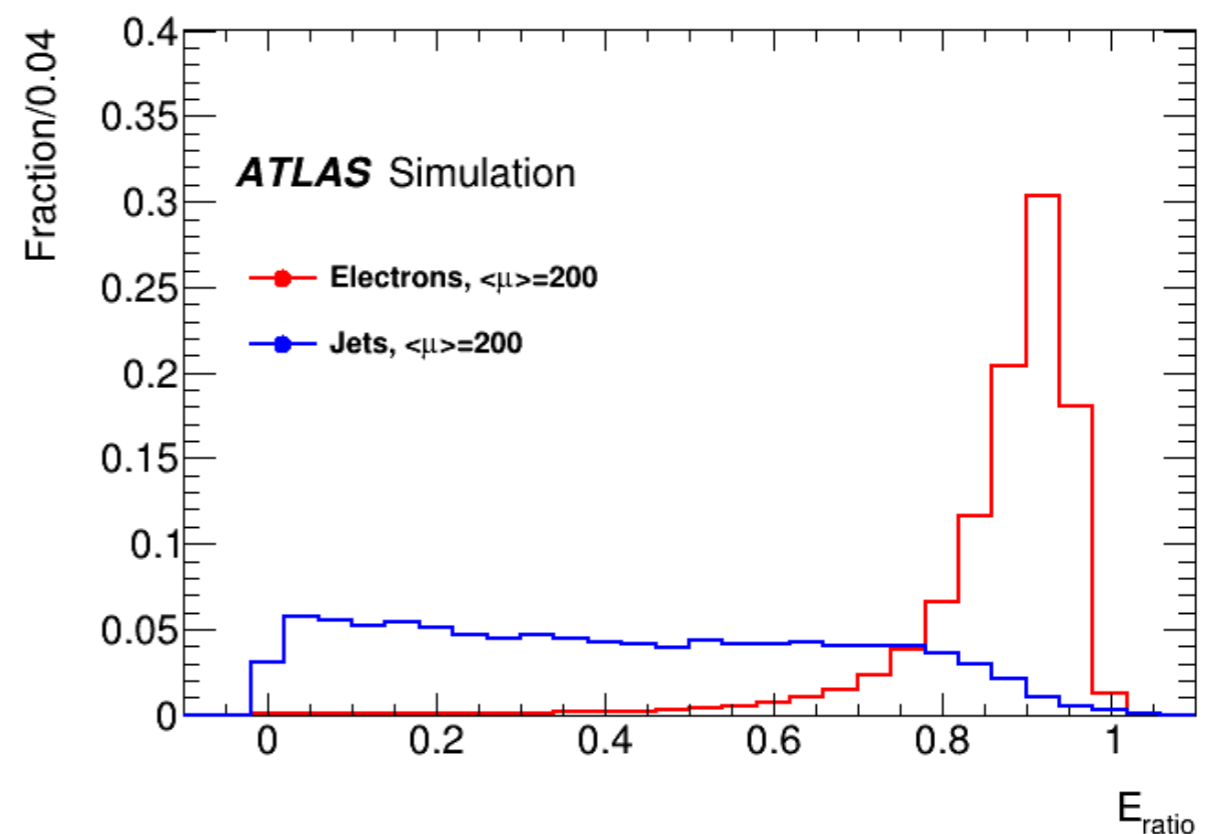
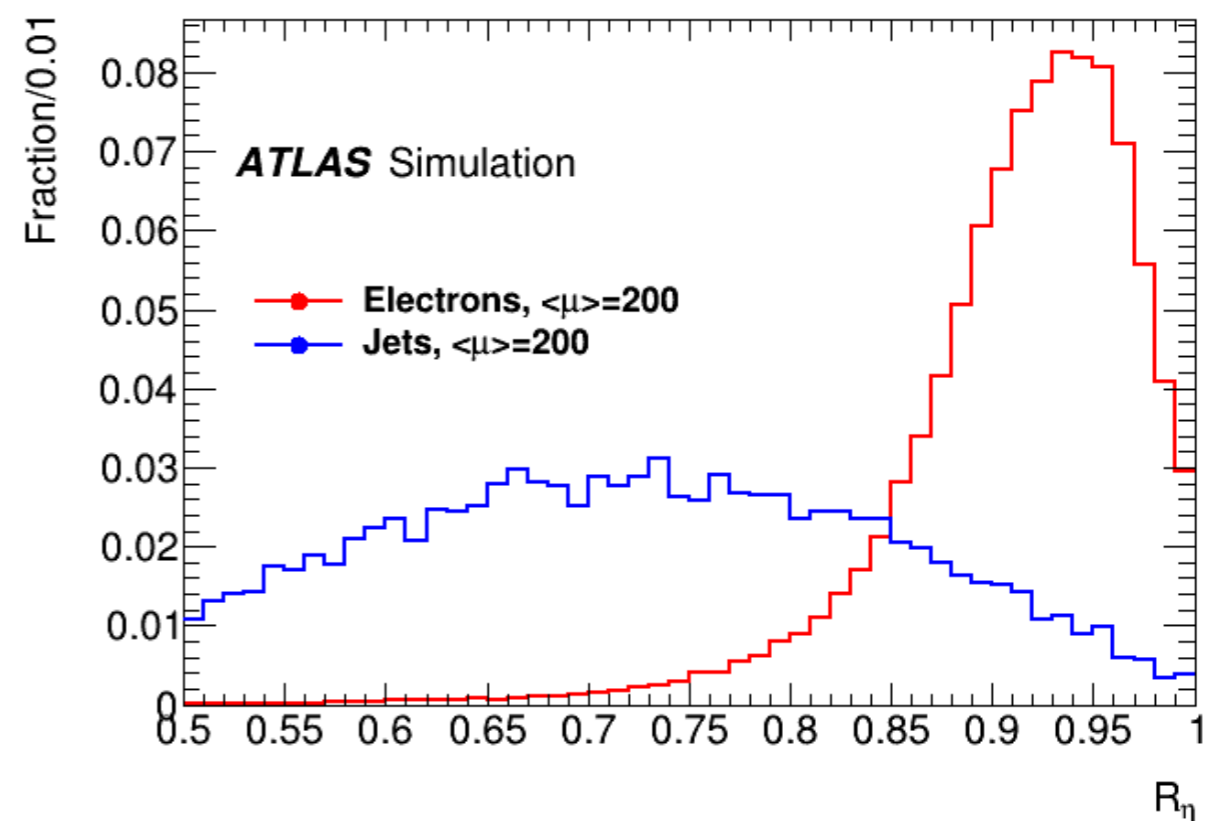
# LAr Calorimeter Electronics at the HL-LHC

- **Front-end LAr electronics** are located on the cryostat for analog performance.
  - Receive moderate radiation dose.
- HL-LHC ATLAS Trigger/DAQ upgrade:
  - ➔ **L0-only option: 10  $\mu$ s, 1 MHz**
  - ➔ **L0/L1 option: 10  $\mu$ s, 4 MHz / 35  $\mu$ s, 800 kHz**
- **New architecture:** switch from analog L1 pipeline to “free-running” all digital design.
  - ➔ Removes 100 kHz, 2.5  $\mu$ s constraint imposed by current electronics.
- **Partial upgrade is not possible.**
  - ➔ Replace all 1524 Front End Boards (FEBs),
  - ➔ and all 120 calibration boards,
  - ➔ and consequently the off-detector electronics.



# LAr Calorimeter - Triggering

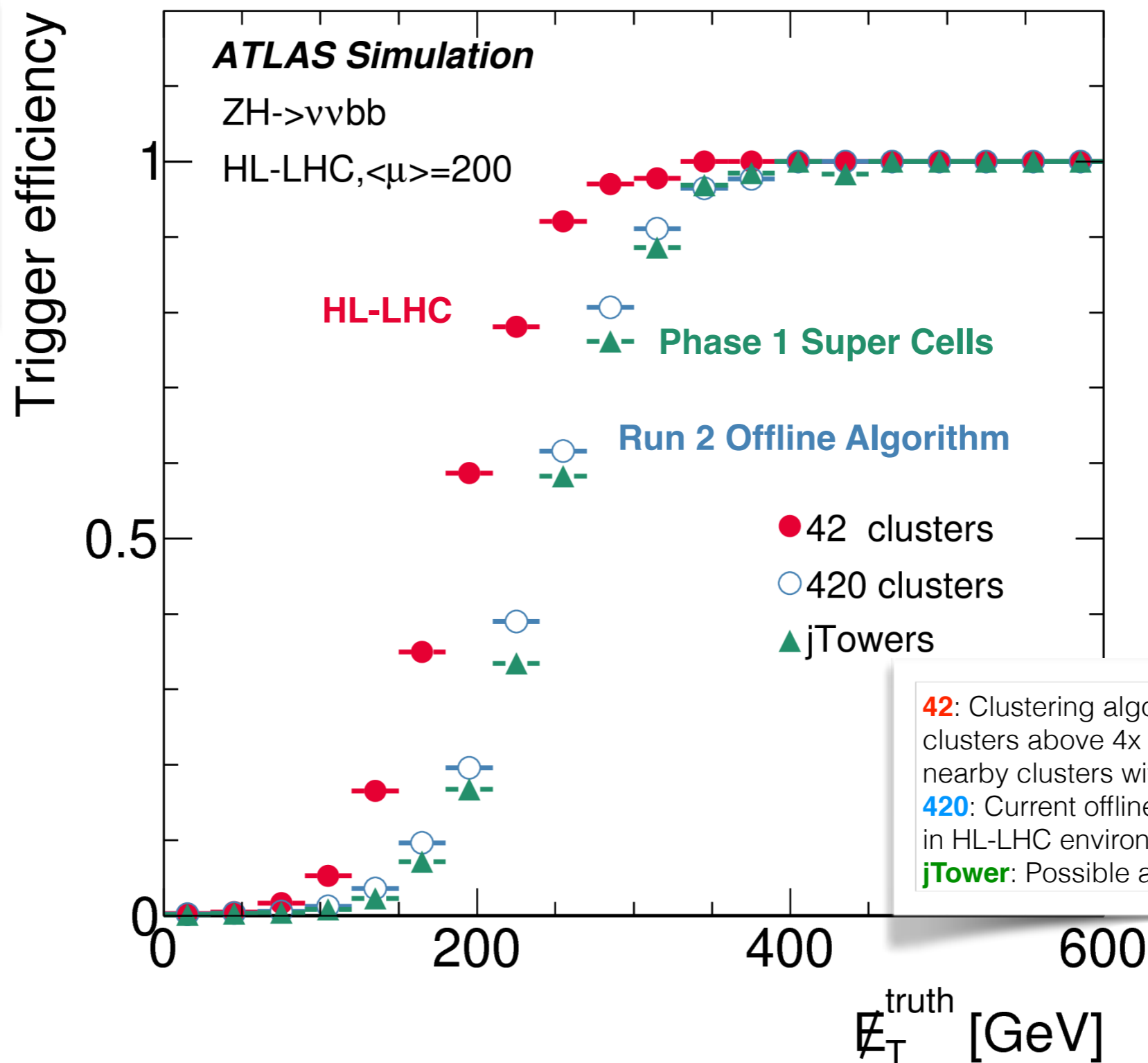
- Maintain ability to trigger on low  $p_T$  objects
  - Example: a 20 GeV  $e/\gamma$  - use EM shower shape variables at L1 to discriminate between  $e/\gamma$  objects and jets)
- New **Front-end electronics** implement digitization and readout of full granularity with full precision ( $\sim 180k$  channels over  $\sim 16$  bit dynamic range) at 40 MHz.
- New **Off-detector electronics** process this data, and provide resultant measurements as inputs to ATLAS HL-LHC trigger and DAQ system (and eventually offline).



# LAr Calorimeter - Triggering

- Full granularity/precision to trigger in turn provides sharper turn-on curves.

Ex: MET  
triggers for  
 $ZH \rightarrow \nu\nu bb$   
events with  
 $\langle \mu \rangle = 200$

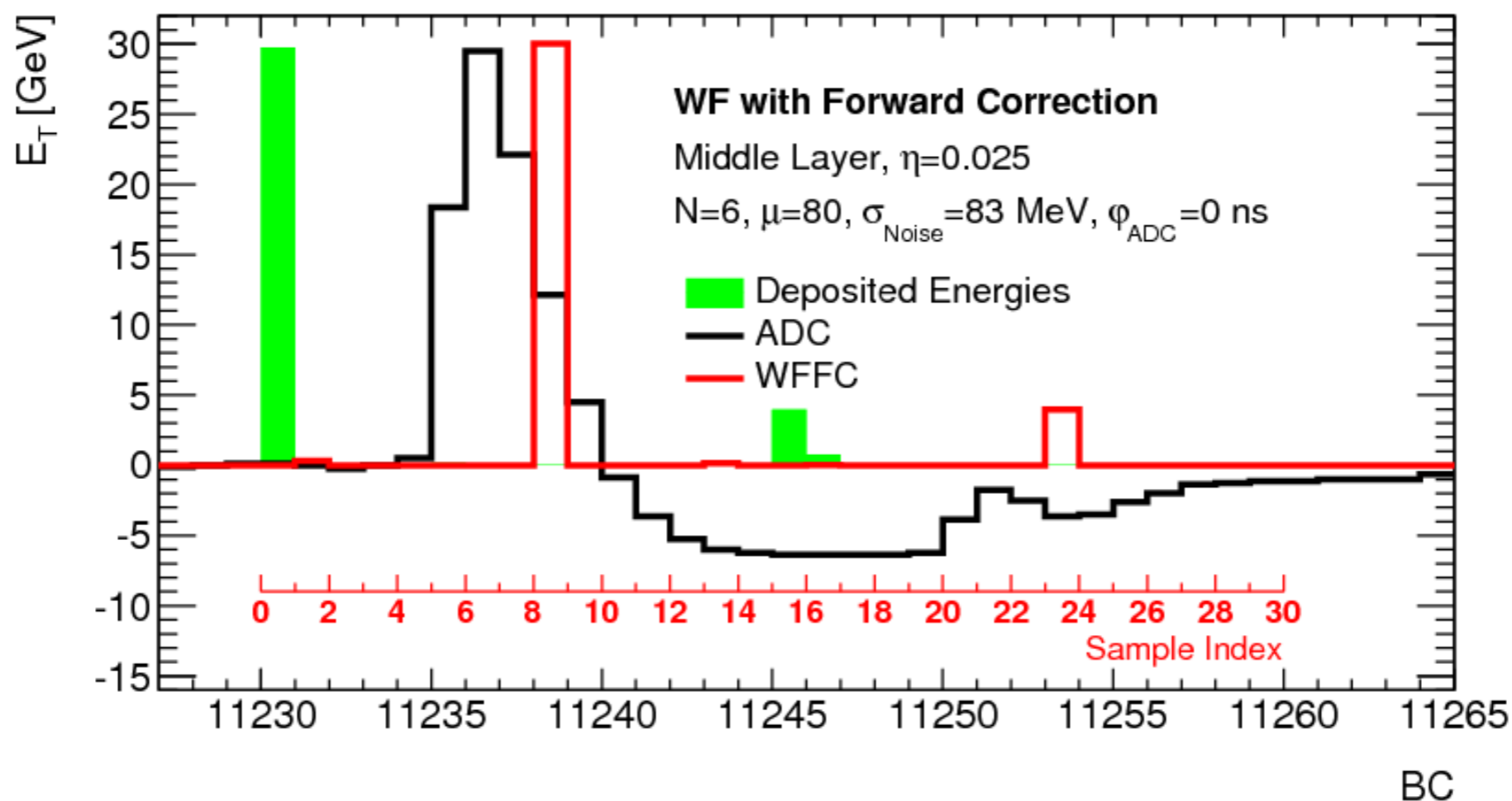
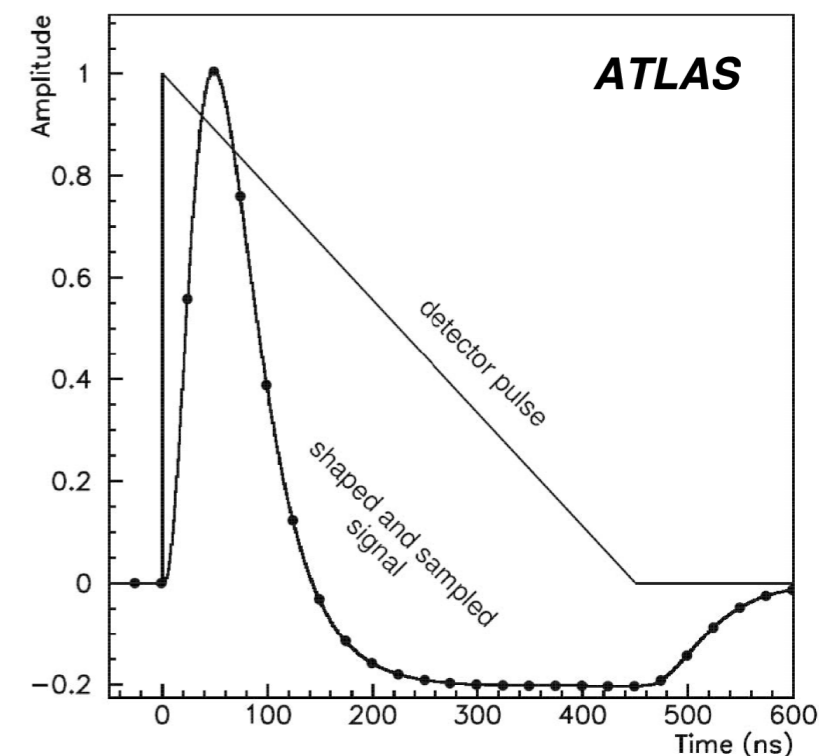


**42:** Clustering algorithm seeded with clusters above 4x noise, augmented with nearby clusters with 2x the noise.  
**420:** Current offline reconstruction applied in HL-LHC environment.  
**jTower:** Possible after Phase 1 upgrade.

# Energy Reconstruction at Cell-Level

## Use full history to determine energy:

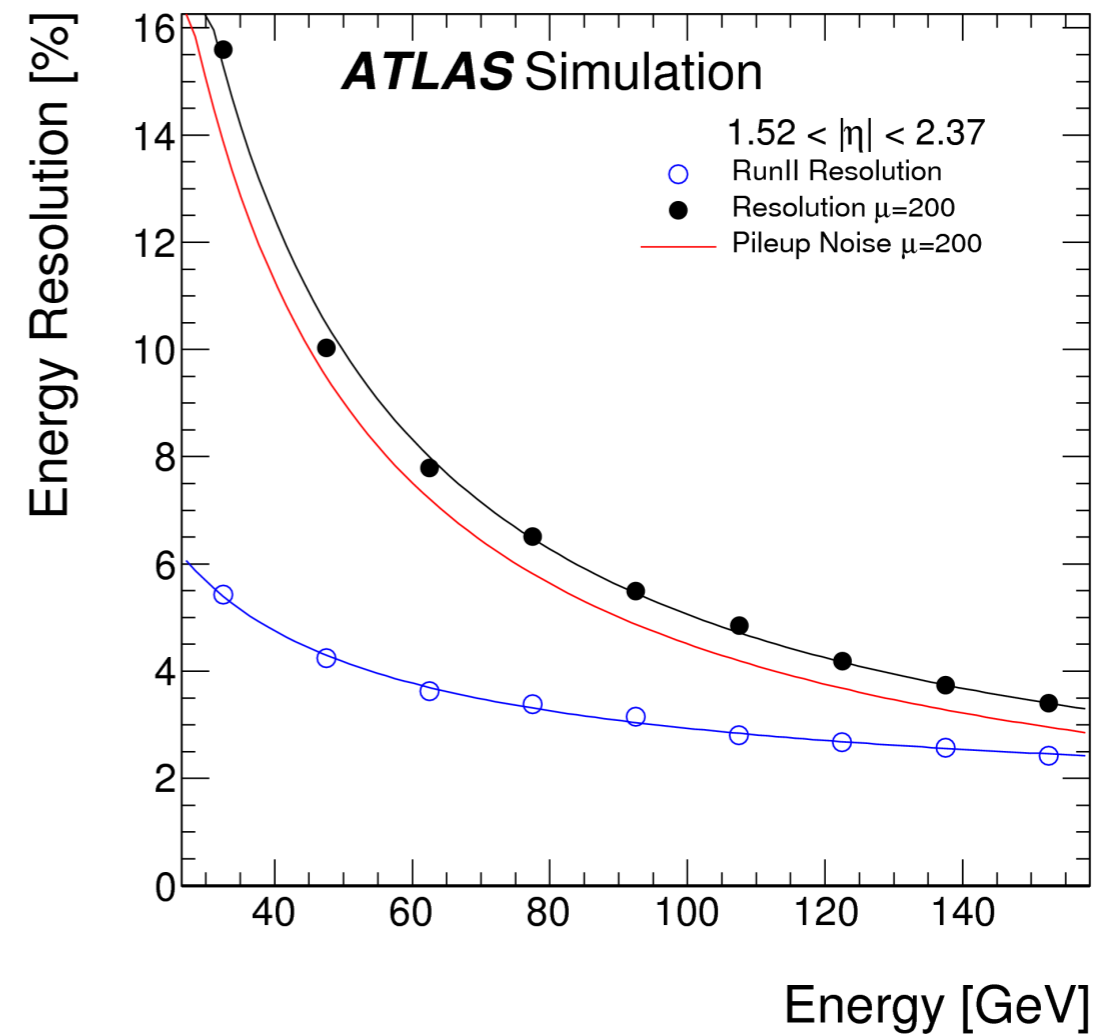
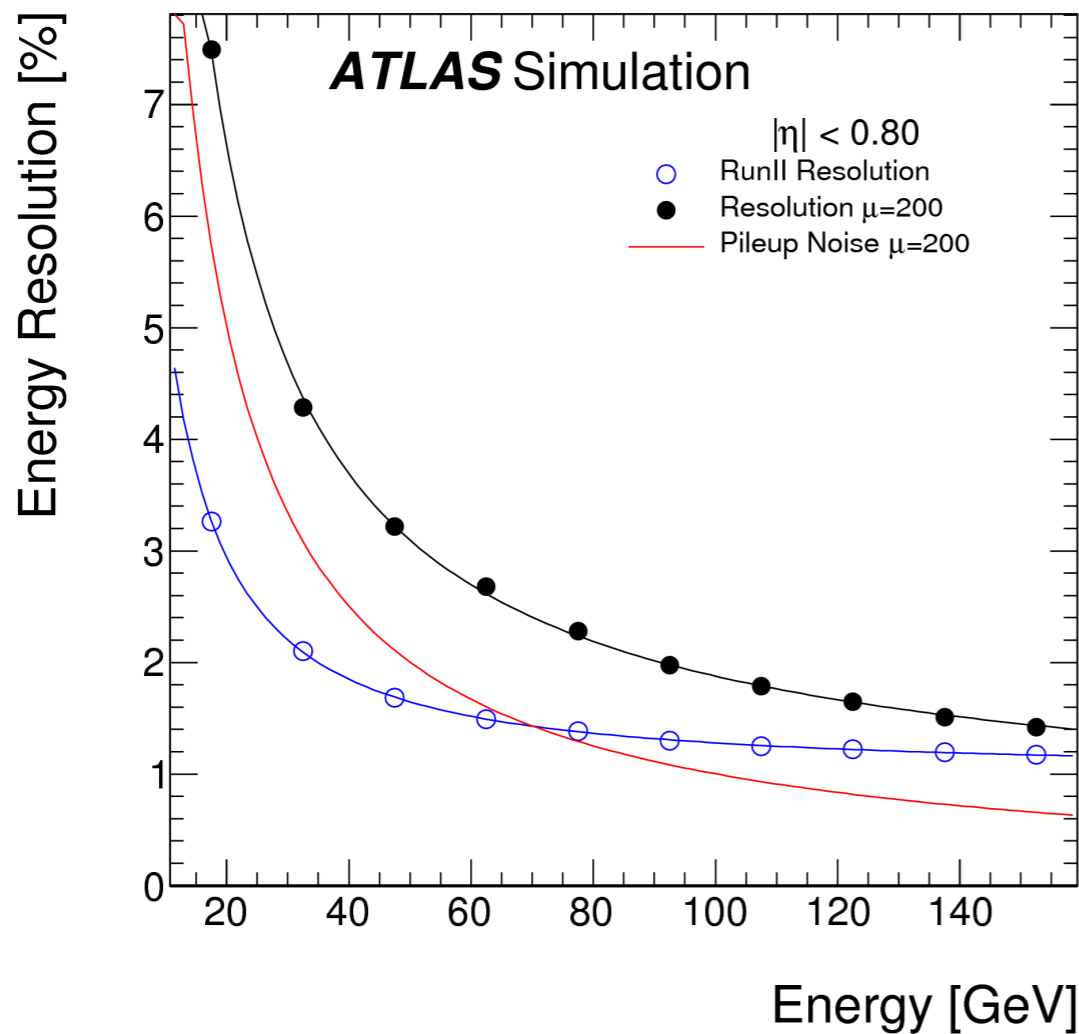
- Currently calculate energy deposited from weighted sum using Optimal Filter Coefficients (OFC) of 4 samples from signal waveform.
- Upgrade will provide continuous pulse train → allows for more advanced filtering.
  - Ongoing studies indicate better rejection of out-of-time pileup can be achieved.





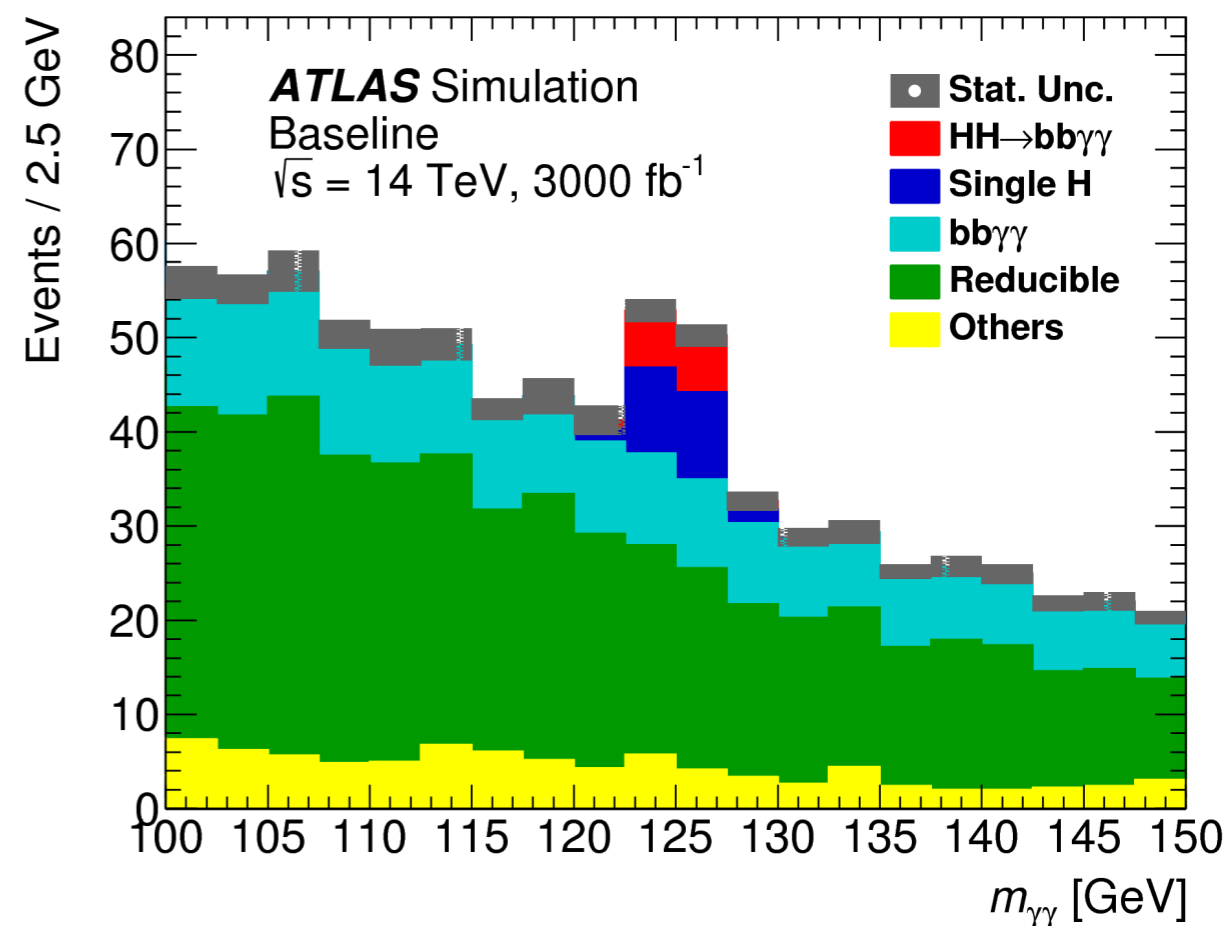
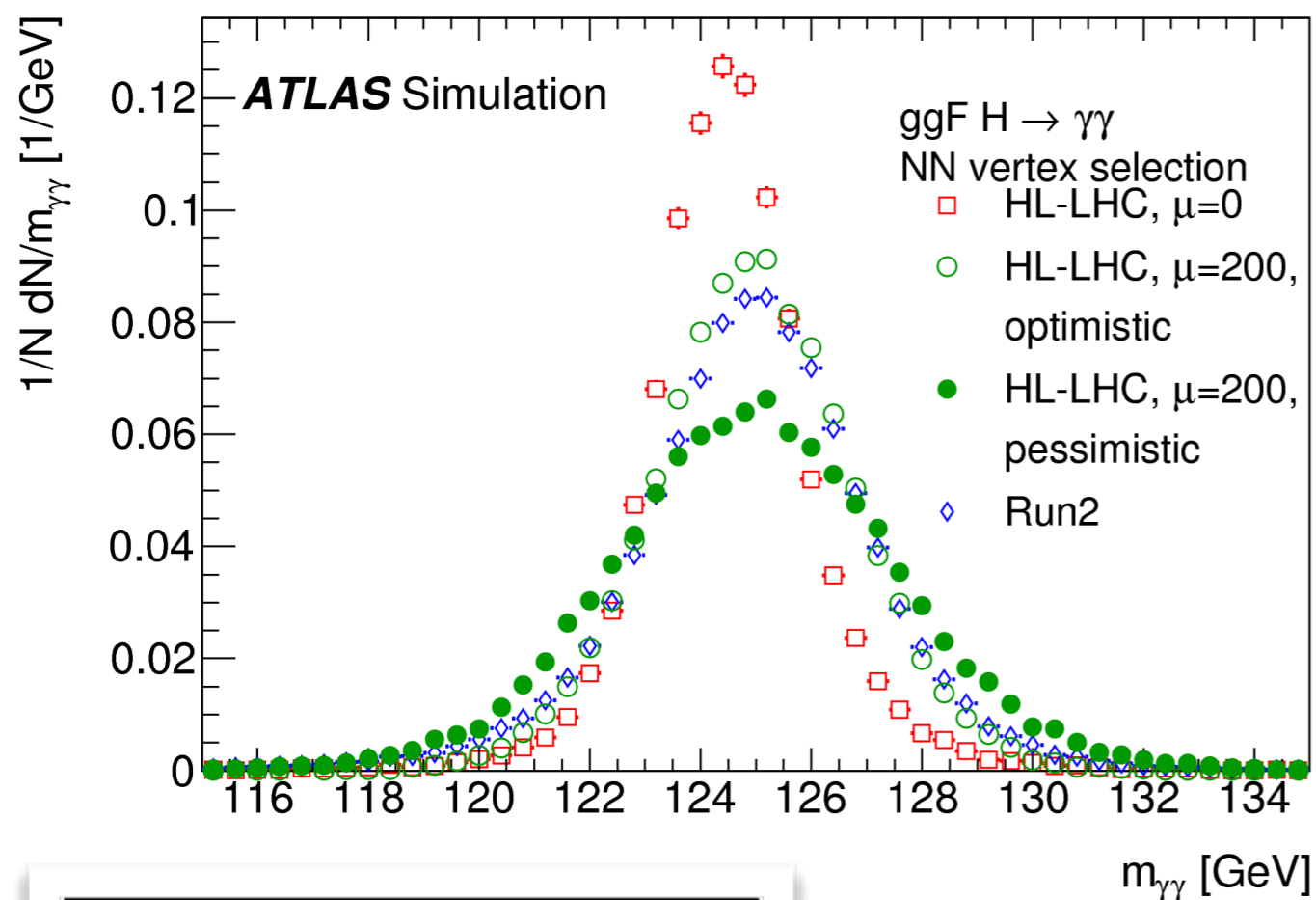
# Electron and Photon Reconstruction

- Electron and photon energy resolution is key to HL-LHC searches and measurements.
- Compare to Run 2 electron reconstruction algorithm, and same electronics noise and constant terms.



- Possible improvements: more advanced filters for better out-of-time pileup rejection, improved clustering algorithms, better track momentum measurement, particle-flow techniques, etc (studies on-going).

- $H \rightarrow \gamma\gamma$  mass resolution is critical to HL-LHC Higgs analyses.
- ★ Di-Higgs measurement is a key physics goal. Finding small, narrow diphoton mass peak on top of large backgrounds sets requirements on photon reconstruction and energy resolution.

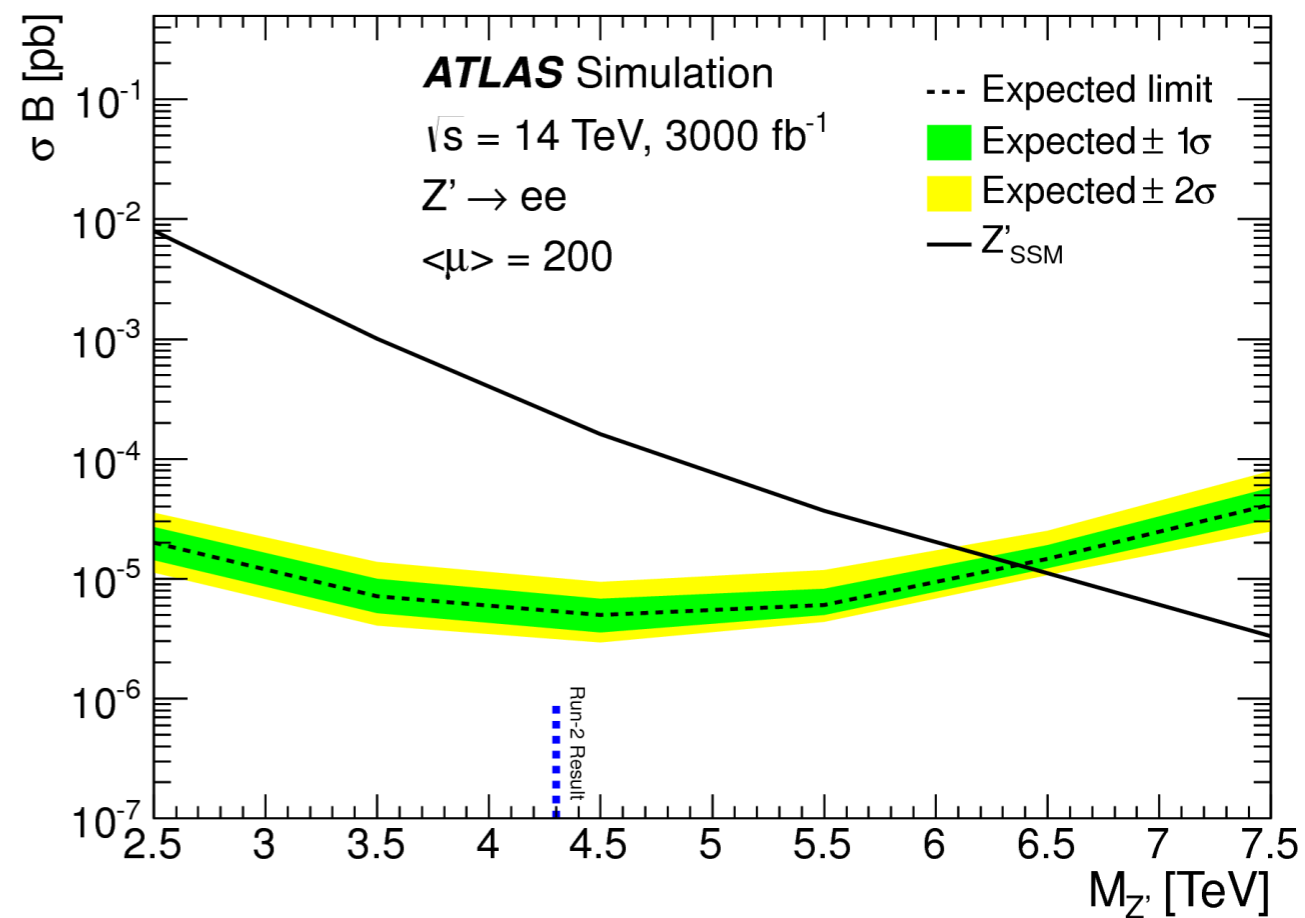
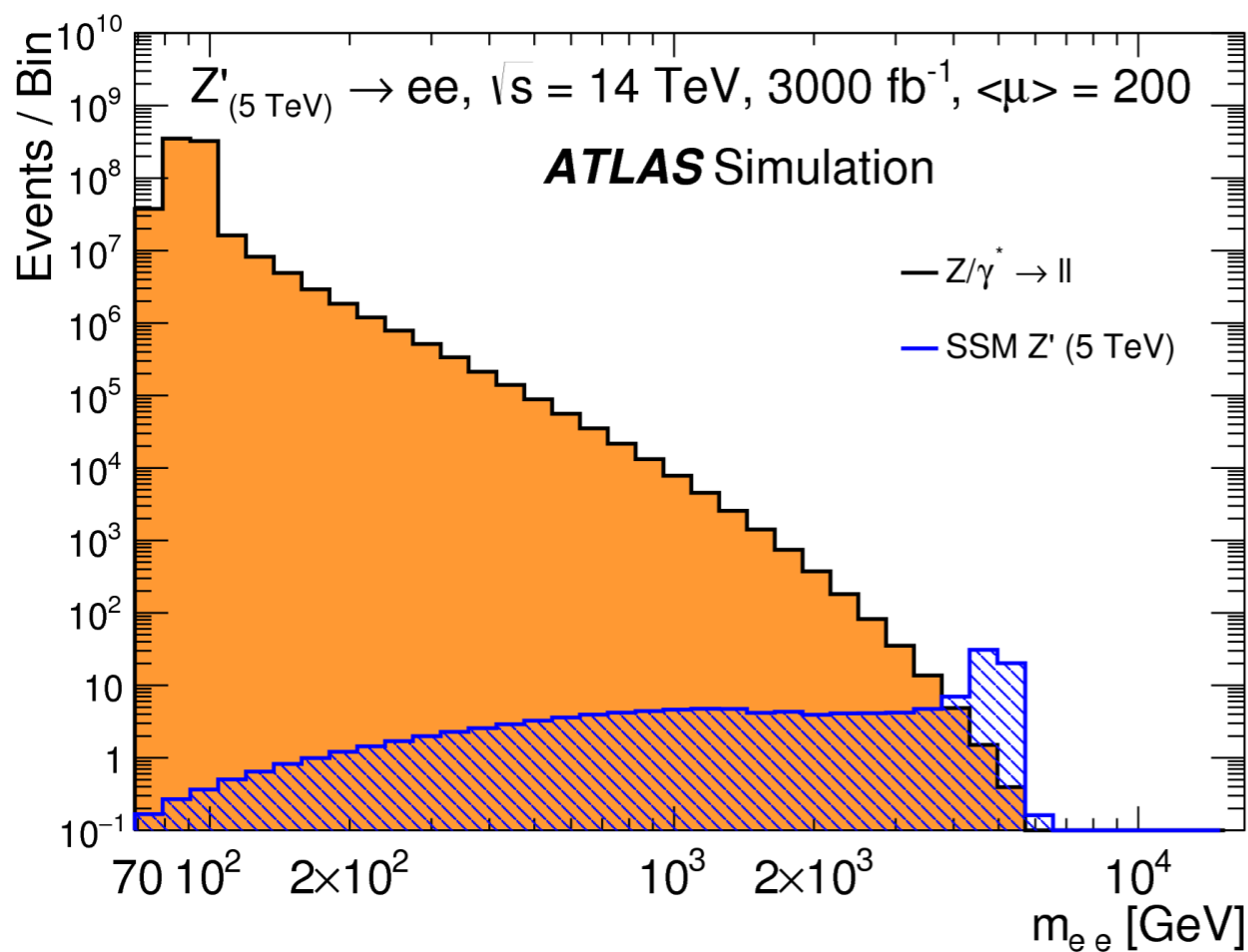


Resolutions [GeV]	ggF	HH
Pessimistic	2.64	2.06
Optimistic	1.99	1.62

# LAr Calorimeter and BSM Physics

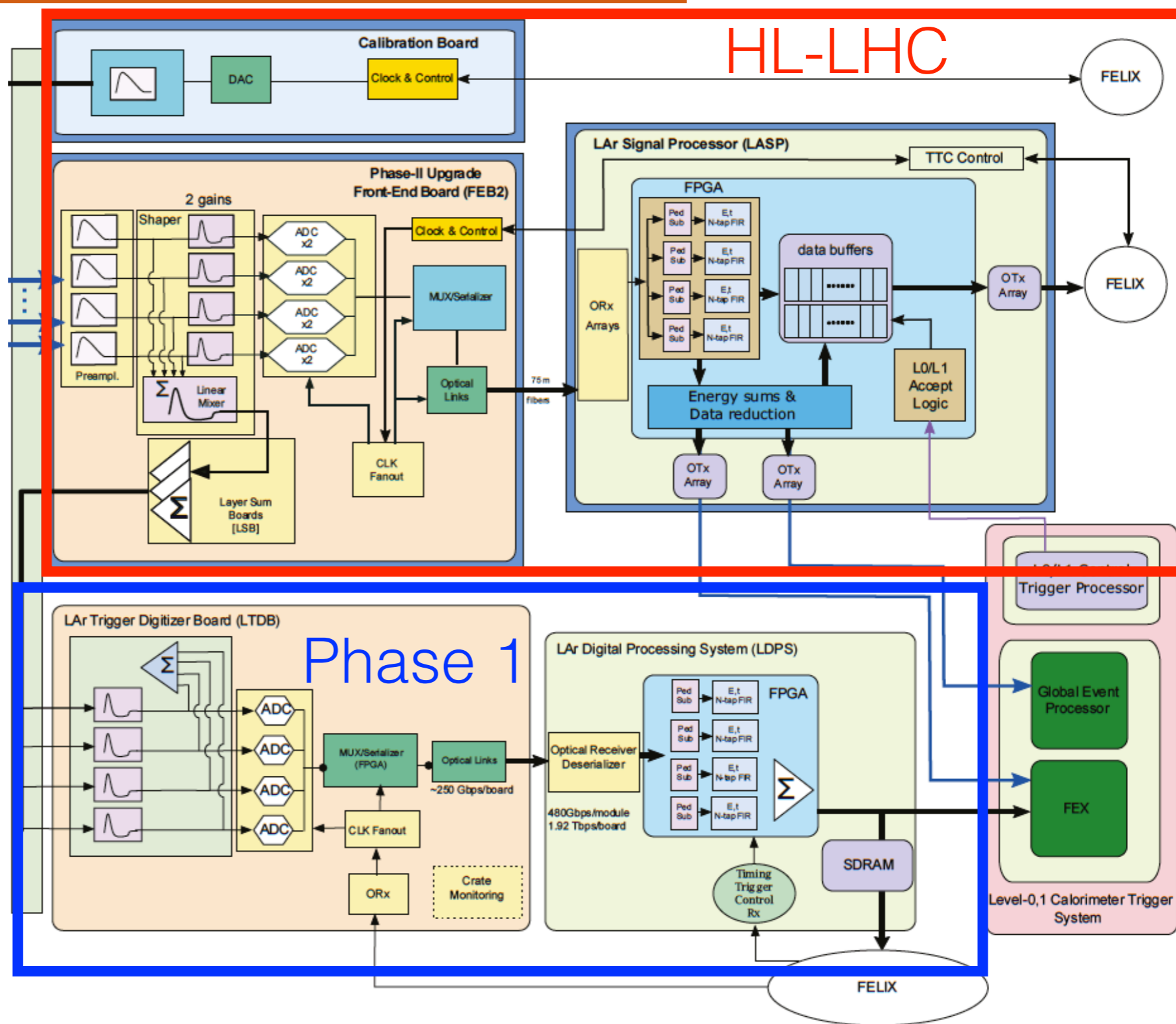
- $Z' \rightarrow ee$  search

★ Sets requirements on electron reconstruction and energy resolution at upper end of 16-bit dynamic range.



# Electronics Requirements

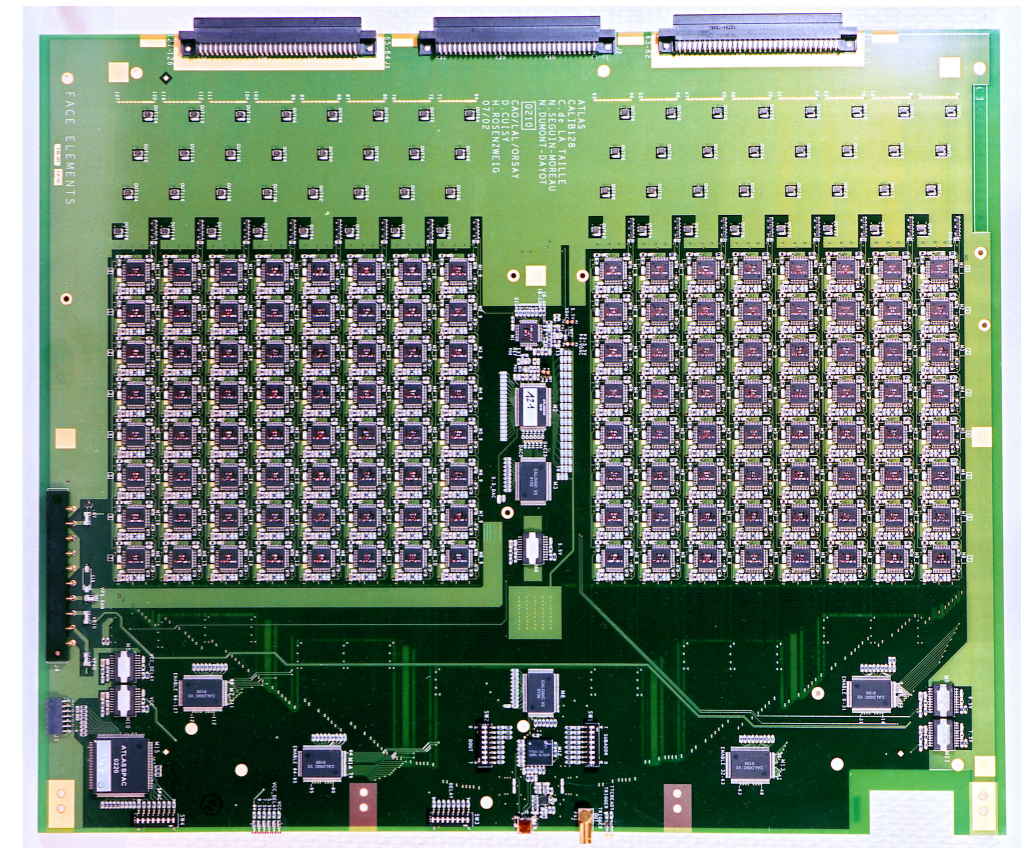
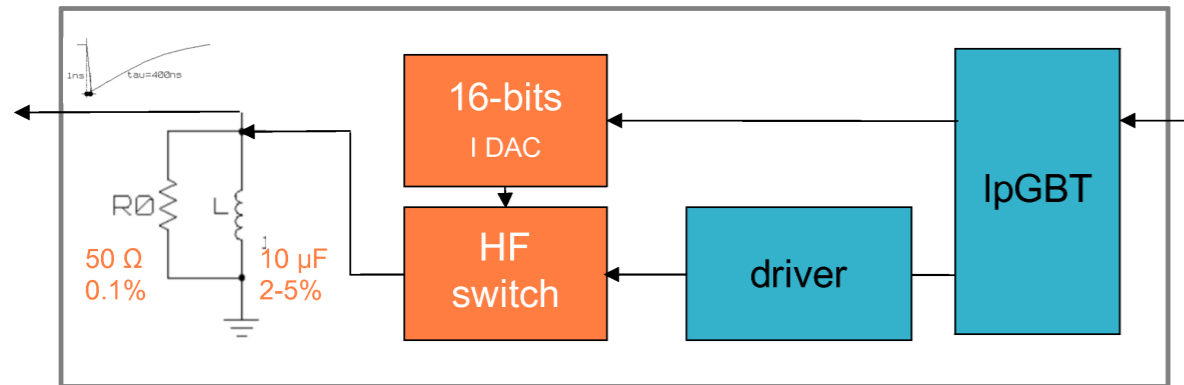
- Cover **full energy range** from electronics noise level to highest possible energy deposited in a single cell: 50 MeV to  $\sim 3$  TeV.
- **Linearity** of 0.1% up to  $\sim 10\%$  of the dynamic range.
- **Low electronics noise**, below intrinsic calorimeter resolution:
- Effective  **$\sim 11$ -bit precision** at high energy
- Equivalent precision in analog signal shaping
- **All data sent off-detector:**
  - 1.3 Gbps per channel if we send two gains
  - $\sim 180$  Gbps per front-end board
  - $\sim 275$  Tbps for the full LAr calorimeter.



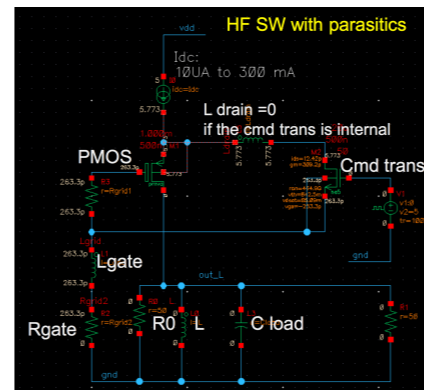
# Front-end Board and Calibration Board

## Calibration board

- Study possible improvements and hardware implications (calibration vs detector position, gain, time).

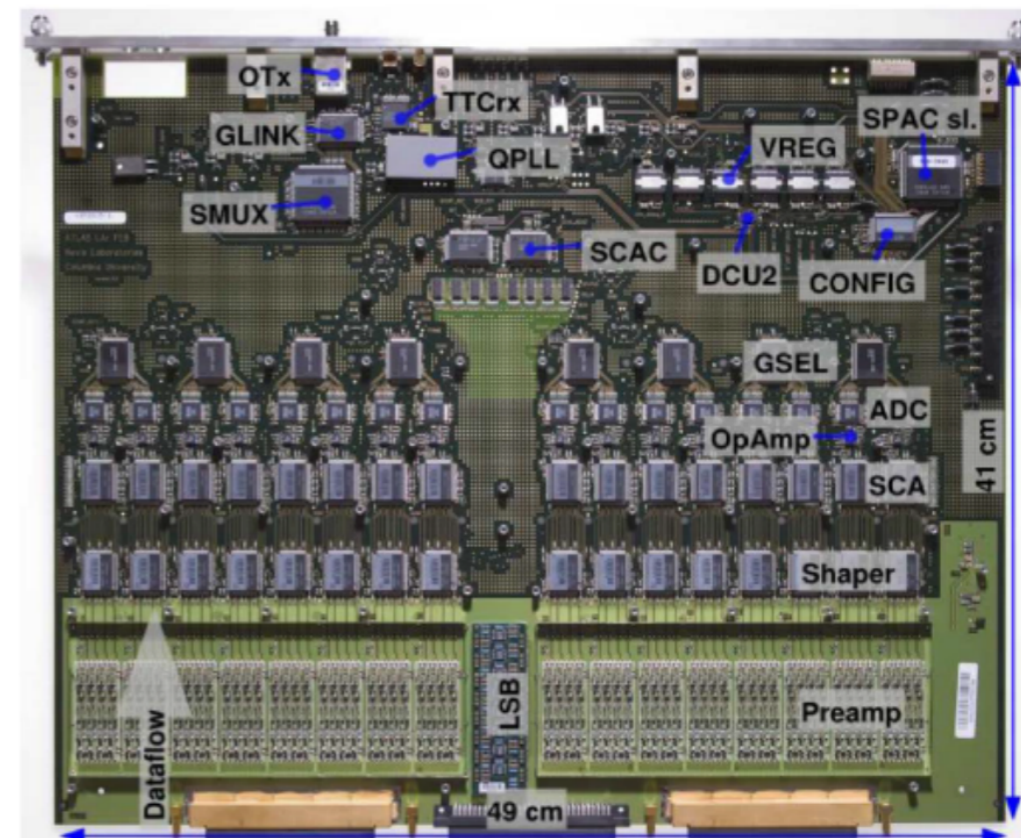


- High-frequency switch implementation in XFAB XT018.



## Front-end Board 2 (FEB2)

- Design based on current FEB:
  - Separate analog/digital
  - Well shielded/grounded
  - Shared power (1 - 4 V)
  - Individual control and clock
  - 22 data links + 2-4 control links/FEB2 (~35k links for system)



# Front-end : Pre-Amplifier and Shaper

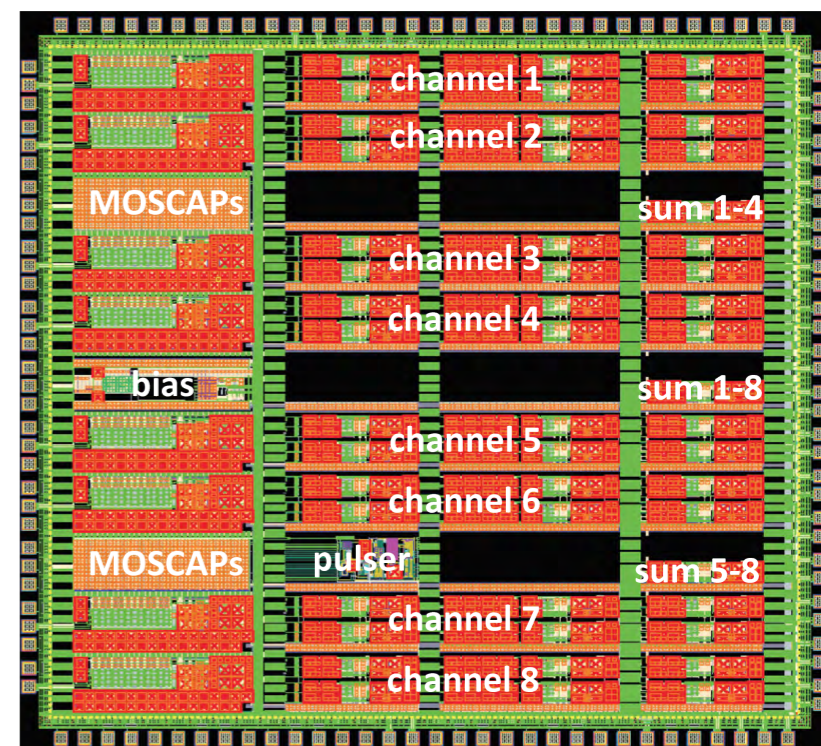
Preamp and shaper integrated on one chip.

**LAUROCO:** ASIC in **130 nm** CMOS

- Line-terminating preamp, electronically cooled resistor
- 8 channels, various gains

**HLC1:** ASIC in **65 nm** CMOS.

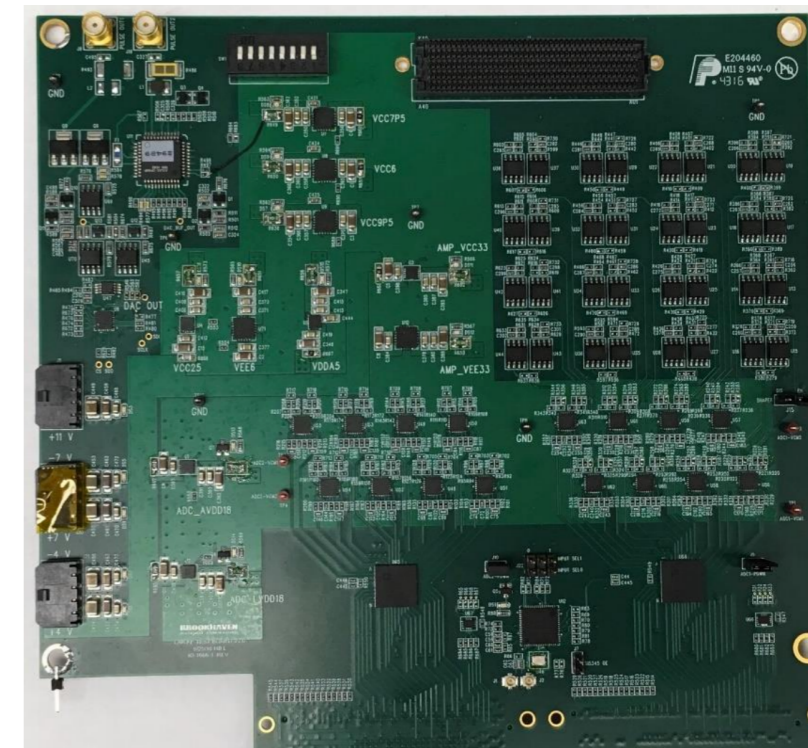
- 8 channels, 2 gains/channel, programmable peaking time, pulse generator.



**Testing:** Front-End Test board (FETB) for both ASICS. Consistent test results for both chips:

- Input impedance tuning
- INL ~0.1-0.3% in respective ranges
- Noise: 10% greater in LAUROCO vs HLC1, investigated (test-structure) and expect significant improvements for LAUROCO1.

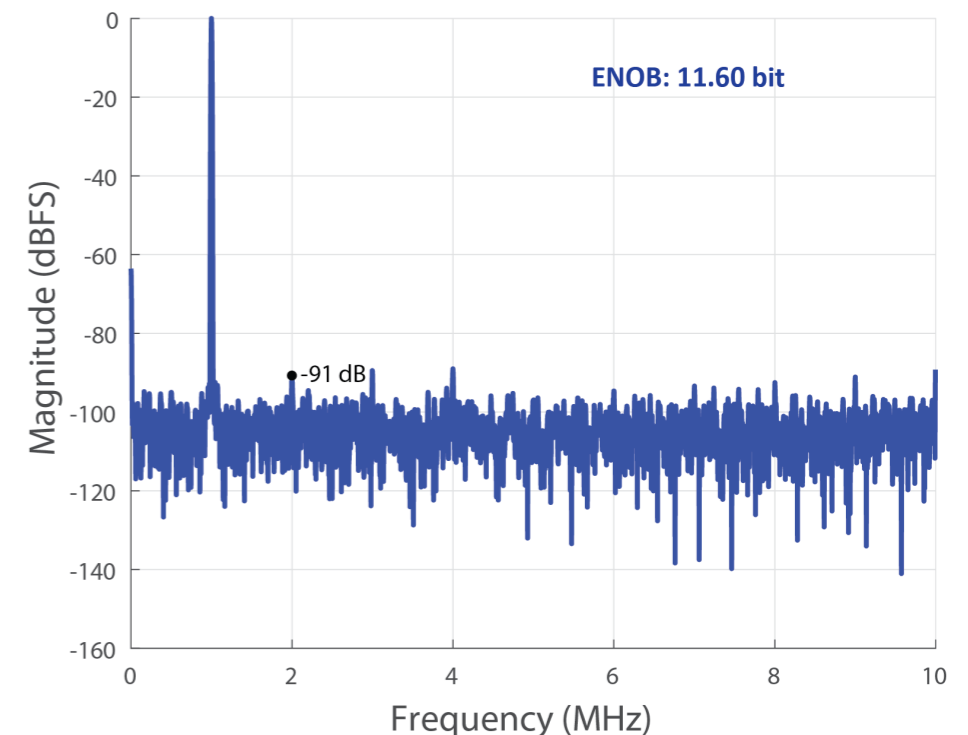
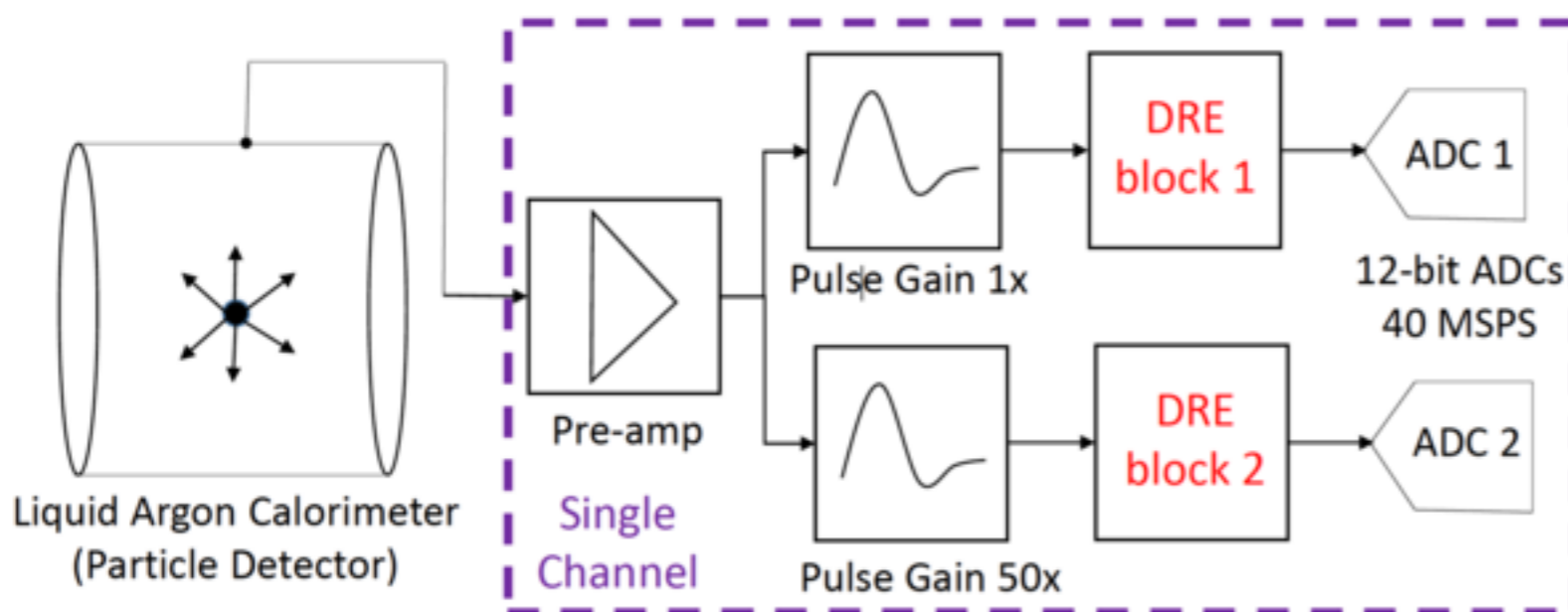
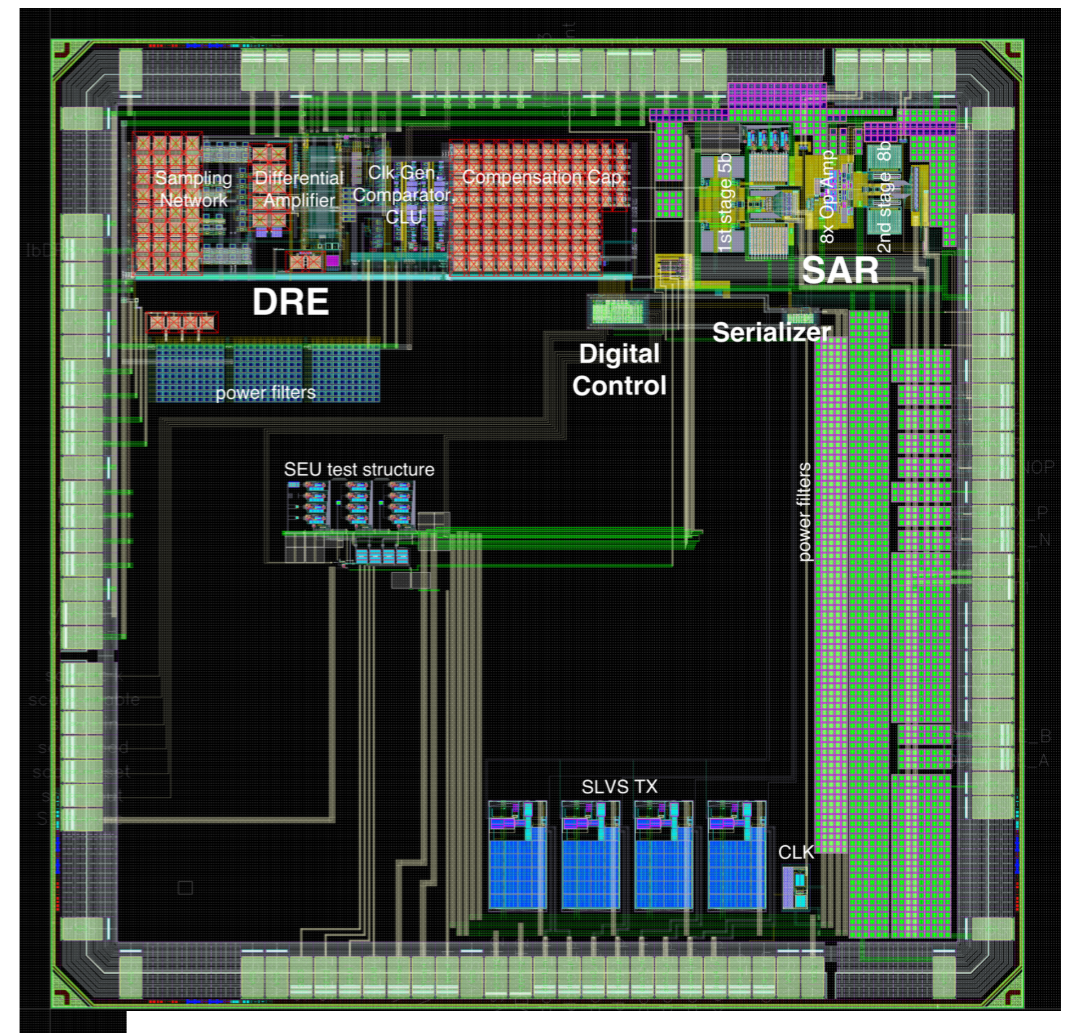
→ **Next version will merge two designs into one 130 nm chip**



# Front-end : Digitization

Several options under consideration:

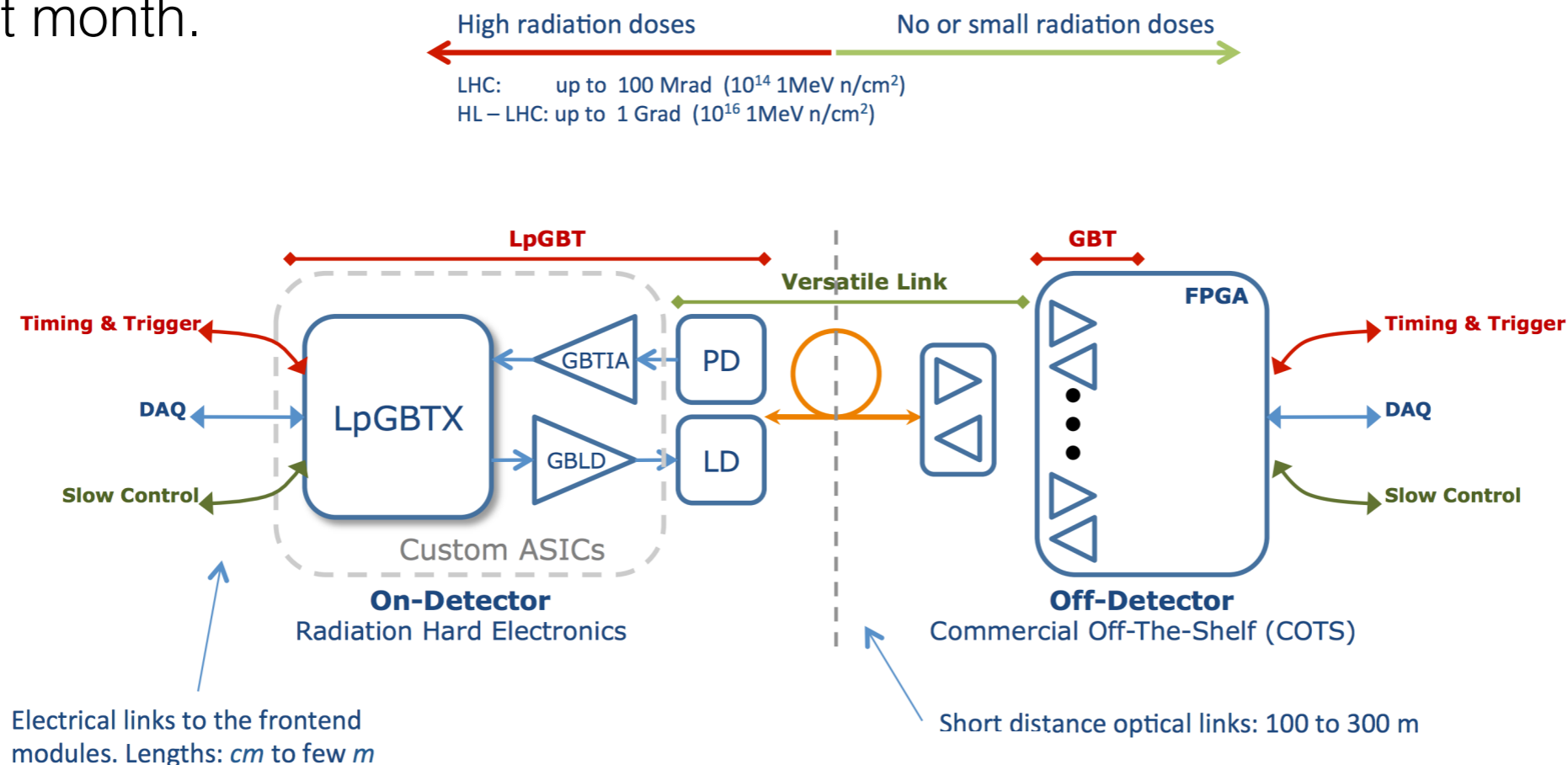
- ◆ Custom design, 40 MSPS **COLUTA ASIC** in 65 nm CMOS (right and below).
  - Architecture: Dynamic Range Extender (DRE) + 12-bit pipeline SAR ADC
  - 14b dynamic range, >11b precise SAR.
  - First version tested, version 2 submission next month.
- ◆ Purchase **ADC IP blocks** - 14b ADC design available in industry (i.e. S3 Group).
  - Would be integrated into custom ADC ASIC.



# Front-end : Optical Links and Power

**Links:** Each FEB readout by 22 ~9 Gbps, radiation tolerant optical links.

- Planning to use lpGBT and VL+, developed in CERN-based projects
- ATLAS LAr project is contributing to development, prototype submission next month.



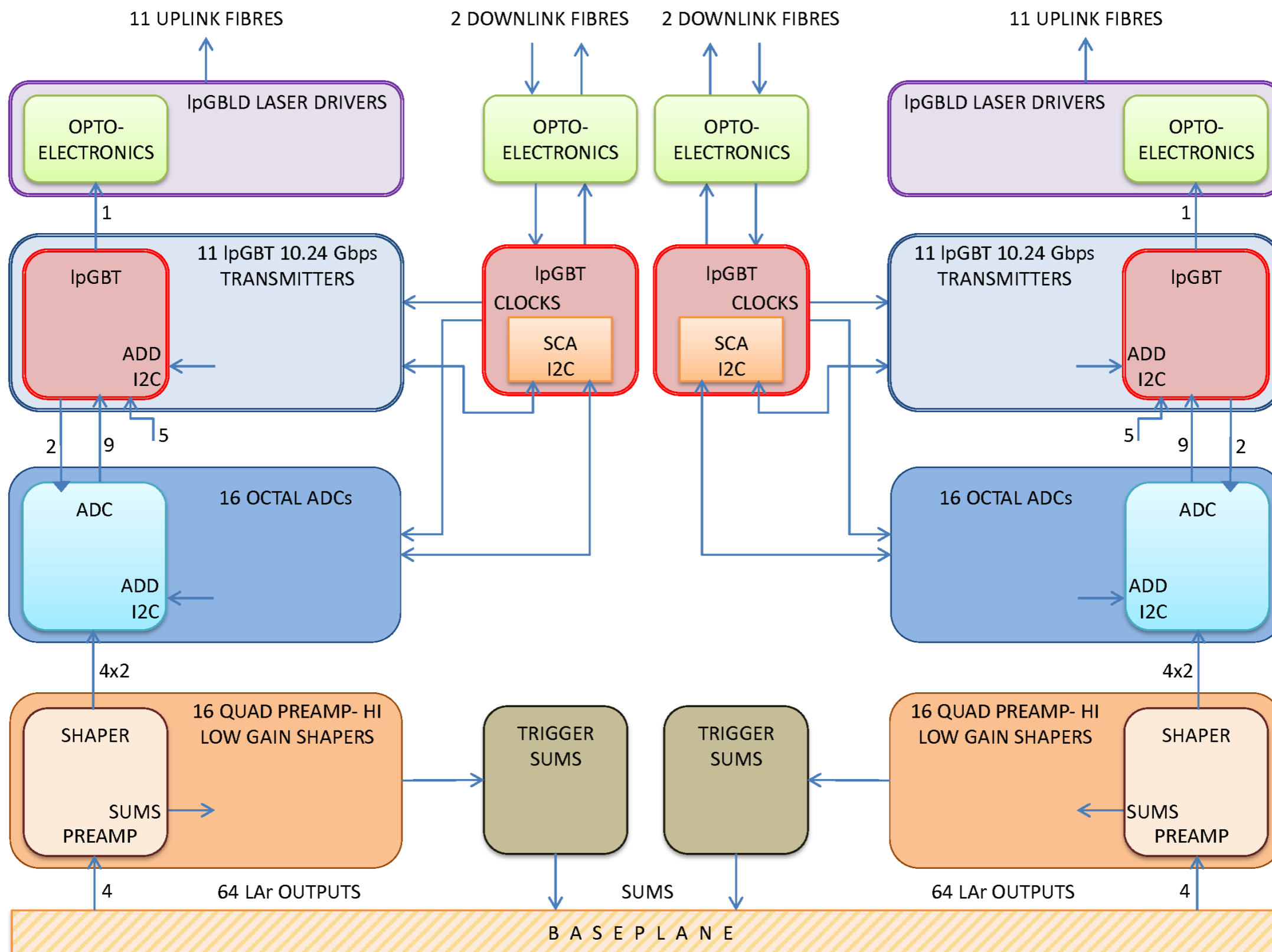
**Power distribution:** Replacing the LVPS for front-end crates.

- 280 V DC to 1 - 4 V devices with new, intermediate ~24 V step.
- Allows possibility of more accessible locations.
- Rad. qualified converters, long cables identified, under study.
- HEC LVPS will be replaced



# Front-end : Summary

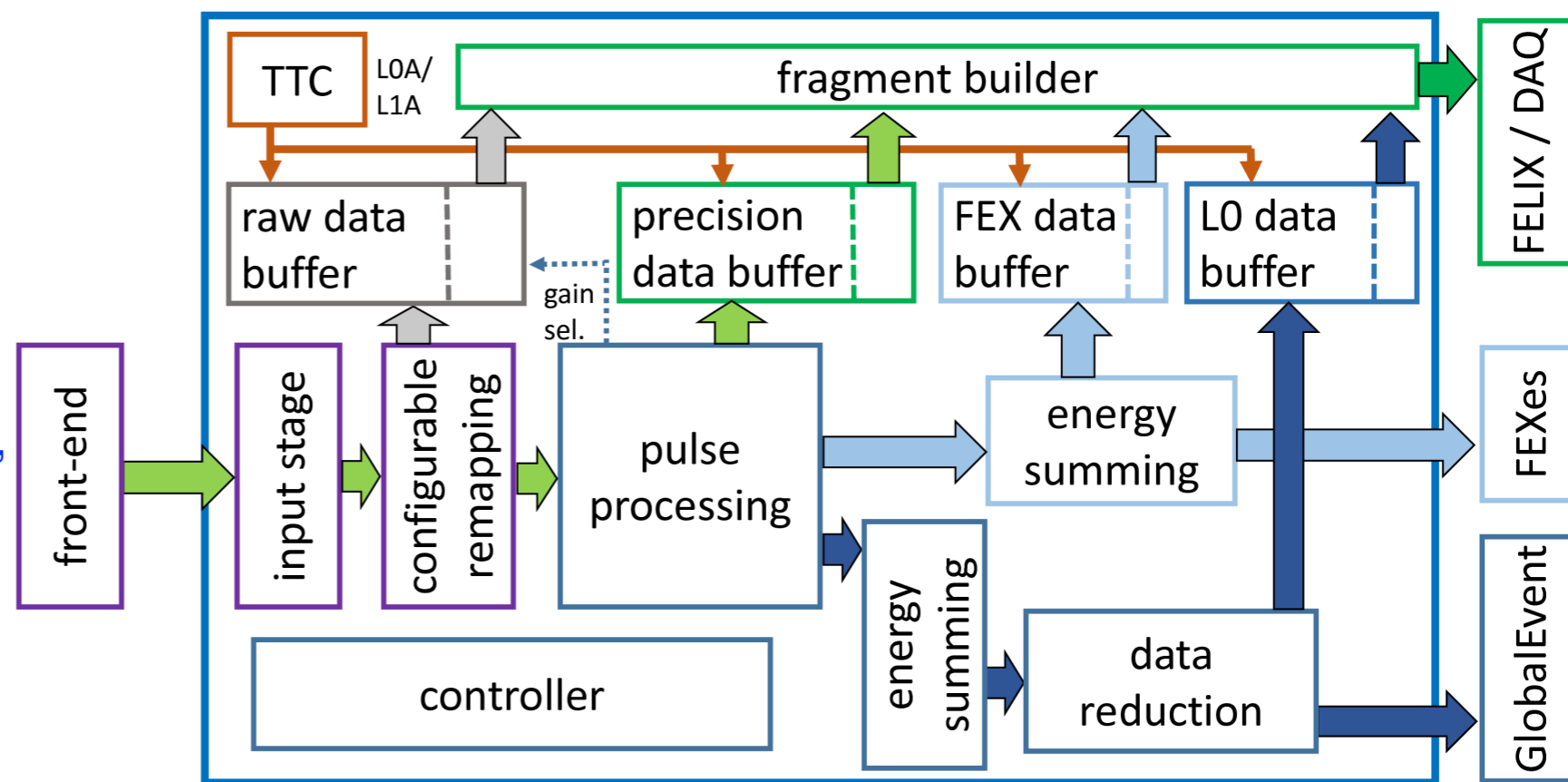
**Connections off detector:** IpGBT and VL+ serialize and transmits data off detector over 22 fibers. Clock and control data over four dedicated links,



# Off-detector Signal Processor

**LAr Signal Processor (LASP)** receives fully digitized signals from FE.

- Determines gain selection
- Calculates energy/time per cell
- Digital filtering + shaping to suppress pile-up and noise, based on bunch position.
- Long latency buffer until L0 or L1 accept.



Exploring Intel Stratix-10 FPGAs for first full test board.

Each LASP takes data from 4 FEB2 boards (4x more than Phase 1 LTDB).

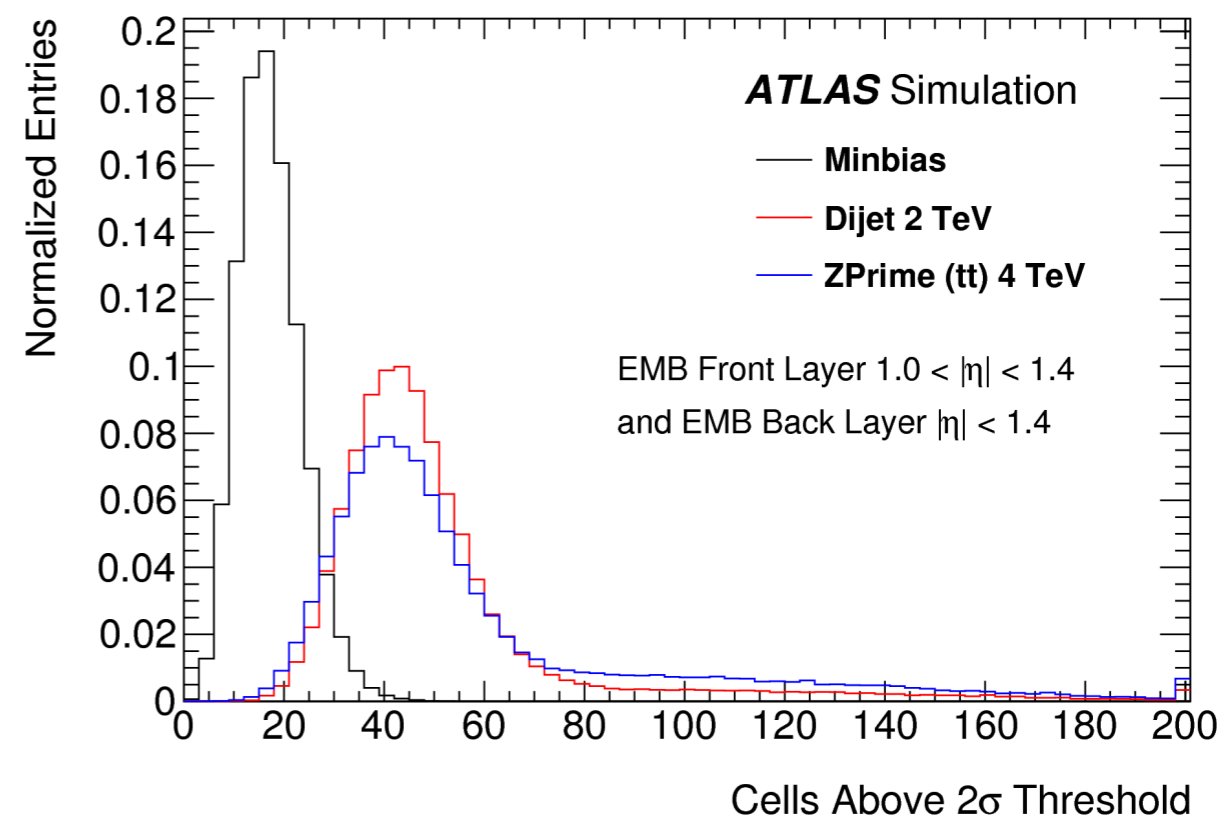
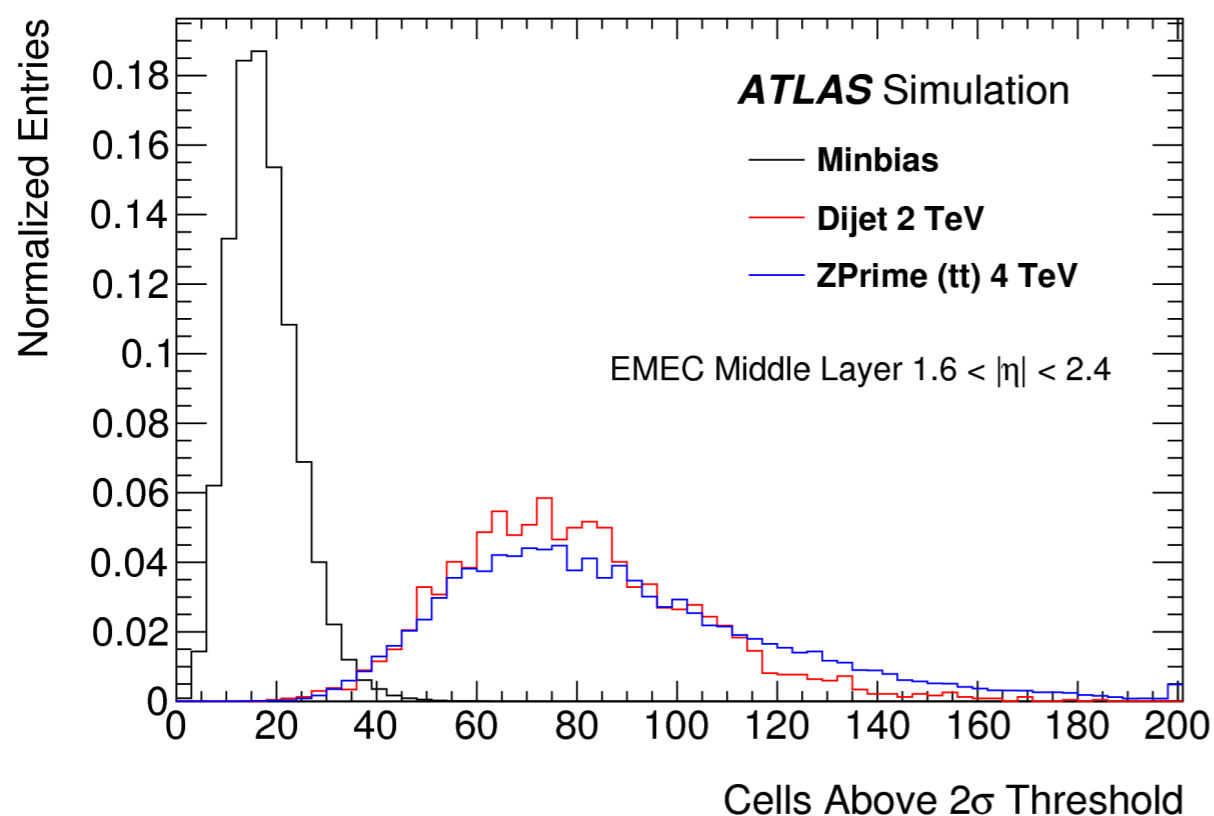
- 22 links/FEB2 (at ~9 Gbps)  
-> 30840 total: 100 Tx/Rx transceivers/FPGA.



★ **FPGA board cooling is a challenge.**

# Interface to Trigger/DAQ

- **LAr will deliver:** (either L0 or L0/L1 trigger scheme)
  - L0/L1 triggered data to DAQ via FELIX network interface
    - ➔ real-time energies above threshold to Global Event trigger processor.
- Data bandwidth and number of links to event processor depends on energy threshold (i.e. number of channel sent per event). With 2-sigma threshold we keep avg. 5% of cells.



## Calorimetry with LAr detectors will continue to be critical to the ATLAS physics program throughout the HL-LHC run.

- **All LAr electronics will be replaced for HL-LHC upgrade.**
  - Current system does not meet rate and latency requirements necessary for physics program at the HL-LHC
  - Current electronics and power supplies will not survive HL-LHC radiation!
- Many pieces are coming together. ASICs designed, tested, repeat...
  - progress on simulation and calibration,
  - and understanding off-detector processing and trigger interface.
- Technical Design Report headed to printers:  
<https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/UPGRADE/CERN-LHCC-2017-018>
- In parallel, **profit from Phase 1** upgrade experience.
  - Many challenges (and people) overlap.
- Looking forward to finalizing design and first prototypes.

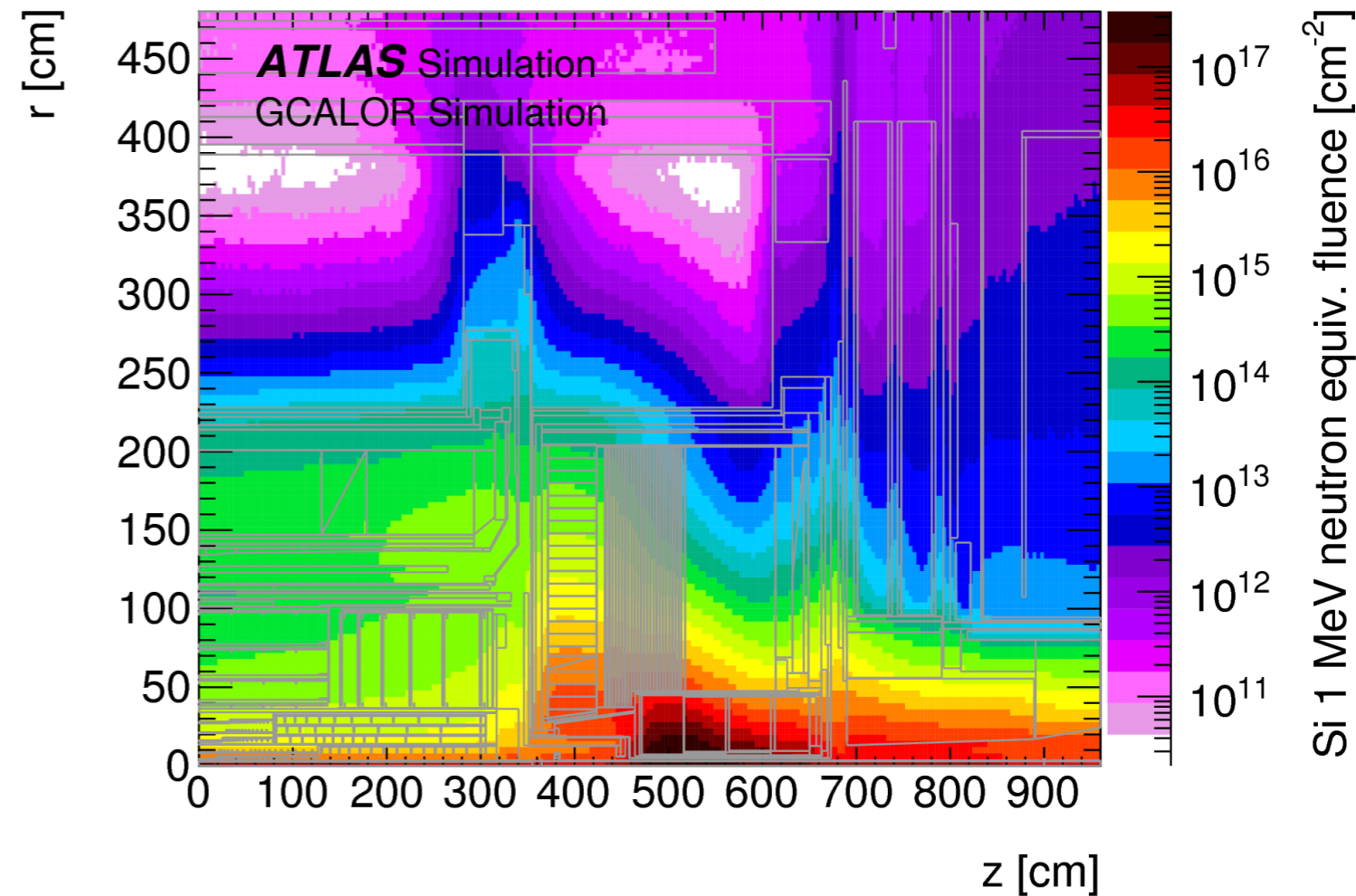


# On the path to the HL-LHC



# Radiation Tolerance

- Expected integrated HL-LHC luminosity of at least  $4000 \text{ fb}^{-1}$ .
- In-situ measurements allowed a reduction in safety factors on the simulated radiation levels for HL-LHC

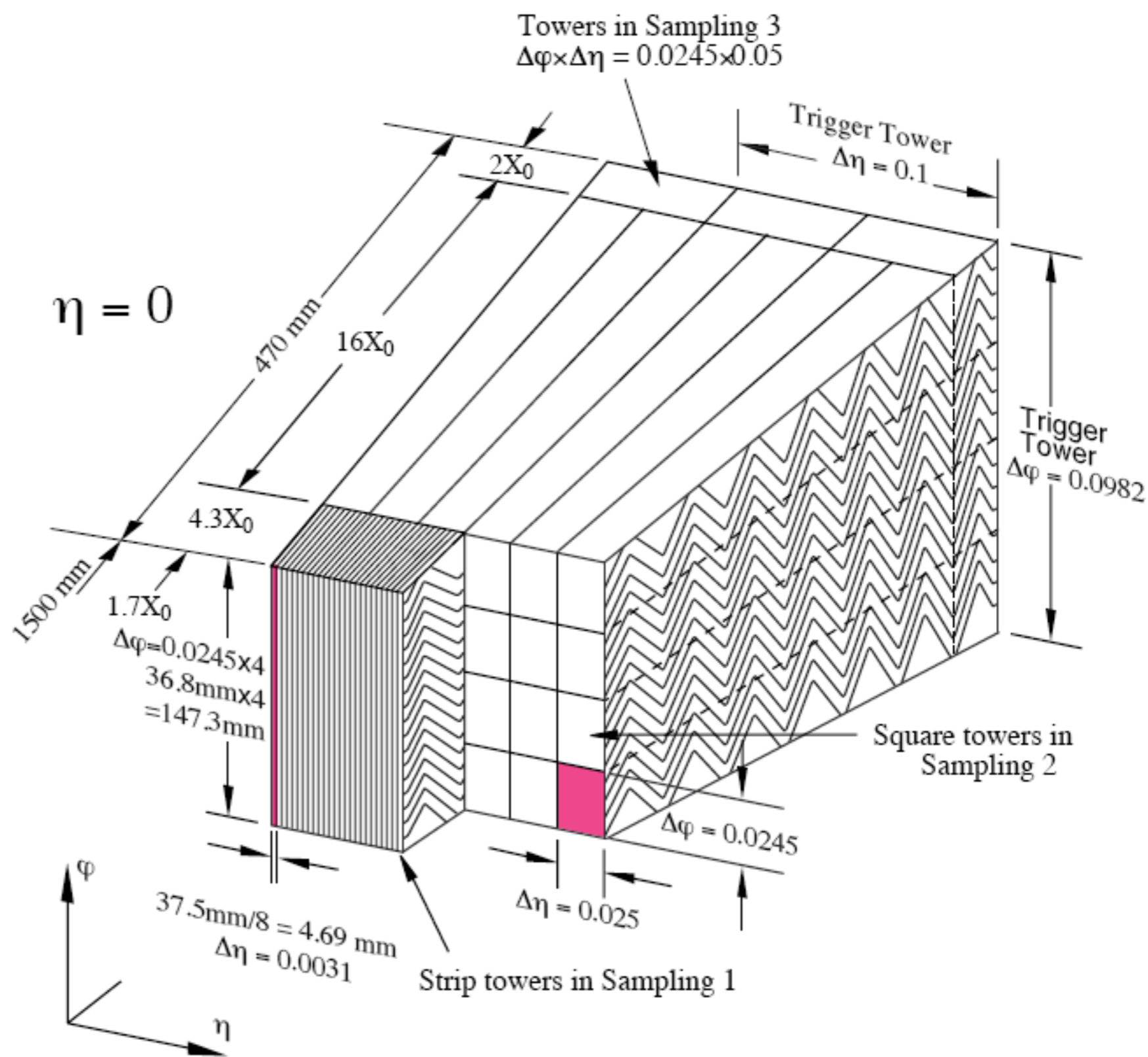


	TID [kGy]		NIEL [ $n_{\text{eq}}/\text{cm}^2$ ]		SEE [ $h/\text{cm}^2$ ]	
ASIC	2.26	(2.25)	$4.9 \times 10^{13}$	(2)	$7.7 \times 10^{12}$	(2)
COTS (multiple lots)	30.2	(30)	$19.6 \times 10^{13}$	(8)	$3.1 \times 10^{13}$	(8)
COTS (single-lot)	7.5	(7.5)	$4.9 \times 10^{13}$	(2)	$7.7 \times 10^{12}$	(2)
LVPS between TileCal fingers (barrel)	6.0	(30)	$4.4 \times 10^{13}$	(8)	$8.0 \times 10^{12}$	(8)
LVPS at PP2 (barrel)	0.39	(30)	$2.4 \times 10^{12}$	(8)	$3.4 \times 10^{11}$	(8)
LVPS between TileCal fingers (endcap)	4.26	(30)	$9.8 \times 10^{12}$	(8)	$1.5 \times 10^{12}$	(8)
HEC LVPS	0.32	(2.25)	$2.4 \times 10^{12}$	(2)	$3.8 \times 10^{11}$	(2)

# Detector Segmentation

- **Current Level-1 trigger**

- Max L1 latency =  $2.5 \mu\text{s}$
- Max L1 rate = 100 kHz read-out.
- Sum (typ.) 60 channels to build L1 Trigger Towers (granularity  $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ , no longitudinal segmentation). Limits discrimination between  $e/\gamma$  objects and jets.

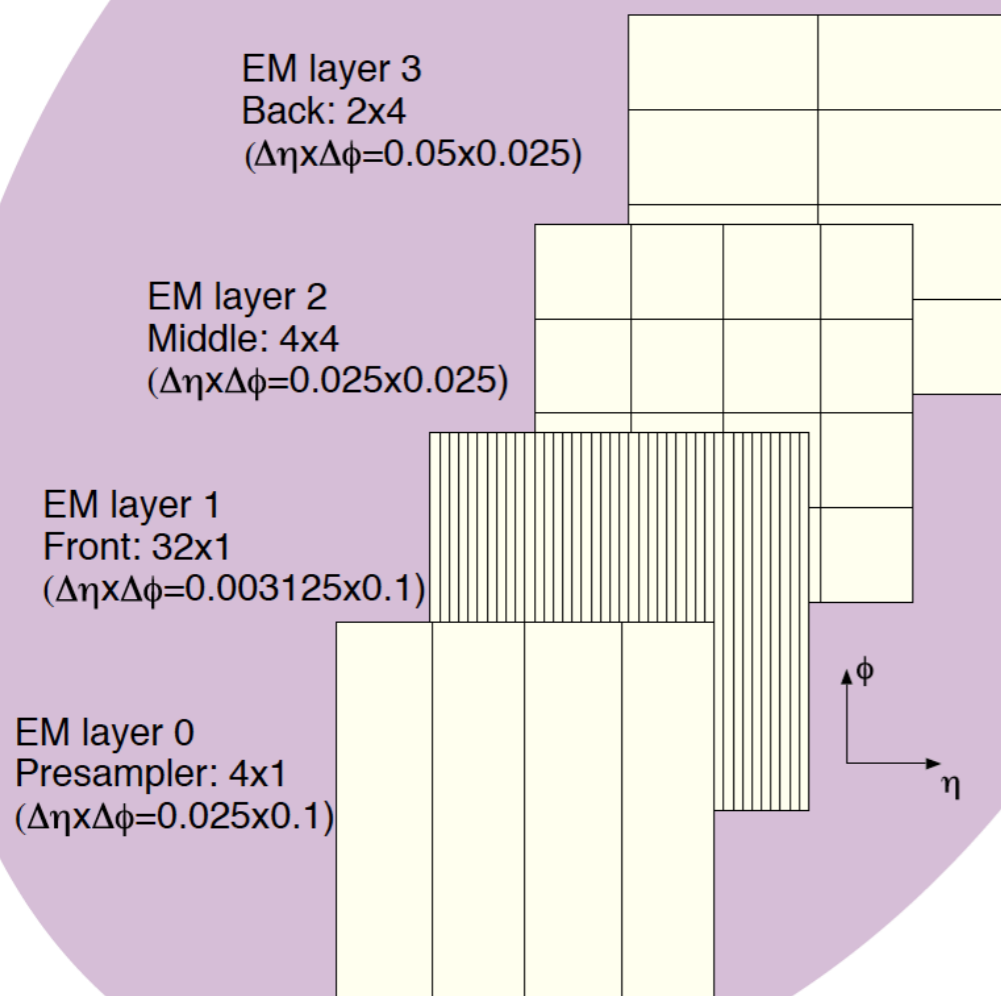




# Phase 1 Super cells

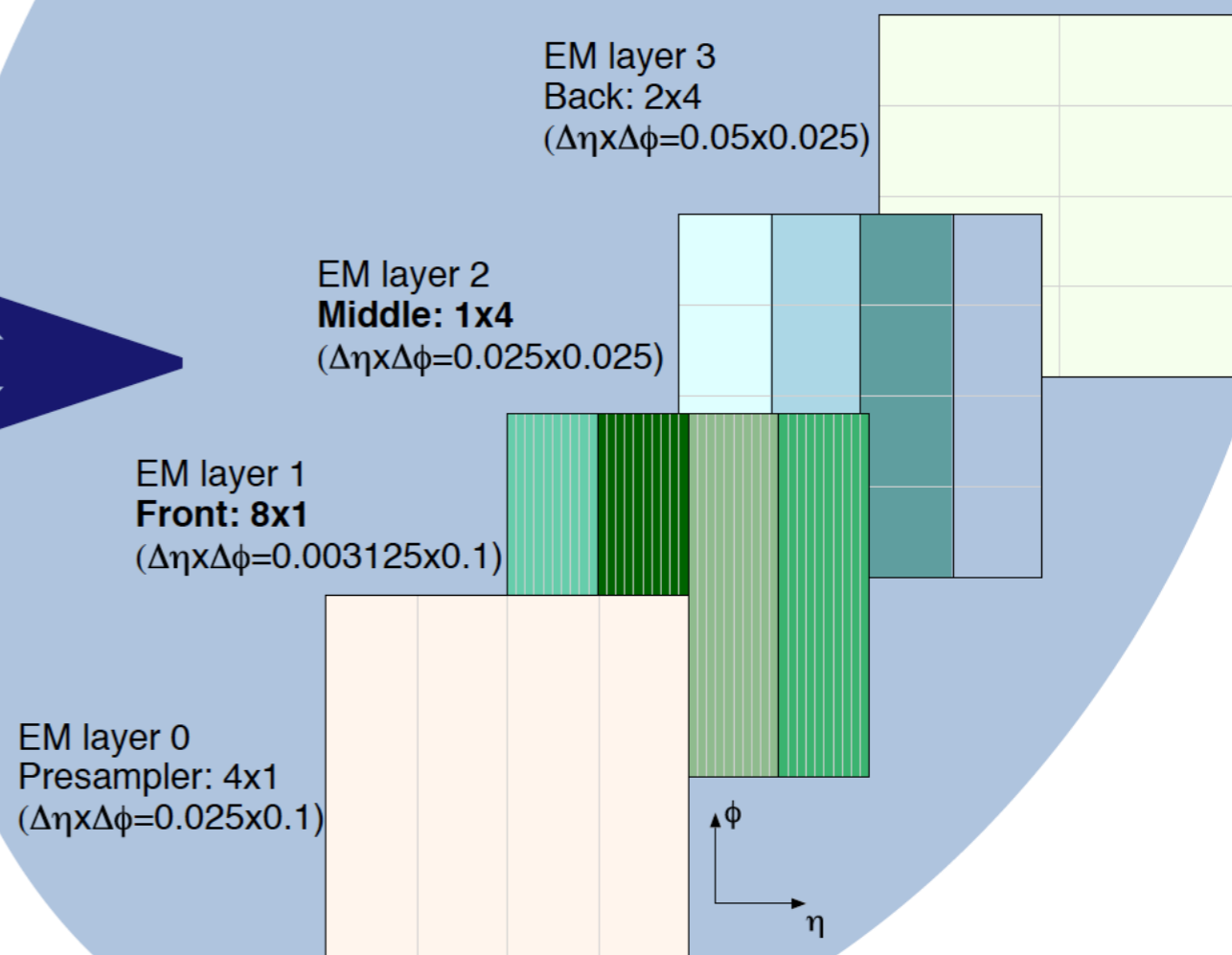
## Existing System

Level-1 Trigger Granularity (Trigger Towers)  
60 cells per Trigger Tower; all layers summed

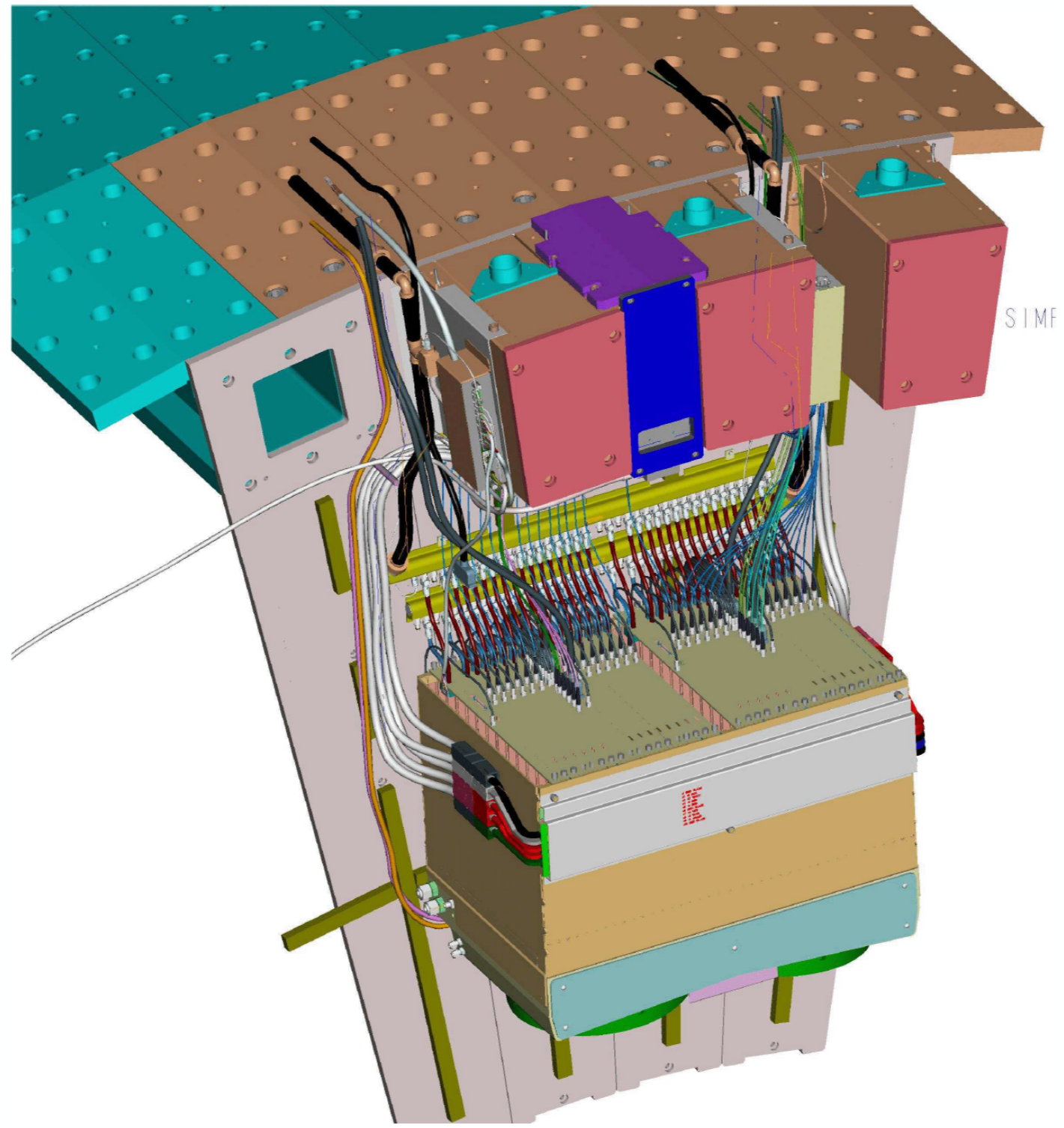


## Phase-I Upgrade

Level-1 Trigger Granularity (Super Cells)  
10 Super Cells per Trigger Tower



# Front-end crate location

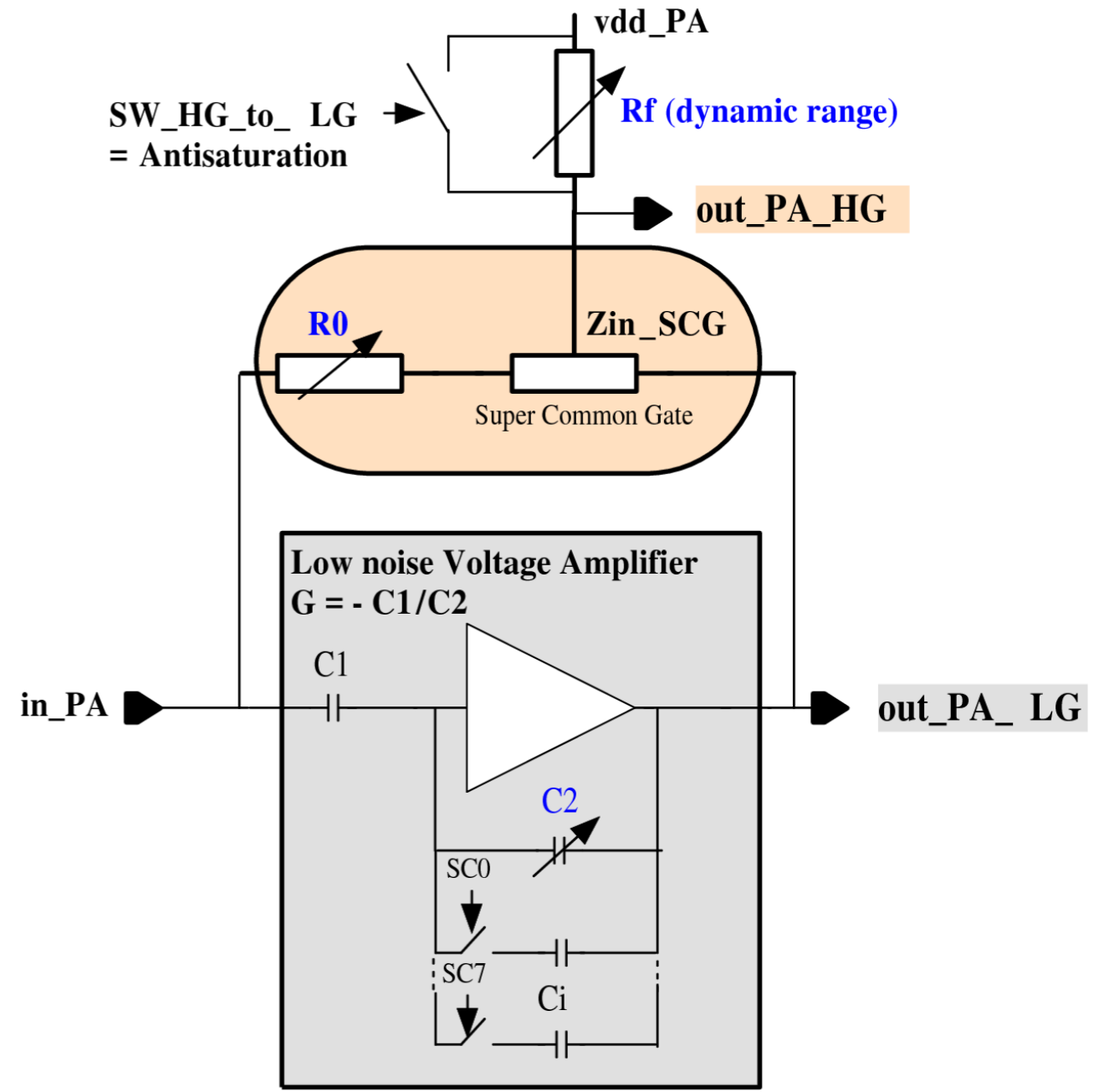
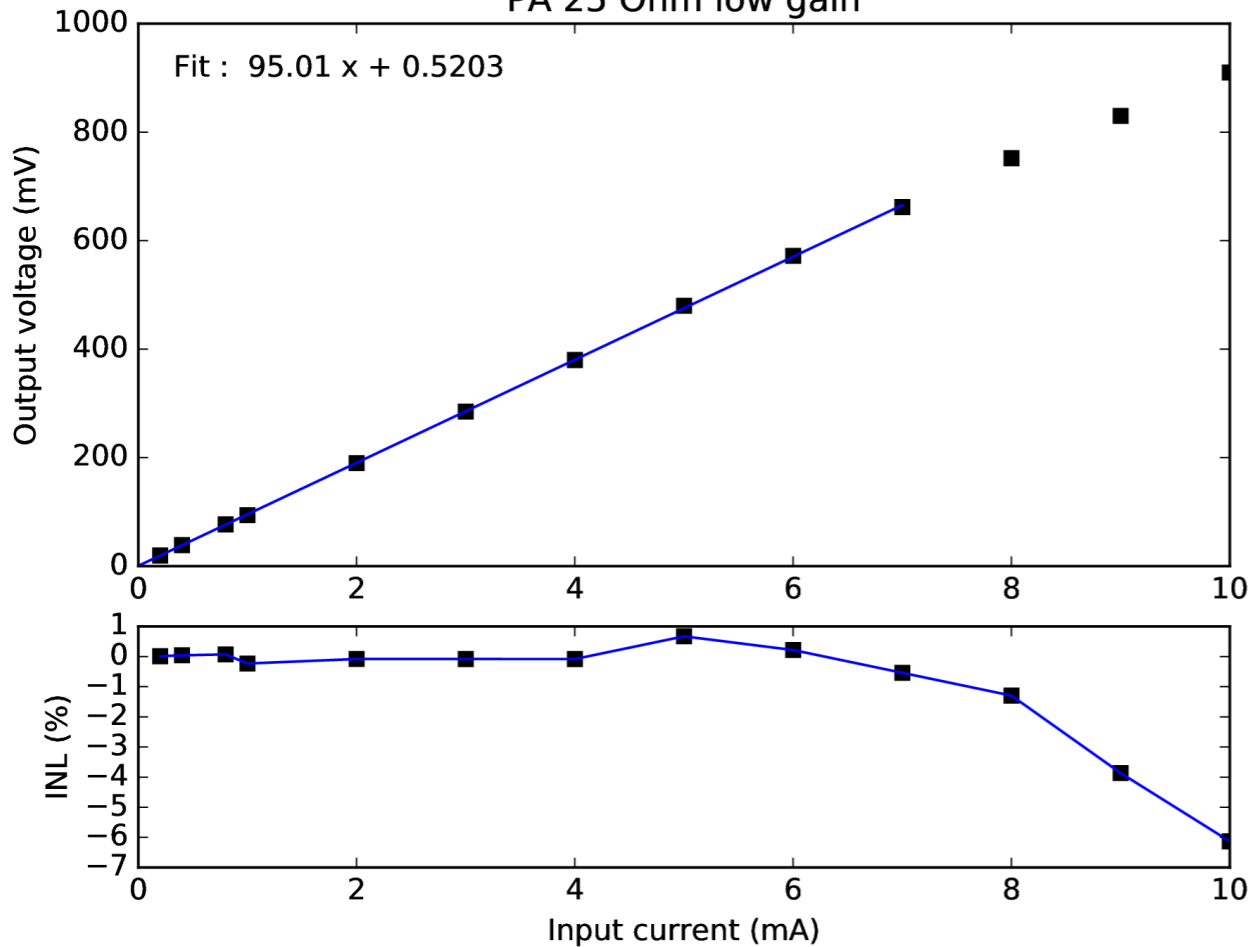


“Electronically cooled” resistor

$$\frac{4kTR_0}{(1 + |G|)^2}$$

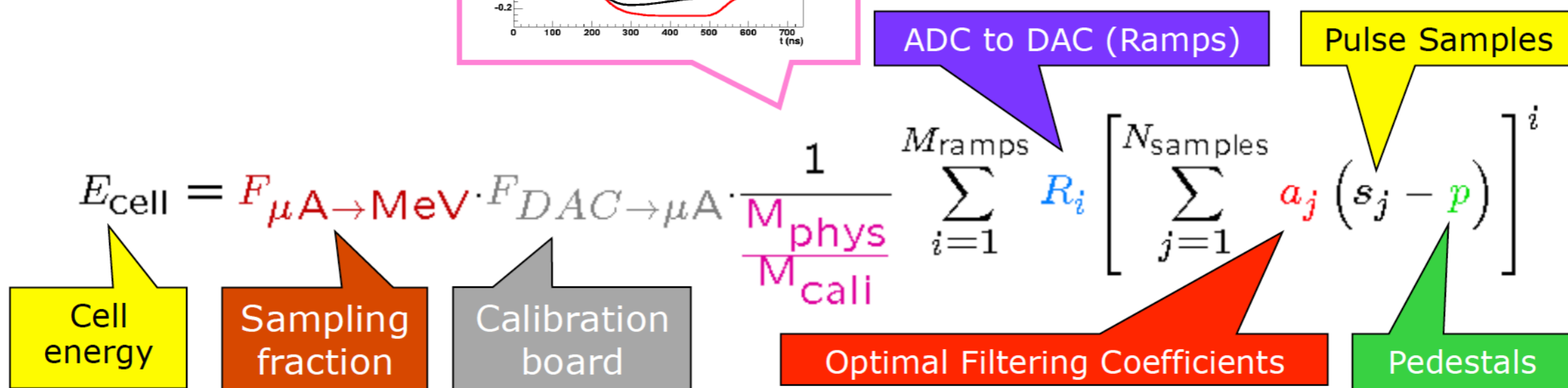
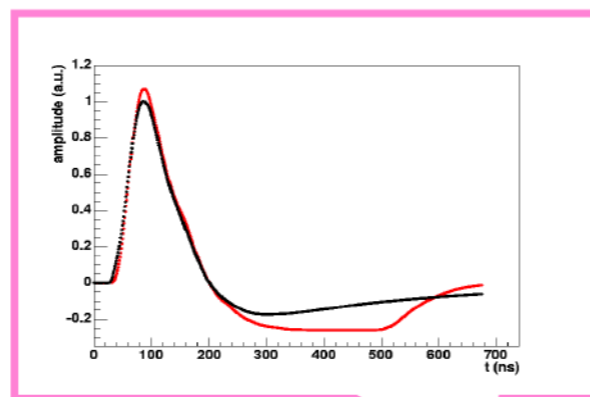
## Linearity after shaping

PA 25 Ohm low gain



$R_0, C_2$  tuneable to set absolute value of  $Z_{in}$   
 $C_i$ : 8-bit fine adjustment of  $Z_{in}$  ( $\pm 5\%$ )  
 using Slow Control parameters

# Optimal Filtering and Calibration Chain



The above formula describes the LAr electronic calibration chain (from the signal ADC samples to the raw energy in the cell). Note that this version of the formula uses the general  $M_{\text{ramps}}$ -order polynomial fit of the ramps. We use a linear fit as the electronics are very linear, and we only want to apply a linear gain in the DSP in order to be able to undo it offline, and apply a more refined calibration. In this case, the formula is simply:

$$E_{\text{cell}} = F_{\mu\text{A} \rightarrow \text{MeV}} \cdot F_{\text{DAC} \rightarrow \mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \cdot R \left[ \sum_{j=1}^{N_{\text{samples}}} a_j (s_j - p) \right]$$

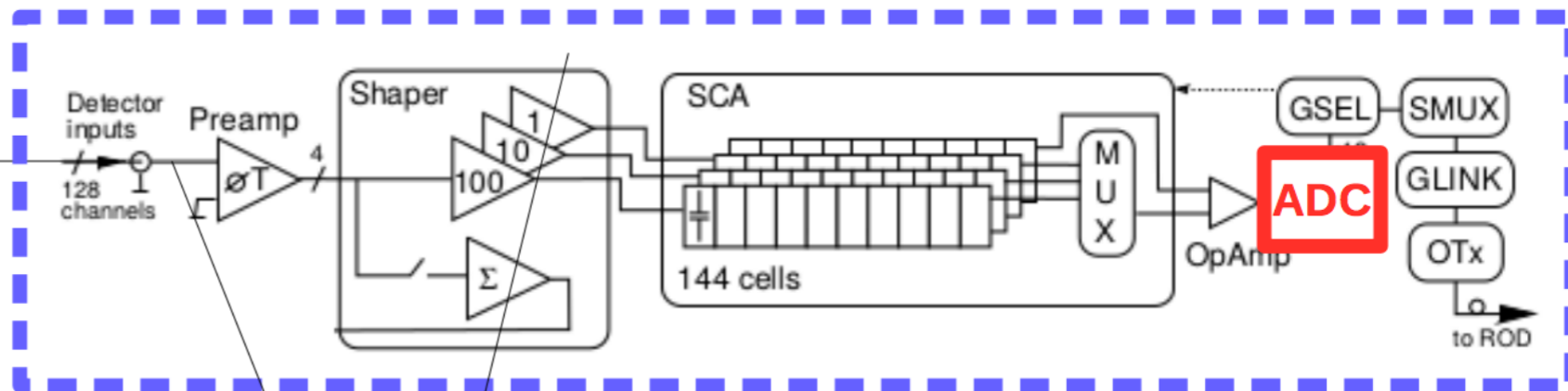
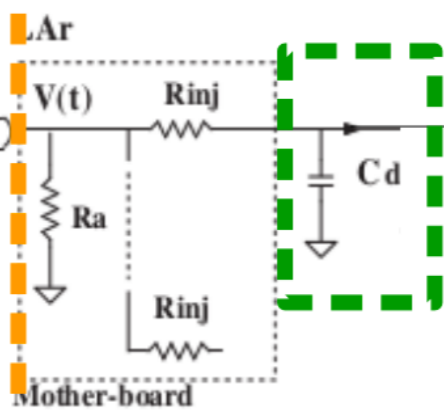
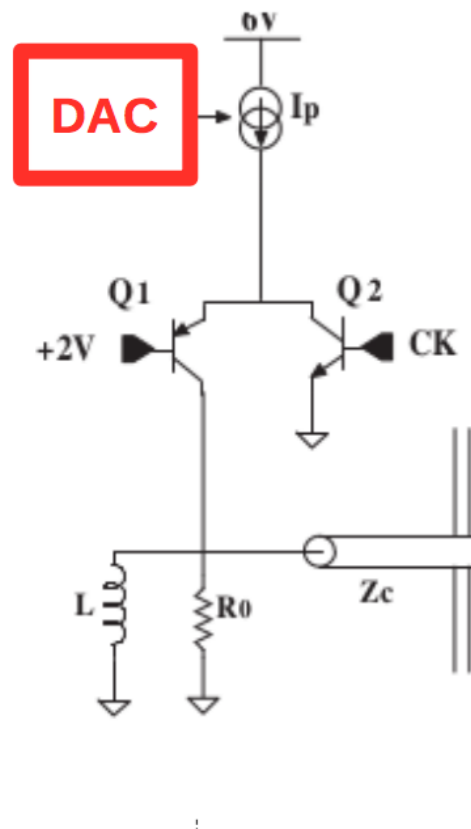
# Calibration

Digital pulse command

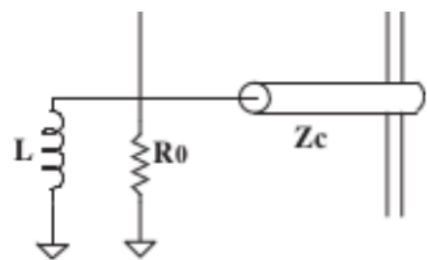
Calibration board

Calorimeter cell

Readout electronics



1 calib line is plugged on several cells  
8 (resp. 32) cells for back/middle (resp. front) layer



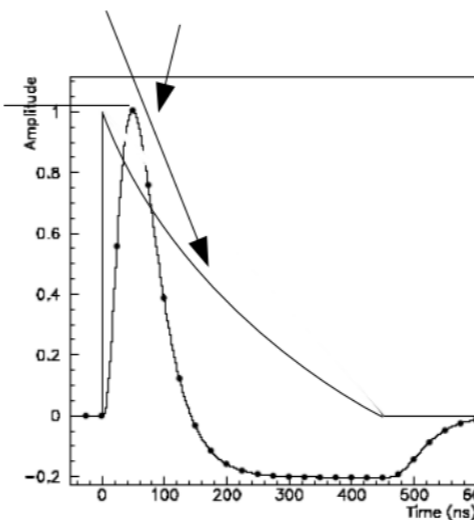
128 calibration lines per calibration board

Exponential calibration pulse ( $\mu A$ )

Shaped pulse (ADC)

Digital pulse samples  $s_i$

$ADC_{max}$



ADC  $\rightarrow$  DAC known from calibration  
DAC  $\rightarrow$   $\mu A$  known from first principle  
 $\mu A \rightarrow$  MeV known from test beam